ZB32L032

ARM® Cortex® -M0+ 32-bit Micro-Controller Datasheet

Version 1.01

2024/1/8

Features

- ARM® Cortex®-M0+ core
  - 64K bytes embedded Flash with write-protect function
  - 16K Byte SRAM
  - Runs up to 64MHz
  - A 24-bit system timer
  - Supports low-power sleep mode
  - Built-in single-cycle 32-bit hardware multiplier
  - 4.3us Wakeup time @Fcpu=32Mhz
- Working conditions
  - Wide voltage operating range 2.5V to 5.5V
  - Wide operating frequency up to 64MHz
  - Operating temperature: -40°C to +85°C
- Clock source
  - 5 optional clock sources
    - External 4MHz~24MHz high speed crystal oscillator
    - External 32.768KHz crystal
    - Internal 4MHz~24MHz high speed clock
    - Internal low-speed 38.4KHz/32.768KHz clock
    - PLL clock Max. 192 MHz
    - Supports hardware clock monitoring
  - RTC
    - Supports RTC counting (seconds/minutes/hours) and perpetual calendar function (day/month/year)
    - Alarm function register support (sec/min/hr/dd/mm/yyyy)
    - Support RTC to wake up the system from Deep Sleep mode
- Power management
  - POR,PDR,LVR
  - Two low-power operating modes: Sleep, Deep Sleep Mode
  - Low voltage detection, configurable as interrupt or reset
  - Wakeup @sleep : all interrupt sources are wakeable
  - Wakeup @Deep sleep: all GPIO PINs with RTC (low speed clock operation)
- Disruptions
  - Nested Vector Interrupt Controller (NVIC) for controlling 32 interrupt sources, each of which can be set to 4 priorities
  - Supports serial debugging (SWD) with 2 watchpoints/4 breakpoints
- General Purpose I/O Pins
  - 39 I/Os in a 48-Pin Package
- Built-in ISP Bootloader
  - Supports program upgrade via UART.
- Timer/Counter
  - General purpose timer: 4x16 bits
  - Advanced Timer: 3x16 bits,1x24bits(SysTick)
  - Programmable counter: 1x16 bits
  - Watchdog Counter : WWDTx1,IWDTx1
  - Base Timer : 2x16bits
  - Low power timer: 1x16bits
- Buzzer Frequency Generator
  - Generates five 1KHz, 2KHz, 4KHz beep signals
- communications interface
  - UART0,1; USART3,4 standard communication interface
  - Ultra-low power LPUART with low-speed clock support
  - QSPI, SPI/I2S standard communication interfaces up to 20 Mbps (with multiplexed I2S interface)
  - I2CX2 standard communication interface, supports up to 1Mbps in master mode and 800Kbps in slave mode.
  - One-Wire communication interface
- ADC
  - 12-bit 1Msps sampling rate, 12-bit SAR Type ADC
  - 24 channels: 16 external pins, 1 internal temperature sensor voltage,2 OPA outputs,1 1/3*VDD, 1 BGR 1.2V, 1 DAC
  - External Reference Voltage : VDD, GPIO(PB01) PIN
  - Built-in reference voltage : 2.5V, 2.048V
- PDMA controller (Primcell µDMA PL230)
  - Support 8 chs : SPI,I2C,USART,Timer,ADC
- PWM

- Supports up to 3 complementary outputs

- DAC(6-bits)x2
- Operational amplifiers (OPA) x 2
- Internal temperature sensor
- Voltage Comparator (VCx2) / Low Voltage Detector (LVD)
- Hardware CRC-16/32 Module, AES Hardware Unit, TRNG True Random Number Generator
- 16-byte (128-bit) Chip Unique ID (UID)
- development tool
  - SWD's full-featured embedded debugging solution
- Package: TSSOP28, QFN32, LQFP32/48

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【1】 Introduction

ZB32L032 is an ultra-low power and wide voltage operating range (2.5V~5.5V) microcontroller embedded with a 32-bit ARM® Cortex-M0®+ core, running up to 64MHz, built-in 64K bytes of embedded Flash, 16K bytes of SRAM, integrated 12-bit 1Msps high-precision SAR ADC (16 channels), DAC (6-bits), OPAx2, RTC, comparator x2, UARTx2, USARTx2, LPUART, SPI/I2S, QSPI, I2Cx2, and PWMx (multiple independent or complementary outputs) and other rich peripheral interfaces, with high integration, high anti-interference, and high reliability.

The ZB32L032 series offers wide voltage operating range, low power consumption, low standby current, highly integrated peripherals, high operating efficiency, fast wake-up, and cost-effective applications, including the following applications:
Small household appliances, chargers, remote controls, electronic cigarettes, gas alarms, digital displays, thermostats, recorders, motor drives, smart door locks, smart sensors, smart homes and smart cities, etc.

【2】 Description

2.1 Overview of equipment

		ZB32L032XXX	ZB32L032XXX	ZB32L032XXX
Pin counts		48	32	28
GPIO		39	25	22
MCU	Core	Cortex M0+		
	CPU Frequency	Up to 64 MHz		
Flash		64K Bytes (50 MHz Access)		
SRAM		16K Bytes		
PDMA		16 CH (SPI, I2C, USART, Timer, ADC)		
Timer	Basic (16-bits)	2x16 bits / 1x32 bits		
	General purpose (16-bits)	4 (T2, T2A, T2B, T2C)		
	Advanced (16-bits)	3 (T1, T1A, T1B)		
	PCA (16-bits)	1		
	SysTick (24-bits)	1		
	Lower power (LPTIMER)	1		
RTC/IWDG/WWDG		1/1/1		
AWK		1		
Operating Voltage Range		2.5~5.5V		
operating temperature		-40~85 ℃		
debugging function		SWD		
unique identifier		16 Bytes		
Communication	UART, USART	2,2	1,1	1,1
	LPUART	1	1	0
	SPI	2 (16/20Mhz)	1 (16/20Mhz)	1 (16/20Mhz)
	I2C	2	2	2
comparator		2	2	2
AES		Yes (128-bytes)		
TRNG		1		
CRC16/32		1		
Internal temperature sensor		1		
Clocks	Internal high-speed crystal	HIRC : 4/8/16/22.12/24MHz		
	Internal low-speed crystal	SIRC : 32.8/38.4KHz		
	External high-speed crystal	HXT : 4M~24MHz		
	External low-speed crystal	LXT : 32.768MHz		
	PLL	PLL : 8M~192Mhz		
12 Bits A/D		17 CH	12 CH	11 CH
OPAx2		2	2	0
buzzers		1		
seal inside		LQFP48	LQFP32/QFN32	TSSOP28

Table 1 ZB32L032 device features and peripheral list

2.2 Block Diagram

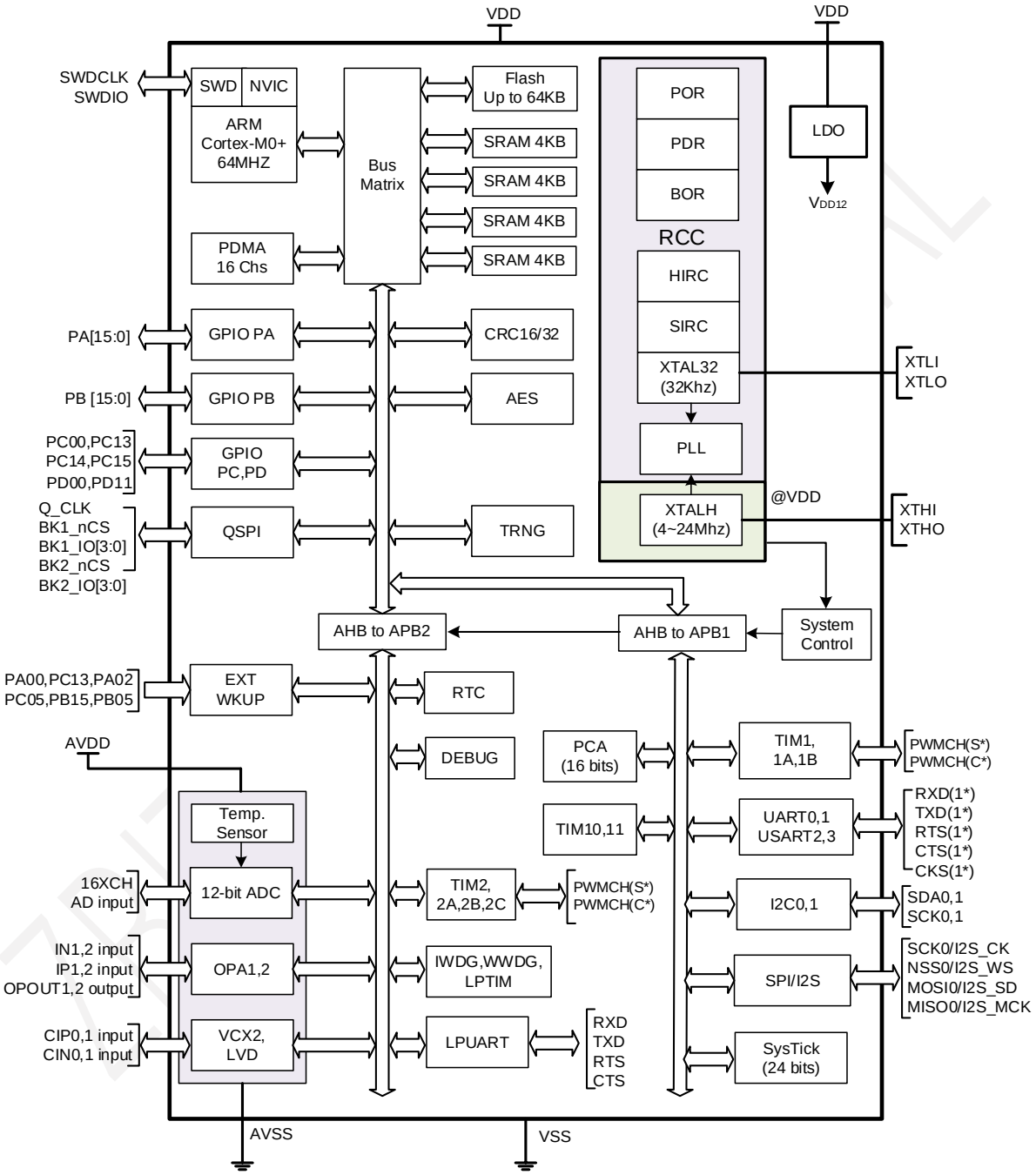


Figure 1 Block Diagram

Note : S*: Maximum channels for Single output ; C*: Maximum channels for complement output .

1* : is UART0,UART1,USART2,USART3

2.3 Pin definition

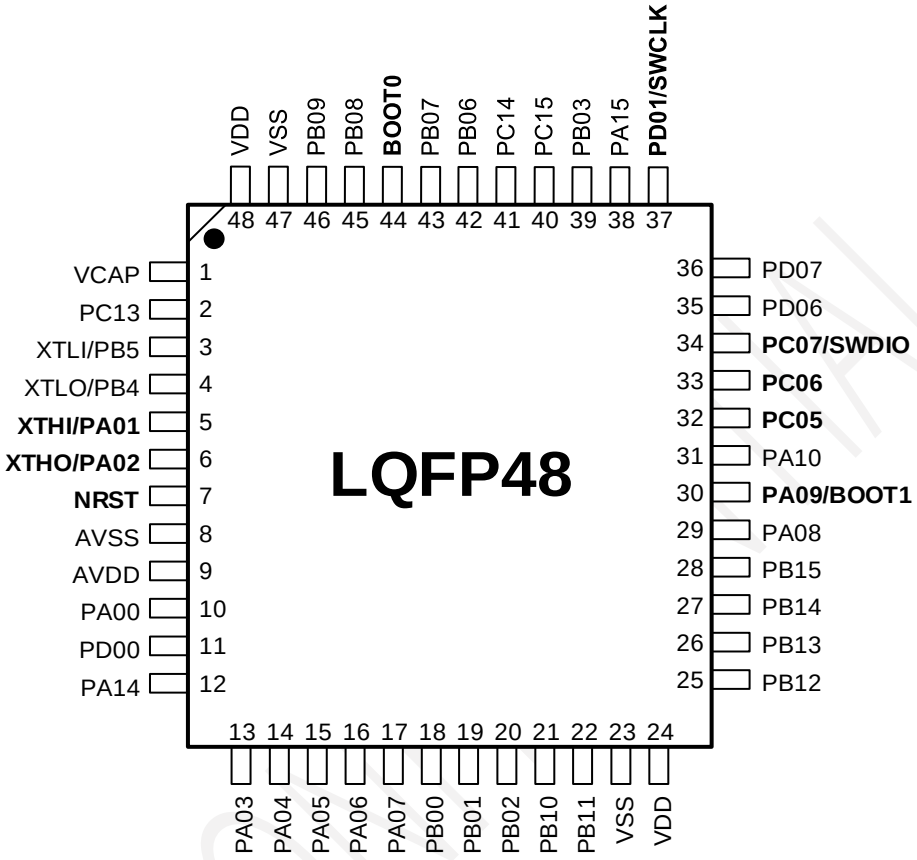


Figure 2 ZB32L032 LQFP48

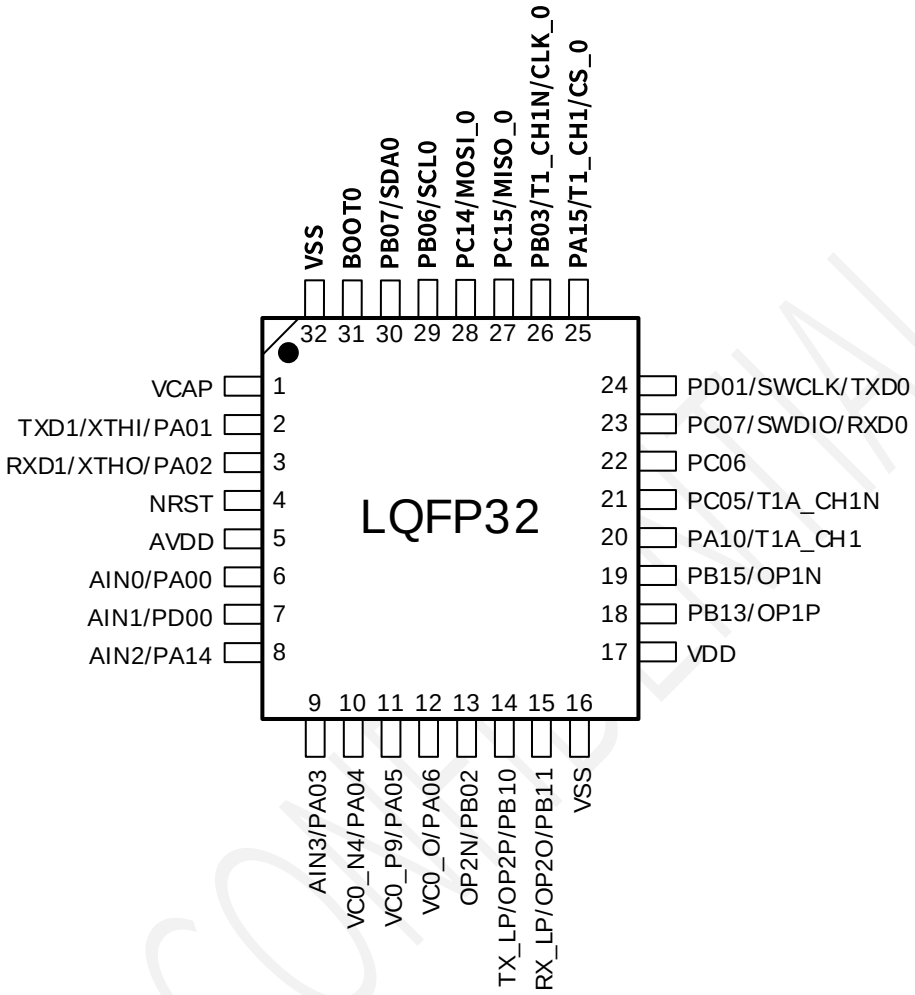


Figure 3 ZB32L032 LQFP32

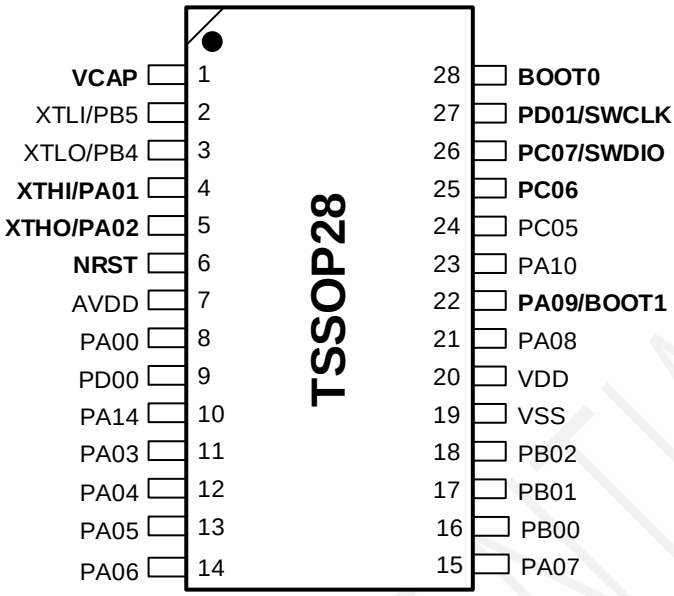


Figure 4 ZB32L032 TSSOP28

2.4 Pin configuration

Pin Num			Pin Name	Power WKUP XTAL ISP	UARTX4 LPUART	SPI/I2S I2CX2	TIM2 PCA LPTIM	TIM2A TIM1	TIM2B TIM1A	TIM2C TIM1B	ADC VCX2 OPAX2	Clock IR LVD SWD
48	32	28										
1	1	1	VCAP	P								
2			PC13	WKUP					T2B_CH4	T2C_CH1		
3		2	PB05	XTLI								
4		3	PB04	XTLO								
5	2	4	PA01	XTHI	TXD_1 CKS_2	SDA_0 Q_CLK	T2_ETR	T1_ETR T2A_ETR	T1A_ETR T2B_ETR	TB1_ETR T2C_ETR		
6	3	5	PA02	XTHO	RXD_1 TXD_2	SCL_0 QBK1_NCS	T2_ETR	T1_CH1 T1_ETR T2A_ETR	T1A_ETR T2B_ETR	TB1_ETR T2C_ETR		
7	4	6	NRST									
8			AVSS	G								
9	5	7	AVDD	P								
10	6	8	PA00	WKUP	RXD_2	QBK1_IO0	T2_CH1 T2_ETR	T1_CH1 T2A_CH1 T1_ETR T2A_ETR	T1A_ETR T2B_ETR	T2C_ETR T1B_ETR	**AIN0** VC0_P4 VC0_N0 VC0_O VC1_P0 VC1_N4	
11	7	9	PD00	WKUP	CTS_2	QBK1_IO1	T2_CH2	T1_CH1N T2A_CH2 T2A_ETR			**AIN1** VC0_P5 VC0_N1 VC1_P1 VC1_N5	
12	8	10	PA14	WKUP	TXD_1 RTS_2	QBK1_IO2	T2_CH3	T1_CH1 T2A_CH1	T2B_CH1		**AIN2** VC0_P6 VC0_N2 VC1_P2 VC1_O	
13	9	11	PA03	WKUP	RXD_1	QBK1_IO3	T2_CH4	T1_CH1N T2A_CH2 T1_ETR	T1A_CH1 T1A_ETR	T1B_CH1 T2C_CH1 T1B_ETR	**AIN3** VC0_P7 VC0_N3 VC1_P3	
14	10	12	PA04	WKUP	TXD_1	CS/WS QBK2_NCS	PCA_CH4 T2_ETR	T2A_CH3 T1_ETR T2A_ETR	T2B_ETR T1A_CH1 T1A_ETR	T1B_CH1N T2C_CH2 T1B_ETR T2C_ETR	**AIN4** VC0_P8 VC0_N4 VC1_P4	
15	11	13	PA05	WKUP		CLK/CK QBK2_IO0	T2_CH1 T2_ETR PCA_ECI	T2A_CH4 T1_ETR T2A_ETR	T1A_CH1N T1A_ETR T2B_ETR	T1B_ETR T2C_ETR	**AIN5** VC0_P9 VC0_N5 VC1_P5	LVD_O

Pin Num			Pin Name	Power WKUP XTAL ISP	UARTX4 LPUART	SPI/I2S I2CX2	TIM2 PCA LPTIM	TIM2A TIM1	TIM2B TIM1A	TIM2C TIM1B	ADC VCX2 OPAX2	Clock IR LVD SWD
48	32	28										
16	12	14	PA06	WKUP	CKS_3	MISO QBK2_IO0	PCA_CH0 T2_ETR	T2A_CH1 T1_ETR T2A_ETR	T1A_ETR T2B_ETR	T1B_CH1 T1B_ETR T2ACETR	**AIN6** VC0_P10 VC0_N6 VC0_O	
17		15	PA07	WKUP	TXD_3	MOSI/SD QBK2_IO0	PCA_CH1	T1_CH1	T2B_CH1	T1B_CH1N T2C_CH1	**AIN7** VC0_P11 VC0_N7 VC1_O	
18		16	PB00	WKUP	RXD_3	QBK2_IO0 MCK	PCA_CH2		T1A_CH1	T2C_CH2	**AIN8** VC0_N10 VC1_N6	MCO
19		17	PB01	WKUP	CTS_3		PCA_CH3		T1A_CH1N	T2C_CH3	**AIN9** **EXVREF** VC1_P6 VC1_N7	
20	13	18	PB02	WKUP	RTS_3		PCA_ECI LPT_TOG	T1_CH1 T1_BK	T1A_BK	T1B_BK	**AIN16** VC1_P7 VC1_N8 OP2_INN	
21	14		PB10	WKUP	TX_LP	SCL_1		T1_CH1 T2A_CH1		T2C_CH1	**AIN17** VC1_P8 OP2_INP	
22	15		PB11	WKUP	RX_LP CKS_2	SDA_1		T1_CH1N		T1B_CH1	**AIN18** OP2_O	
23	16	19	VSS	G								
24	17	10	VDD	P								
25			PB12	WKUP	TXD_2	QBK1_NCS		T1_BK		T1B_CH1	**AIN19** VC1_P9	
26	18		PB13	WKUP	RXD_2	Q_CLK SCL_1		T1A_CH1N		T2C_CH1 T1B_CH1N	**AIN20** VC1_P10 OP1_INP	
27			PB14	WKUP	CTS_2	QBK1_IO0 SDA_1	T2_CH1	T1_CH1	T1A_BK	T2C_CH1	**AIN21** VC1_P11 OP1_O	
28	19		PB15	WKUP	RTS_2	QBK1_IO1	T2_CH2	T1_CH1N		T2C_CH2	**AIN22** OP1_INN	
29		21	PA08	WKUP		QBK1_IO2	T2_CH3	T1_CH1		T2C_CH3		
30		22	PA09	WKUP	TXD_0	QBK1_IO3 SCL_0	T2_CH4	T1_CH1N T1_BK	T1A_CH1	T2C_CH4		
31	20	23	PA10	WKUP	RXD_0	QBK2_NCS SDA_0		T1_CH2	T1A_CH1	T1B_CH1 T2C_CH1 T1B_BK		

Pin Num			Pin Name	Power WKUP XTAL ISP	UARTX4 LPUART	SPI/I2S I2CX2	TIM2 PCA LPTIM	TIM2A TIM1	TIM2B TIM1A	TIM2C TIM1B	ADC VCX2 OPAX2	Clock IR LVD SWD
48	32	28										
32	22	25	PC05	WKUP		SCL_1 MISO QBK2_IO0	T2_ETR	T1_CH2N T1_ETR T2A_ETR	T1A_CH1N T1A_ETR T2B_ETR	T1B_ETR T2C_ETR	VC0_O	MCO
33	22	25	PC06	WKUP		SDA_1 MOSI/(SD) QBK2_IO1	T2_ETR	T1_CH3 T1_ETR T2A_ETR	T1A_CH2 T2B_ETR T1A_ETR	T1B_CH1 T2C_ETR T1B_ETR T2C_ETR	VC1_O	
34	23	26	PC07	WKUP	RXD_0	QBK2_IO2		T1_CH3N T1_ETR	T1A_CH2N T1A_ETR	T1B_CH1N T2C_ETR T1B_ETR		SWDIO LVD_O
35			PD06	WKUP		QBK2_IO3 SCL_1		T1_CH4	T1A_CH3	T1B_CH2		
36			PD07			SDA_1			T1A_CH3N	T1B_CH2N		
37	24	27	PD01	WKUP	TXD_0 TXD_1	MCK		T2A_CH1 T1_ETR	T1A_CH4 T1A_ETR	T1B_CH3 T1B_ETR		SWCLK LVD_O MCO
38	25		PA15	WKUP	RXD_1	CS (WS)	T2_ETR T2_CH1	T2A_CH2 T1_CH1		T1B_CH3N T2C_CH4		
39	26		PB03	WKUP		CLK (CK)	T2_CH2 LPT_Gate	T2A_CH3 T1_CH1N		T2C_CH3 T1B_CH1	VC1_N9	
40	27		PC15	WKUP		MISO_0	PCA_CH0 LPT_ETR	T2A_CH4		T2C_CH2 T1B_CH1N T1B_BK	VC0_P12 VC1_P12 VC1_N10	
41	28		PC14	WKUP		MOSI/SD	PCA_CH1 LPT_Gate	T1_BK		T2C_CH1	VC0_P13 VC1_P13	
42	29		PB06	WKUP	TXD_0	SCL_0 Q_CLK	T2_CH1 LPT_ETR LPT_TOG	T1_CH1 T2A_CH2			VC0_P14 VC1_P14	
43	30		PB07	WKUP	RXD_0	SDA_0 QBK1_NCS	T2_CH2 LPT_TOGN	T1_CH1N	T2B_CH1	T1B_CH1	VC0_P15 VC1_P15	
44	31	28	PD03	BOOT0								
45			PB08	WKUP	TXD_0	SCL_0 Q_CLK		T2A_CH1	T2B_CH2	T2C_CH2 T1B_CH1N		
46			PB09	WKUP	RXD_0	SDA_0 QBK1_NCS			T2B_CH3	T1B_CH4		
47	32		VSS	G								
48			VDD	P								

Table 2 Pin Function Table

2.5 Pin mux description

Pin Num			GPIOX_AFR[i+3:i]										
48	32	28	0	1	2	3	4	5	6	7	8	9	F/Config
1	1	1	VCAP	P	P	P	P	P	P	P	P	P	P
2			PC13			T2C_CH1		T2B_CH4					
3		2	PB05										XTLI
4		3	PB04										XTLO
5	2	4	PA01	SDA_0		TXD_1					CKS_2	Q_CLK	XTHI
6	3	5	PA02	SCL_0	T1_CH1	RXD_1					TXD_2	QBK1_NCS	XTHO
7	4	6	NRST										
8			AVSS	G	G	G	G	G	G	G			G
9	5	7	AVDD	P	P	P	P	P	P	P			P
10	6	8	PA00	TIM10_TOG	T1_CH1	T2_CH1		T2A_CH1		RXD_2	VC0_O	QBK1_IO0	**AIN0** VC0_P4 VC0_N0 VC1_P0 VC1_N4
11	7	9	PD00	TIM10_TOGN	T1_CH1N	T2_CH2	CTS_2	T2A_CH2			TIM11_TOGN	QBK1_IO1	**AIN1** VC0_P5 VC0_N1 VC1_P1 VC1_N5
12	8	10	PA14	TXD_1	T1_CH1	T2_CH3	T2A_CH1	T2B_CH1	TIM11_TOG		RTS_2	QBK1_IO2	**AIN2** VC0_P6 VC0_N2 VC1_P2
13	9	11	PA03	RXD_1	T1_CH1N	T1A_CH1	T1B_CH1	T2A_CH2	T2_CH4		T2C_CH1	QBK1_IO3	**AIN3** VC0_P7 VC0_N3 VC1_P3
14	10	12	PA04	CS/WS	TXD_1	PCA_CH4	T1A_CH1	T1B_CH1N	T2A_CH3		T2C_CH2	QBK2_NCS	**AIN4** VC0_P8 VC0_N4 VC1_P4
15	11	13	PA05	CLK/CK	PCA_ECI		T1A_CH1N	T2_CH1	T2A_CH4	LVDO	VC1_O	QBK2_IO0	**AIN5** VC0_P9 VC0_N5 VC1_P5
16	12	14	PA06	MISO	PCA_CH0		T1B_CH1	T2A_CH1		VC0_O	CKS_3	QBK2_IO1	**AIN6** VC0_P10 VC0_N6

Pin Num			GPIOX_AFR[i+3:i]										
48	32	28	0	1	2	3	4	5	6	7	8	9	F/Config
17		15	PA07	MOSI/SD	PCA_CH1	T1_CH1	T1B_CH1N	T2B_CH1	T2C_CH1	VC1_O	TXD_3	QBK2_IO2	**AIN7** VC0_P11 VC0_N7
18		16	PB00	PCA_CH2	MCK	T1A_CH1	TIM11_G		T2C_CH2	MCO	RXD_3	QBK2_IO3	**AIN8** VC0_N10 VC1_N6
19		17	PB01	PCA_CH3		T1A_CH1N	TIM11_EXT		T2C_CH3		CTS_3		**AIN9** **EXVREF** VC1_P6 VC1_N7
20	13	18	PB02		PCA_ECI	LPT_TOG	T1_CH1	T1_BK	T1A_BK	T1B_BK	RTS_3		**AIN16** VC1_P7 VC1_N8 OP2_INN
21	14		PB10	SCL_1		T1_CH1		T2A_CH1	T2C_CH1		TX_LP		**AIN17** VC1_P8 OP2_INP
22	15		PB11	SDA_1		T1_CH1N		T1B_CH1		CKS_2	RX_LP		**AIN18** OP2_O
23	16	19	VSS	**G**									
24	17	20	VDD	**P**									
25			PB12		T1B_CH1		T1_BK		LXT_out		TXD_2	QBK1_NCS	**AIN19** VC1_P9
26	18		PB13		SCL_1	T1A_CH1N	T1B_CH1N		HXT_out	T2C_CH1	RXD_2	Q_CLK	**AIN20** VC1_P10 OP1_INP
27			PB14		SDA_1	T1_CH1	T2_CH1	T1A_BK	SIRC_out	T2C_CH1	CTS_2	QBK1_IO0	**AIN21** VC1_P11 OP1_O
28	19		PB15		T1_CH1N	T2_CH2	T2C_CH2		HIRC_out		RTS_2	QBK1_IO1	**AIN22** OP1_INN
29		21	PA08	TXD_0		T1_CH1	T2_CH3		BEEP	T2C_CH3		QBK1_IO2	
30		22	PA09 **(BOOT1)**	TXD_0	T1_CH1N	T1A_CH1	T2_CH4	T1_BK	1-Wire	T2C_CH4	SCL_0	QBK1_IO3	
31	20	23	PA10	RXD_0	T1_CH2	T1A_CH1	T1B_CH1	T1B_BK	RTC_1Hz	T2C_CH1	SDA_0	QBK2_NCS	
32	21	24	PC05	TIM10_EXT	MISO	T1_CH2N	T1A_CH1N		MCO	VC0_O	SCL_1	QBK2_IO0	
33	22	25	PC06	TIM10_G	MOSI/SD	T1_CH3	T1A_CH2	T1B_CH1		VC1_O	SDA_1	QBK2_IO1	
34	23	26	PC07		RXD_0	T1_CH3N	T1A_CH2N	T1B_CH1N		LVD_O		QBK2_IO2	**SWDIO** (Config)

Pin Num			GPIOX_AFR[i+3:i]										
48	32	28	0	1	2	3	4	5	6	7	8	9	F/Config
35			PD06	SCL_1		T1_CH4	T1A_CH3	T1B_CH2				QBK2_IO3	
36			PD07	SDA_1			T1A_CH3N	T1B_CH2N					
37	24	27	PD01	TXD_1	TXD_0	T1A_CH4	T1B_CH3	T2A_CH1	LVD_O	MCO	MCK		**SWCLK** (Config)
38	25		PA15	CS/WS	RXD_1	T1_CH1	T1B_CH3N		T2_CH1	T2A_CH2	T2C_CH4		
39	26		PB03	CLK/CK	LPT_GATE		T1_CH1N	T1B_CH1	T2_CH2	T2A_CH3	T2C_CH3		VC1_N9
40	27		PC15	MISO		PCA_CH0	LPT_ETR	T1B_CH1N	T2A_CH4	T1B_BK	T2C_CH2		VC0_P12 VC1_P12 VC1_N10
41	28		PC14	MOSI/SD		LPT_GATE	PCA_CH1	T1_BK		T2C_CH1			VC0_P13 VC1_P13
42	29		PB06	SCL_0	TXD_0	LPT_ETR	LPT_TOG	T1_CH1	T2A_CH2	T2_CH1		Q_CLK	VC0_P14 VC1_P14
43	30		PB07	SDA_0	RXD_0	LPT_TOGN	T1_CH1N	T1B_CH1	T2_CH2	T2B_CH1		QBK1_NCS	VC0_P15 VC1_P15
44	31	28	PD03 **(BOOT0)**										
45			PB08	SCL_0	TXD_0	T1B_CH1N	T2A_CH1	T2B_CH2	T2C_CH2			Q_CLK	
46			PB09	SDA_0	RXD_0			T2B_CH3	T1B_CH4			QBK1_NCS	
47	32		VSS	G									
48			VDD	P									

Table 3 Select Chip Pin Table

2.6 Pin description

Function	Pin name	Description
Power	VDD	Power supply
	AVDD	Power supply
	VCAP	Internal LDO output. It must be connected an external capacitor, at least 1uf.
Ground	VSS	Ground
	AVSS	Ground
GPIO (x=0~15)	PAx, PBx, PCx, PDx	PAx general purpose digital input/output pins
NRST	NRST	External Reset Input, Low Active
ADC	AIN0~AIN23	ADC input channel 0~23
	EXVREF	ADC external reference voltage
OPA X=0, 1, 2	OPx_INN	OPA Negative
	OPx_INP	OPA Positive
	OPx_O	OPA Output
VC X=0, 1	VCxN0~VCxN11	Select VC0 , VC1 negative inputs
	VCxP0~VCxP11	Select VC0,VC1 positive inputs
	VCx_O	VC0,VC1 Comparison Outputs
LVD	LVD_O	Voltage Detection Output
ISP	BOOT0 BOOT1	When reset BOOT0 (PD03) pin is high level chip works in ISP programming mode, can be programmed through the ISP protocol for FLASH. When the BOOT0 (PD03) pin is low during reset, the chip operates in user mode and the chip executes the program code within FLASH, which can be programmed via the SWD protocol.
WKUP	All GPIO	External Wakeup input
LPUART	TXD_LP	LPUART Data Transmitter
	RXD_LP	LPUART Data Receiver
UART x=0,1,2,3 USART y=2,3	CKS_y	USART_y CKS
	RTS_x	USART_y RTS
	CTS_x	USART_y CTS
	TXD_x	UART_x Data Transmitter
	RXD_x	UART_x data receiver

Function	Pin name	Description
SPI	MISO	SPI Master Input/Slave Output signal
	MOSI	SPI Master Output/Slave Input signal
	CLK	SPI Clock signal
	CS	SPI Enable signal
I2C x=0,1	SDA_x	I2C Data signal
	SCL_x	I2C Clock signal
General purpose timer, TIMx X=2,2A,2B,2C	Tx_CH1,2,3,4	Timer x capture input/comparison output/PWM output Ch1,2,3,4
	Tx_ETR	External count input signal for Timerx
PCA timer	PCA_ECI	External clock input signal
	PCA_CH0~PCA_CH4	Capture Input/Compare Output/PWM Output 0~4
Advanced Timer TIMX Timer1, 1A, 1B	TIM1_CH1,2,3,4	TIM1 PWM output channel 1/2/3/4
	TIM1_CH1N,2N,3N	TIM1 PWM output Inverted channel 1N/2N/3N
	TIM1_BKIN	TIM1 Brake signal input
	TIM1A_CH1,2,3,4	TIM1 PWM output channel 1/2/3/4
	TIM1A_CH1N,2N,3N	TIM1 PWM output Inverted channel 1N/2N/3N
	TIM1A_BKIN	TIM1 Brake signal input
	TIM1B_CH1,2,3,4	TIM1 PWM output channel 1/2/3/4
	TIM1B_CH1N,2N,3N	TIM1 PWM output Inverted channel 1N/2N/3N
	TIM1B_BKIN	TIM1 Brake signal input
LPTimer	LP_ETR	LP Timer External counting input signal
	LP_GATE	LP Timer GATE input signal
	LP_TOG	Compare Output Positive
	LP_TOGN	Compare Output Negative
QSPI	BK1_IO0~IO3	QSPI host (slave) Input/output data signals
	BK2_IO0~IO3	QSPI host (slave) Input/output data signals
	Q_CLK	SPI clock signal
	BK1_nCS,BK2_nCS	SPI chip select enable

Table 4 Pin description table

2.7 Serial Interface Description

Number / Serial	0	1	2	3	4	5	6
I2C	SCL_0 SDA_0	SCL_1 SDA_1					
SPI	CS CLK MISO MOSI						
QSPI	BK1_IO0~IO3 BK2_IO0~IO3 Q_CLK BK1_nCS BK2_nCS						
UART	CTS_0 RTS_0 TXD_0 RXD_0	CTS_1 RTS_1 TXD_1 RXD_1	CTS_2 RTS_2 TXD_2 RXD_2	CTS_3 RTS_3 TXD_3 RXD_3			
LPUART	CTS_LP RTS_LP TXD_LP RXD_LP						
PWM Independent output	T1_CH1/ T1_CH2/ T1_CH3/ T1_CH4/ PCA_CH0/ PCA_CH1/ PCA_CH2/ PCA_CH3/ PCA_CH4/	T1A_CH1/ T1A_CH2/ T1A_CH3/ T1A_CH4/	T1B_CH1 T1B_CH2 T1B_CH3 T1B_CH4	T2_CH1 T2_CH2 T2_CH3 T2_CH4	T2A_CH1 T2A_CH2 T2A_CH3 T2A_CH4	T2B_CH1 T2B_CH2 T2B_CH3 T2B_CH4	T2C_CH1 T2C_CH2 T2C_CH3 T2C_CH4
PWM Complementary outputs	T1_CH1, 1N T1_CH2, 2N T1_CH3, 3N	T1A_CH1, 1N T1A_CH2, 2N T1A_CH3, 3N	T1B_CH1, 1N T1B_CH2, 2N T1B_CH3, 3N				

Table 5 Serial Interface Description Table

Note.

PWM complementary outputs : Tx_CHx -> Positive, Tx_CHxN -> Negative

【3】 Memory Mapping

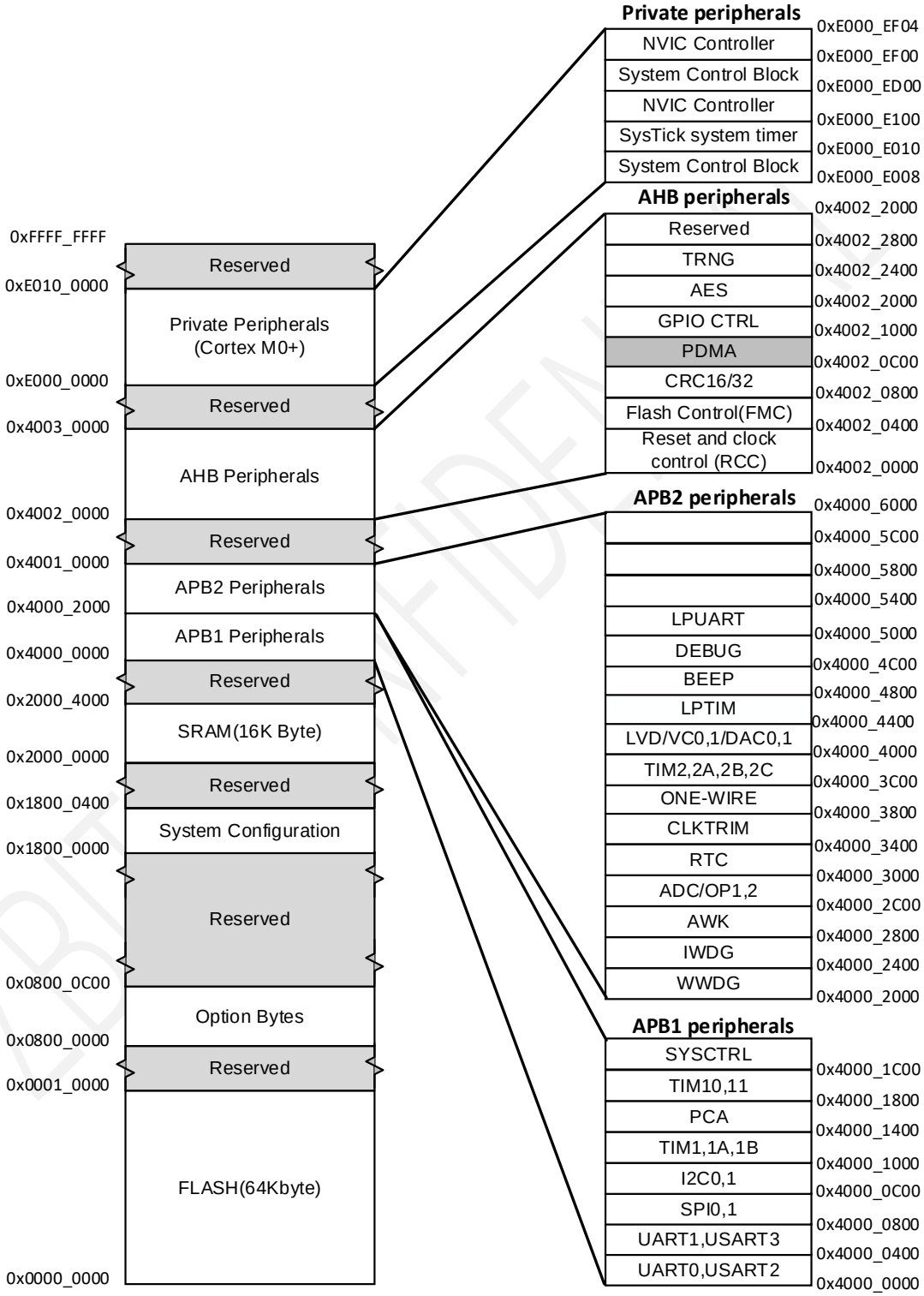


Figure 5 Memory map

【4】 Typical Application Circuit

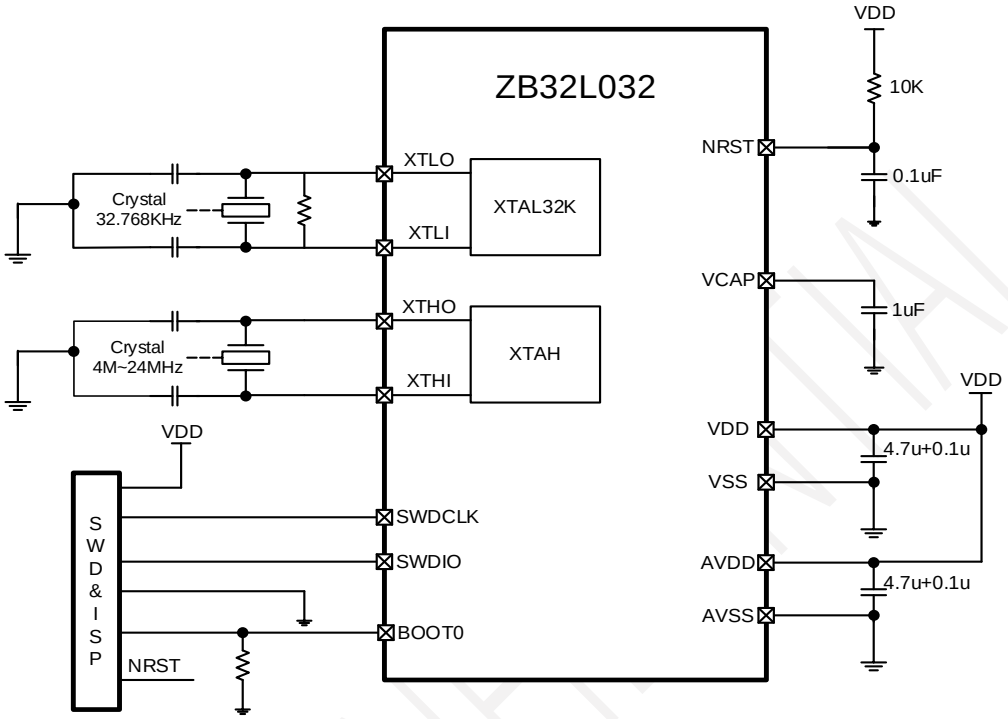


Figure 6 Typical Application Circuit Diagram

【5】 Electrical Characteristics

5.1 Test conditions

Unless otherwise specified, all voltages are referenced to VSS.

5.1-1 Minimum and maximum values

Unless otherwise stated, all minimum and maximum values are guaranteed at the worst ambient temperature, supply voltage and clock frequency conditions by testing 100% of the products on the production line at ambient temperatures T_A =25°C and $T_{A\ =Top,Max}$ ($Top_{,Max}$ matches the temperature range corresponding to the selected Part Number).

In the notes below each table, it is stated that the data obtained through comprehensive evaluation, design simulation and/or process characterization will not be tested on the production line; on the basis of the comprehensive evaluation, the minimum and maximum values are obtained by taking the average of the samples tested and adding or subtracting three times the standard distribution (mean ±3Σ).

5.1-2 Typeical values

Typeical data is based on T_A =25°C and VDD=3.3V (2.5V ⩽ VDD ⩽ 5.5V voltage range) unless otherwise noted. These data are for design guidance only and have not been tested.

Typeical ADC accuracy values are obtained by sampling a standardized batch, tested over all temperature ranges, with 95% of the products having an error less than or equal to the value given (average ±2Σ).

5.2 Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Type	Max	Unit
VDD-VSS	External main supply voltage		2.5		5.5	V
AVDD-AVSS						
V_{IO}	IO voltage		-0.3		VDD+0.3	V
T_{STG}	Storage temperature		-40	25	150	°C
T_{OP}	Work temperature		-40	25	85	°C
F_{CPU}	CPU work frequency		32.768K	24M	64M	Hz
$V_{ESD, HBM}$	Refer to 5.3-10.1					
$V_{ESD, CDM}$	Refer to 5.3-10.1					
$V_{ESD, MM}$	Refer to 5.3-10.1					

Note :

1. CP tests high temperature 85°C, and low temperature -40°C. And high temperature 85°C chip level test is only tested in laboratory and Production Quality Qualification.
2. Frequency test method: The 64MHz frequency is tested in the CP test, and Final Test only focuses on the defects of the packaging process.

5.3 Operating conditions

5.3-1 General operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit	Reference
VDD	Standard operating voltage	-	2.5	5.5	V	
C_S	VCAP Capacitors	-	0.47	2.2	μF	Recommended 1.0μF
T_{OP}	Operating temperature		-40	85	°C	

Note:

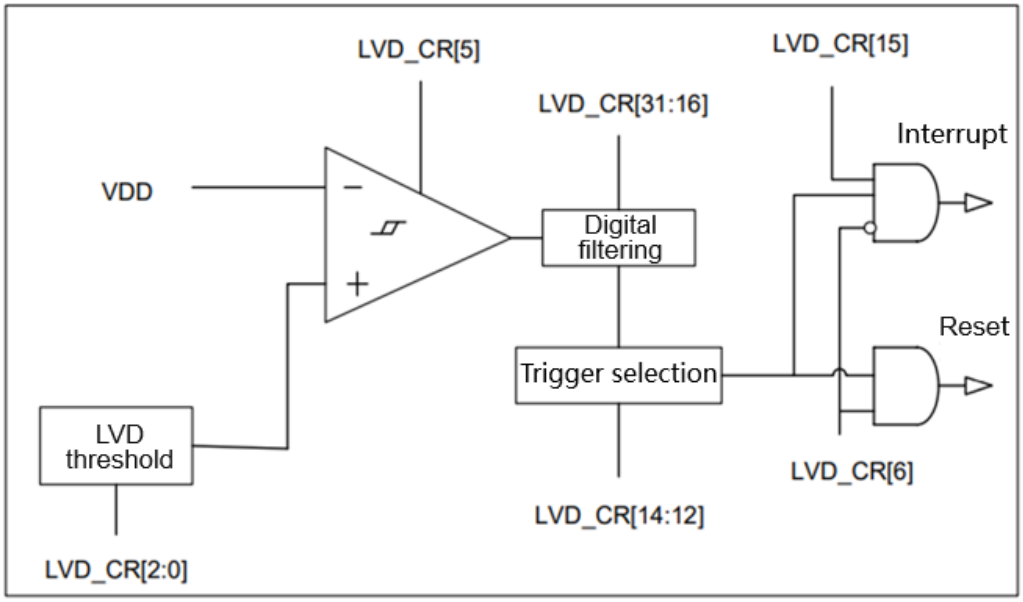
1. The recommended operating conditions are those that ensure the normal operation of the semiconductor chip. All specification values of electrical characteristics are guaranteed within the recommended operating conditions. Be sure to use semiconductor chips under recommended operating conditions. Use beyond this condition may affect semiconductor reliability.
2. The company does not guarantee the use of items, conditions of use or logical combinations not described in this data sheet. If the user considers using this chip outside the listed conditions, please contact the sales representative in advance.

5.3-2 Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Type	Max	Unit
V_{POR} V_{BOR}	POR voltage threshold (Rising voltage on VDD) BOR voltage threshold (Falling voltage on VDD)		2.2	2.25	2.3	V

Note: Guaranteed by design, not tested in production

5.3-3 Embedded Reset and LVD Characteristics



Symbol	Parameter	Conditions	Min	Type	Max	Unit
Vleve	VDD Detectable threshold	lvd_cr[2:0] = 000 (4.4v)	4.20	4.39	4.54	V
		lvd_cr[2:0] = 001 (4.0v)	3.78	3.95	4.08	
		lvd_cr[2:0] = 010 (3.6v)	3.44	3.59	3.72	
		lvd_cr[2:0] = 011 (3.3v)	3.14	3.29	3.4	
		lvd_cr[2:0] = 100 (3.1v)	2.90	3.04	3.16	
		lvd_cr[2:0] = 101 (2.9v)	2.70	2.82	2.92	
		lvd_cr[2:0] = 110 (2.7v)	2.52	2.63	2.72	
		lvd_cr[2:0] = 111 (2.5v)	2.36	2.46	2.54	
I_{comp}	Detector's current	@25°C	0.7	1	1.3	μA
Tresponse	Detector's response time when VDD fall below or rise above the threshold.	@25°C	2	3	4	μs
T_{setup}	Detector's setup time when ENABLE. VDD unchanged.	@25°C	3	5	10	μs

Note: Data based on evaluation results, not tested in production.

5.3-4 Built-in Reference Voltage

Symbol	Parameter	Conditions	Min	Type	Max	Unit
V_{CAP}	Internal 2.5V Reference Voltage	-40~85°C 2.8~5.5V	2.54*(1-5%)	2.54V	2.54*(1+5%)	V
$V_{2.048}$	Internal 2.048V Reference Voltage	-40~85°C 2.8~5.5V	2.048*(1+5%)	2.048V	2.048*(1+5%)	V
T_{START}	Built-in reference voltage $V_{2.048}$ Start-up time		4			us
T_{S_temp}	Reading $V_{2.048}$ ADC sampling time		5			us

Note:

(1*) : Guaranteed by design, not tested in production.

Built-in reference voltage V2.048 Calibration value Name	Description	Stored address
VREFINT_CAL	VREFINT ADC raw data acquired at temperature of 25° C, VDD=3.3V	0x1800_002C~0x1800_002D

5.3-5 Supply Current Characteristics

Symbol	Parameter	Conditions			Type	Max	Unit
I_{DD} (Run Mode in RAM)	All Peripherals clock OFF, Run while(1) in RAM	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource:HIRC HCLK=HIRC PLL off	4M	223.8	270.6	μA
				8M	293.5	333.5	
				16M	430	469	
				24M	566	603	
			Clocksource:HXT(8M) HCLK=PLL, HIRC Off	32M	1402	1495	
				64M	1811	1908	
I_{DD} (Run Mode in FLASH)	All Peripherals clock ON, Run while(1) in Flash	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource:HIRC HCLK=HIRC PLL off	4M	697	768	μA
				8M	1161	1268	
				16M	2110	2274	
				24M	3046	3260	
			Clocksource:HXT(8M) HCLK=PLL, HIRC Off	32M	4450	4600	
				64M	6340	6500	
	All Peripherals clock OFF, Run while(1) in Flash	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource:HIRC HCLK=HIRC,PLL off	4M	449	485	μA
				8M	644	699	
				16M	1040	1132	
				24M	1435	1565	
			Clocksource:HXT(8M) HCLK=PLL,HIRC Off	32M	2550	2690	
				64M	3560	3740	
	All Peripherals clock ON, Run while(1) in Flash	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource: LXT32.768KHz Driver=1	Ta=-40°C	160.2	173.8	μA
				Ta=25°C	162.3	177.8	
				Ta=50°C	166.9	176.4	
				Ta=85°C	175.8	189.4	
	All Peripherals clock OFF, Run while(1) in Flash	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource: LXT32.768KHz Driver=1	Ta=-40°C	158.1	171.8	μA
				Ta=25°C	159.9	174.8	
				Ta=50°C	164.7	174.2	
				Ta=85°C	173.5	187.1	
I_{DD} (Sleep Mode)	All Peripherals clock ON	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource:HIRC	4M	430	456.5	μA
				8M	701	730.3	
				16M	1241	1279	
				24M	1816	1816	
	All Peripherals clock OFF	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource:HIRC	4M	204.5	229.4	μA
				8M	247.1	272.8	
				16M	333	385.5	
				24M	415	442.7	

Symbol	Parameter	Conditions			Type	Max	Unit
	All Peripherals clock ON	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource: LXT32.768KHz Driver=1	Ta=-40°C	77.8	94.6	μA
				Ta=25°C	79.5	90.2	
				Ta=50°C	81.5	93.5	
				Ta=85°C	89.1	101.6	
	All Peripherals clock OFF	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource: LXT32.768KHz Driver=1	Ta=-40°C	75.8	92.5	μA
				Ta=25°C	77	88.2	
				Ta=50°C	79.1	91.5	
				Ta=85°C	87.2	99.7	
I_{DD} (Deep Sleep Mode)	All Peripherals clock OFF, except RTC, IWDG, LPTIM, AWK	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource: SIRC32.768KHz	Ta=-40°C	0.9	1	μA
				Ta=25°C	1.1	1.3	
				Ta=50°C	2	3	
				Ta=85°C	7.3	11.2	
	All Peripherals clock OFF, except RTC	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource: SIRC32.768KHz	Ta=-40°C	0.9	0.9	μA
				Ta=25°C	1.1	1.3	
				Ta=50°C	1.9	2.8	
				Ta=85°C	7.3	11.1	
	All Peripherals clock OFF, except IWDG	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource: SIRC32.768KHz	Ta=-40°C	0.9	1	μA
				Ta=25°C	1.1	1.3	
				Ta=50°C	1.9	2.8	
				Ta=85°C	7.3	11.1	
	All Peripherals clock OFF, except LPTIM	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource: SIRC32.768KHz	Ta=-40°C	0.9	0.9	μA
				Ta=25°C	1.1	1.3	
				Ta=50°C	1.9	2.8	
				Ta=85°C	7.3	11.1	
	All Peripherals clock OFF, except AW	V_{core} =1.2V VDD=2.5V-5.5V	Clocksource: SIRC32.768KHz	Ta=-40°C	0.8	0.9	μA
				Ta=25°C	1.1	1.3	
				Ta=50°C	1.9	2.8	
				Ta=85°C	7.4	11	
	All Peripherals clock OFF	V_{core} =1.2V VDD=2.5V-5.5V		Ta=-40°C	0.6	0.7	μA
				Ta=25°C	0.7	1	
				Ta=50°C	1.7	2.6	
				Ta=85°C	7	10.9	

Note:

1. Data based on TT Wafer appraisal results, not tested in production
2. Typeical values are measured at Ta=25°C, VDD=3.3V unless otherwise noted.
3. Unless otherwise specified, maximum values are measured at Ta=-40°C~85°C, VDD=2.5V~5.5V.

5.3-6 Wakeup time from low-power modes

The wake-up time is the time the chip wakes up from deep sleep mode by an external interrupt. The clock source is HIRC. VDD = 3.3V

Symbol	Parameter	Conditions	Min	Type	Max	Unit
T_{wakeup}	Deep sleep mode to activemode	HIRC=24M HCLK=4M	80	85	90	μs

Note: Data based on assessment results, not tested in production

5.3-7 External Clock Source Characteristics

5.3-7.1 Low-speed External Clock LXT

Symbol	Parameter	Condition	Min	Type	Max	Unit
F_{SCLK}	Crystal frequency			32.768		KHz
ESR_{SCLK}	Supportedcrystal equivalent Series resistance		40	65	85	KOhm
R_{FB}	Feedback resistance			1000		KOhm
C_{SCLK}(1)	Supported crystal external external load range	There are two C_{SCLK} on 2 crystal pins respectively		12		pF
Idd(2)	Current consumption when stable	ESR=65KOhm CSCLK=12pF @max driving	460	760	960	nA
DC_{SCLK}	Duty cycle			50		%
T_{start}(3)	Start-up time	ESR=65KOhm CSCLK=12pF 40%~60% duty cycle Reached Max @ 85 Co	150	300	450	ms

Note.

(1) It is recommended that a crystal be used to give a reference value

(2) RCC_LXTCR.LXTDRV=0011, ESR=65K

(3) Data based on appraisal results, not tested in production

5.3-7.2 High-Speed External Clock HXT

Symbol	Parameter	Condition	Min	Type	Max	Unit
F_{FCLK}	Crystal frequency		4	16	24	MHz
ESR_{FCLK}	Supported crystal equivalent series resistance		30	60	1500	Ohm
C_{FCLK}(1)	Supported crystal external external load range	There are 2 C_{FCLK} on 2 crystal pins individually		12		pF
Idd(2)	Supported crystal external external load range	24MHz Xtal ESR=30Ohm C_{FCLK} =12pF	200	300	400	μA
DC_{FCLK}	Duty cycle		45	50	55	%
Tstart	Start up time	24M	450	550	650	μA

Note.

(1) It is recommended that a crystal be used to give a reference value.

(2) Current consumption could vary with oscillating frequency, RCC_HXTCR.HXTDRV=111.

(3) Data based on appraisal results, not tested in production.

5.3-7.3 PLL Characterization

Symbol	Parameter	Condition	Min	Type	Max	Unit
F_{clkin}	PLL Input Reference Frequency			4		MHz
F_{out}	PLL Output Frequency		32		64	MHz
Fvco	VCO		128		192	MHz
Tstable	stabilization time	VDD = 5V PLLTRIM = 0x92 PLLSTARTUP[1:0] = 0	105		143	us
$Idd_{(PLL)}$	Current consumption	VDD = 5V	450	520	600	μA
DC_{FCLK}	Duty cycle		40	50	60	%
F_{PJ}	period Jitter	PLL output 64MHz	0.75 @-40 C°	2	3.6 @90 C°	ns

5.3-8 Internal Clock Source Characteristics

5.3-8.1 High-speed internal RC oscillator (HIRC)

Symbol	Parameter	Condition	Min	Type	Max	Unit
F_{MCLK}	Internal RC Oscillation frequency		4.0	4.0 8.0 16.0 24	24	MHz
T_{Mstart}(1)	Start-up time Not including software calibration	F_{MCLK}=4MHz	3.17	3.32	3.41	μs
		F_{MCLK}=8MHz	3.18	3.32	3.41	μs
		F_{MCLK}=16MHz	3.25	3.33	3.47	μs
		F_{MCLK}=24MHz	3.19	3.29	3.37	μs
I_{MCLK}	Current consumption	F_{MCLK}=4MHz	92.7	104.62	113.81	μA
		F_{MCLK}=8MHz	105.59	115.59	123.89	μA
		F_{MCLK}=16MHz	123.75	133.41	144.67	μA
		F_{MCLK}=24MHz	143.31	153.25	166.93	μA
DC_{MCLK}	Duty cycle		45	50	55	%
D_{evM}	Frequency Deviation	VDD = 2.5V~5.5V Ta = -40°C~85°C	-2.5		+2.5	%

Note: Data based on assessment results, not tested in production.

5.3-8.2 Low-speed internal RC oscillator (SIRC)

Symbol	Parameter	Condition	Min	Type	Max	Unit
F_{ACLK}	Internal RC Oscillation frequency		37.83 32.28	38.43 32.768	38.97 33.26	KHz
T_{Astart}(1)	Start-up time	38K 32K	93.80 111.31	101.63 115.65	105.49 118.98	μs
I_{ACLK}	Current consumption	38K 32K	0.14 0.13	0.38 0.25	0.88 0.59	uA
DC_{ACLK}	Duty cycle	38K 32K	39.55 39.83	48.25 48.12	54.12 53.80	%
D_{evA}	Frequency Deviation	VDD = 2.5V~5.5V Ta = -40°C~85°C 32K	-10		10	%

Note: Data based on assessment results, not tested in production.

5.3-9 Flash characteristics

Symbol	Parameter	Condition	Min	Type	Max	Unit
EC_{flash}	Sector Endurance		20k			cycles
RET_{flash}	Data Retention		20			Years
T_{prog}	Byte/Half Word/Word Program Time			65	86	μs
$T_{Sector-erase}$	Sector Erase Time			3	3.7	ms
$T_{Chip-erase}$	Chip Erase Time			29	39	ms

5.3-10 Electromagnetic Sensitivity Characterization

5.3-10.1 ESD Characteristics

Symbol	Parameter	Condition	Min	Type	Max	Unit
$V_{ESD, HBM}$	ESD @ Human Body Mode		5			KV
$V_{ESD, CDM}$	ESD @ Charge Device Mode		1			KV
$V_{ESD, MM}$	ESD @ Machine Mode		400			V
$I_{Latchup}$	Latch up current		200			mA

5.3-10.2 Static Latch-Up

Two complementary static tests are required on 3 parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin。

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Symbol	Parameter	Condition	Type
LU	Static latch-up class	TA = +25 °C conforming to JESD78A	Class I Leve

5.3-11 I/O Port Characteristics

5.3-11.1 Output Characteristics - Port PA,PB,PC,PD

Symbol	Parameter	Condition	Min	Max	Unit
V_{OH}	High level Output voltage Source Current	Sourcing 4 mA, VDD = 3.3 V (see Note 1)	VDD-0.2		V
		Sourcing 6 mA, VDD = 3.3 V (see Note 2)	VDD-0.3		
V_{OL}	Low level output voltage Sink Current	Sinking 4 mA, VDD = 3.3 V (see Note 1)		VSS+0.2	V
		Sinking 6 mA, VDD = 3.3 V (see Note 2)		VSS+0.3	
V_{OHD}	High level output voltage Double Source Curre	Sourcing 8 mA, VDD = 3.3 V (see Note 1)	VDD-0.2		V
		Sourcing 12 mA, VDD = 3.3 V (see Note 2)	VDD-0.3		
V_{OLD}	Low level output voltage Double Sink Current	Sinking 8 mA, VDD = 3.3 V (see Note 1)		VSS+0.2	V
		Sinking 12 mA, VDD = 3.3 V (see Note 2)		VSS+0.3	

Note:

1. Single output PIN maximum current is 12mA, IVDD Max = 80mA, IVSS Max = 100mA.
2. Derived from a comprehensive assessment and not tested in production.

5.3-11.2 Input Characteristics - Port PA,PB,PC,PD

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IT+}	Positive-going input threshold voltage	VDD=2.5	1.4			V
		VDD=3.3	1.8			V
		VDD=5.5	3			V
V_{IT-}	Negative-going input threshold voltage	VDD=2.5			0.9	V
		VDD=3.3			1.3	V
		VDD=5.5			2.4	V
V_{hys}	Input voltage hysteresis (VIT+ - VIT-)	VDD=2.5		0.5		V
		VDD=3.3		0.5		V
		VDD=5.5		0.6		V
$R_{pullhigh}$	Pullup Resistor	Pullup enable	40	50	60	Kohm
$R_{pulldown}$	Pulldown Resistor	Pulldown enable	60	80	100	Kohm
C_{input}	Input Capacitance			5		pf

Note: Derived from a comprehensive assessment and not tested in production.

5.3-11.3 Port Leakage Characteristics - Port PA,PB,PC,PD

Symbol	Parameter	Condition	Min	Max	Unit
I_{lkg}	Leakage current	See Note 1, 2	2.5V / 3.6V	±50	nA

Notes.

1. The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.
3. Derived from a comprehensive assessment and not tested in production.

5.3-11.4 Port External Input Sampling Requirements - Timer Gate/Timer Clock

Symbol	Parameter	Condition	Min	Max	Unit
T(int)	External interrupt timing	External trigger signal for the interrupt flag(see Note 1)	255		ns
T(cap)	Timer Captuter timing	TIM1/TIM2 capture pulse width Fsystme =4MHz	25		μs
f_{EXT}	Timer clock frequency applied to pin	TIM1,TIM2,TIM10,TIM11 external clock input Fsystme =4MHz	0	$f_{TIMxCLK}/4$	MHz
T(PCA)	PCA clock frequency applied to pin	PCA external clock input Fsystme =4MHz	0	$f_{PCACLK}/4$	MHz

Note.

1. The external signal sets the interrupt flag every time the minimum t(int) parameters are met. It may be set even with trigger signals shorter than t(int).
2. Derived from a comprehensive assessment and not tested in production.

5.3-12 ADC Characterization

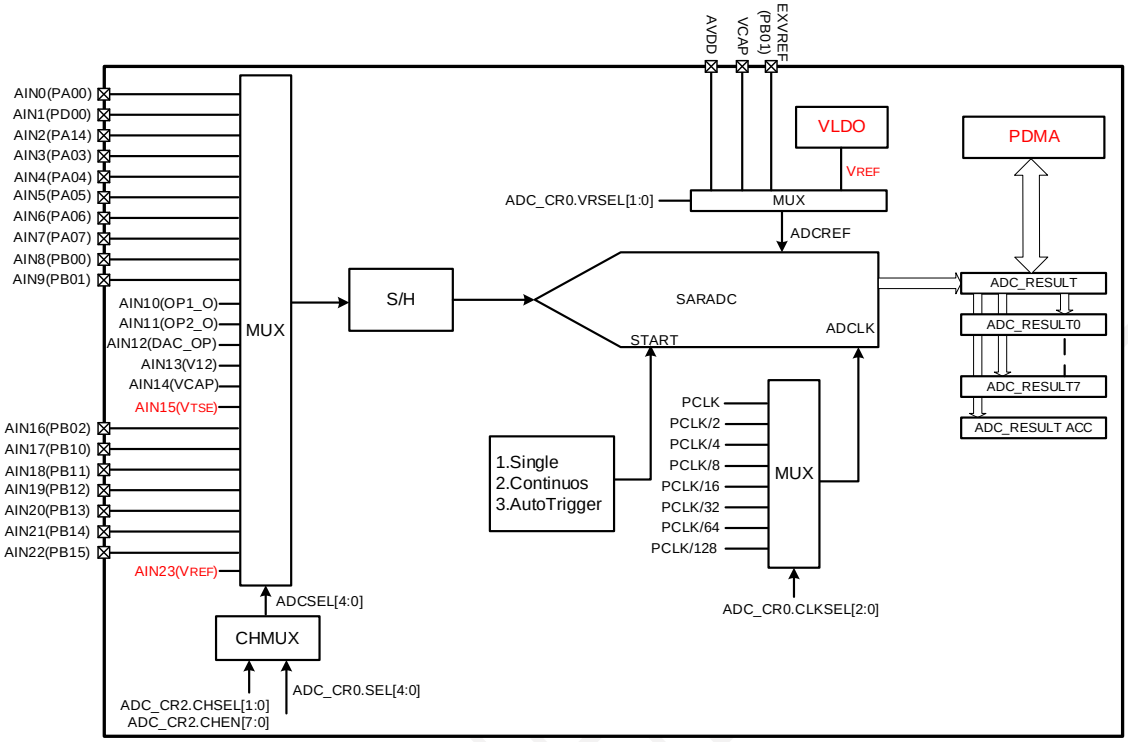


Figure 7 ADC Block Diagram

Symbol	Parameter	Condition	Min	Type	Max	Unit
VDDA	Supply Voltage		2.5		5.5	V
V_{ADCIN}	Input voltage range	Single ended	0		VREF	V
V_{REF}	ADC Reference Voltage			VDDA		V
		VCAP		2.55		V
				2.048		V
fs	ADC Sample Rate	@VDD>2.5V		1		MHz
I_{ADC}	ADC Power Consumption	@fs=1Mhz	0.7	0.9	1.2	mA
C_{ADC}	ADC input capacitance			16	18.4	pF
R_{ADC}	ADC Sampling switch			0.6		kΩ
F_{ADCCLK}	ADC clock Frequency		0.5	4	24	MHz
$T_{ADCSTART}$	Startup time of ADC bias		2	3	4	μs

Symbol	Parameter	Condition	Min	Type	Max	Unit
$T_{ADCCONV}$	Conversion time			16	20	cycles
ENOB			9.5	10	10.4	Bit
DNL	Differential non-linearity	uncalibrated VREF=VDD		±1	3	LSB
INL	Integral non-linearity		-7	±1	7	LSB
E_o	Offset error		-6	±1	6	LSB
E_g	Gain error		-6	±1	6	LSB
DNL	Differential non-linearity	Calibrated VREF=VDD	-1	±1	3	LSB
INL	Integral non-linearity		-5	±1	5	LSB
E_o	Offset error		-2	±1	2	LSB
E_g	Gain error		-4	±1	4	LSB
DNL	Differential non-linearity	uncalibrated VREF=2.048V	-1		23	LSB
INL	Integral non-linearity		-54			LSB
E_o	Offset error		-54			LSB
E_g	Gain error				14	LSB
DNL	Differential non-linearity	Calibrated VREF=2.048V	-1		12	LSB
INL	Integral non-linearity		-10		19	LSB
E_o	Offset error			0		LSB
E_g	Gain error		-6			LSB

Note: Guaranteed by design, not tested in production

5.3-12.1 ADC Input Impedance

Typeical ADC connection diagram as below.

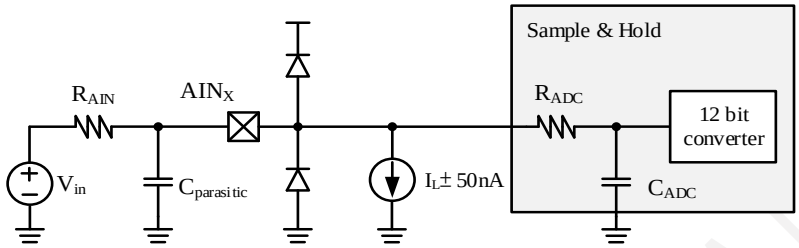


Figure 8 Typeical ADC Application Diagram

1. $C_{parasitic}$ is the capacitance on the PCB, and its capacitance value size depends on the PCB line configuration (about 7pF). If the capacitance is too large, the ADC accuracy will be reduced or the ADC clock frequency will need to be reduced to maintain ADC accuracy.
2. The maximum R_{AIN} value in Table (B) is obtained by referring to C_{ADC} and R_{ADC} in the ADC specification table and Figure 8.

Table (B). RAIN corresponds to fADCCLK

t_S (μs)	f_{ADCCLK}(Hz)	*SAM*	R_{AIN} (kΩ)
0.167	24M	4	0.05
0.333	12M	4	0.5
0.667	6M	4	2.0
2.67	3M	8	10
5.33	1.5M	8	20
10.7	0.75M	8	40
21.3	0.375M	8	50

5.3-13 VC Characteristics

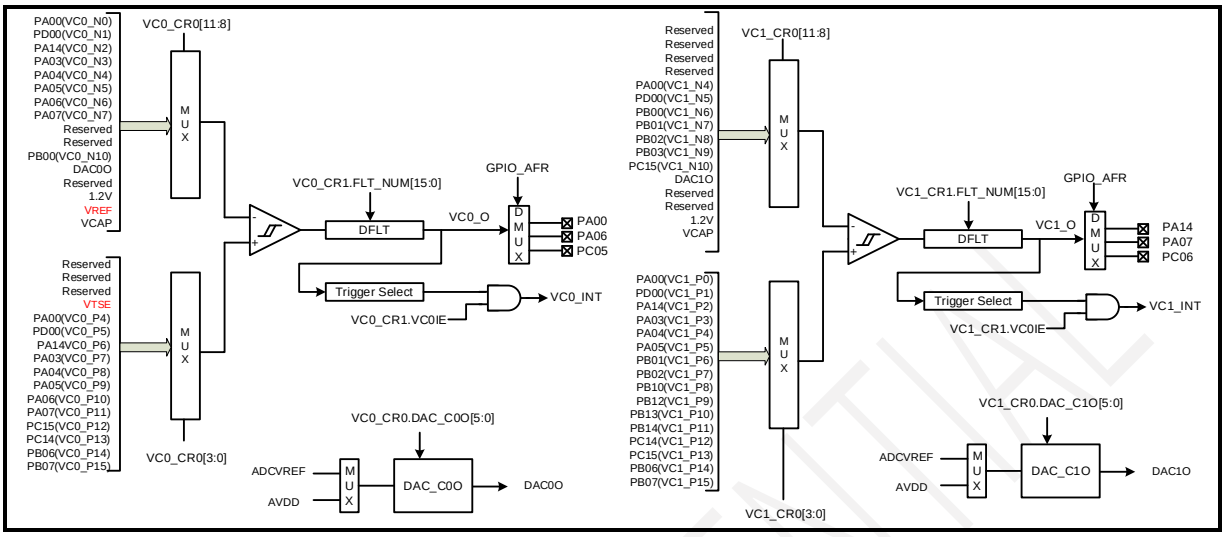


Figure 9 VC Block Diagram

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{in}	Input voltage range		0		5.5	V
V_{incom}	Input common mode range		0		5.5	V
V_{offse}	Input offset	@25°C		±10		mV
I_{comp}	Comparator's current		8.26	9.473	11.1	μA
Tresponse	Comparator's response		40ns	150ns	280ns	ns

Note: Data based on assessment results, not tested in production

5.3-14 DAC Characteristics

Symbol	Parameter	Condition	Min	Type	Max	Unit
VDDA	Analog supply voltage	-	2.5	3.3	5.5	V
DNL	Differential non-linearity (deviation between two consecutive codes - 1LSB)	-	-	±1-		LSB
INL	ntegral non-linearity (Deviation between the value measured at code 1 and the line between code 0 and code 1023)			±1		LSB
Offset	Offset error (Difference between the measured value at code (0x80) and the ideal value VDDA/2)	-	-	±2-		LSB
$T_{SETTLING}$	Settling time (Full scale: for 8-bit input code conversion between the lowest and highest input codes until DA0/DA1 reaches its final value of ±4LSB)	CLOAD ≤ 50pF RLOAD ≥ 5kΩ	-	-	8	μs

5.3-15 OPA Characteristics

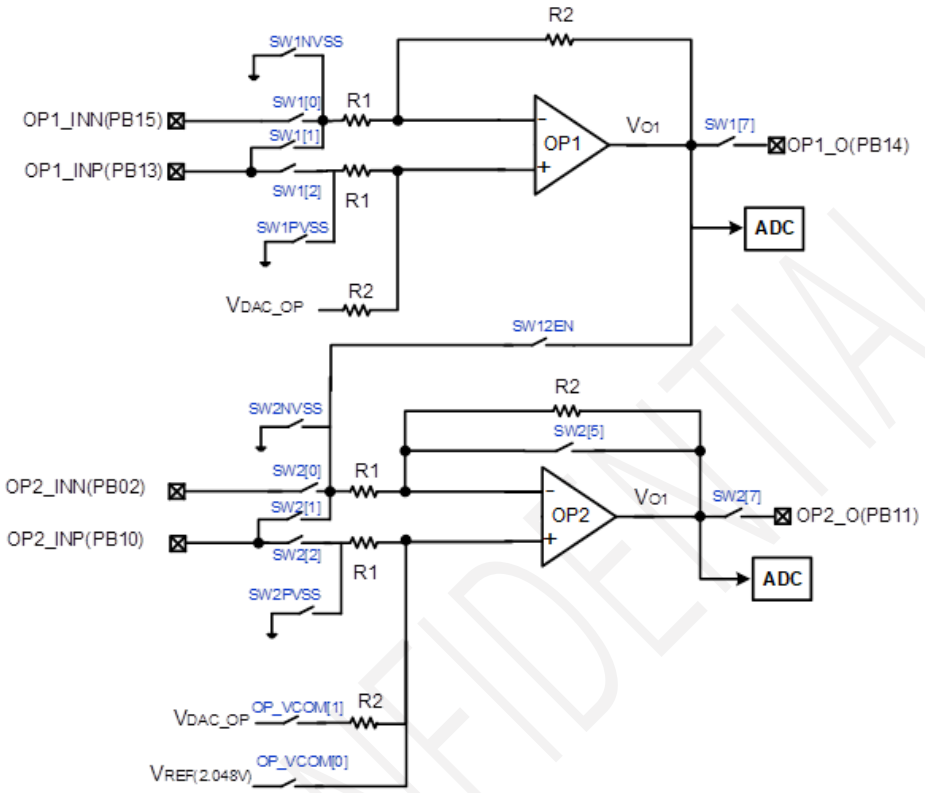


Figure 10 OPA Block Diagram

$V_{OP1\_O} = V_{DACO} + (V_{OP1\_INP} - V_{OP1\_INN}) * GAIN1$ GAIN1=R2/R1=16 (As SW1[0], SW1[2] on)

$V_{OP2\_O} = V_{DACO} + (V_{OP1\_INP} - V_{OP1\_INN}) * GAIN2$ GAIN2=R2/R1=16 (As SW1[0], SW1[2] on)

OPA: (AVDD=2.5V ~ 5.5 V, AVSS=0 V, Ta=- 40°C ~ +85°C)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{DDA}	Analog supply voltage		2.5		5.5	V
CMIR	Common mode input range	Except differential mode	0		VDDA	V
		Differential mode	-0.2		VDDA	V
Vio	Input offset voltage (follower mode)	OPA1	-4		4	mV
		OPA2	-4		4	mV
△Vio	Input offset voltage drift	-40~85°C	-6	--	26	μV/°C
I_{LOAD}	Drive current				50	μA
IOP	Operating current	VDDA=5V	0.86	0.88	0.89	mA
CMRR	Common mode rejection ratio	0.2<V_{CM} <VDDA-0.2 25°C		57.5		dB
PSRR	Power supply rejection ratio	0.2<V_{CM} <VDDA-0.2 25°C		59.4		dB
Rin	Input Resistive (Differential gain)			20		kΩ
R_{LOAD}	Resistive load		100			kΩ
C_{LOAD}	Capacitive load				40	pF
VOH_{SAT}	High saturation voltage	R_{LOAD} =Min. Input at V_{DDA}	V_{DDA} -0.1			V
VOL_{SAT}	Low saturation voltage	R_{LOAD} =Min. Input at 0V			0.1	V
PGA gain	Unit gain	Gain=1 @25°C	0.99	1	1.01	
	Non-inverting gain	Gain=17 @25°C		17		
	Inverting gain	Gain=-16 @25°C		-16		
	Differential gain (VDAC_OP=1/2VDD)	Gain=16 @25°C		16		
	OP1 and OP2 shunt (VDAC_OP=1/2VDD)	Gain=16 @25°C		256		
Gain error	PGA gain error	@25°C	--	1	--	%
PGA BW	PGA bandwidth	Gain=1		700		

Symbol	Parameter	Condition	Min	Type	Max	Unit
	(Unit gain)	C_{LOAD} =10pF@25°C				
	PGA bandwidth (Non-inverting gain)	Gain=17 C_{LOAD} =10pF@25°C		1000		
	PGA bandwidth (Inverting gain)	Gain=-16 C_{LOAD} =10pF@25°C		1000		
	PGA bandwidth (Differential gain)	Gain=16 C_{LOAD} =10pF@25°C		1000		

5.3-16 TIM Timer Features

Symbol	Parameter	Condition	Min	Max	Unit
$T_{(int)}$	External interrupt timing	External trigger signal for the interrupt flag (see Note 1)	251		ns
$T_{(cap)}$	Timer Captuter timing	TIM1/TIM2 capture pulse width Fsystme = 4MHz	24.97		μs
f_{EXT}	Timer clock frequency applied to pin	TIM1,TIM2,TIM10,TIM11 external clock input Fsystme =4MHz	0	$F_{TIMxCLK}$/4	MHz
$T_{(PCA)}$	PCA clock frequency applied to pin	PCA external clock input Fsystme = 4MHz	0	F_{PCACLK}/4	MHz

Note.

1. The external signal sets the interrupt flag every time the minimum t(int) parameters are met. It may be set even with trigger signals shorter than t(int).
2. Derived from a comprehensive assessment and not tested in production.

5.3-17 Communications interface

5.3-17.1 I2C characteristics

Symbol	Parameter	Standard mode (100K)		Fast mode (400K)		High speed mode (1M)		Unit
		Min	Max	Min	Max	Min	Max	
tSCLL	SCL clock low time	5		1.25		0.5	5	us
tSCLH	SCL clock high time	5		1.25		0.5	5	us
tSU.SDA	SDA data setup time	12.08		6.74		159		ns
tHD.SDA	SDA data hold time	22.5		14.4		27.6		ns
tHD.STA	START condition hold time	275		262		20		ns
tSU.STA	Repeated START condition setup time	14.8		4.22		4.63		ns
tSU.STO	STOP condition setup time	2.26		0.377		0.17		us
tBUF	Bus idle time (STOP to START)	7.38		3.42		3.44		us

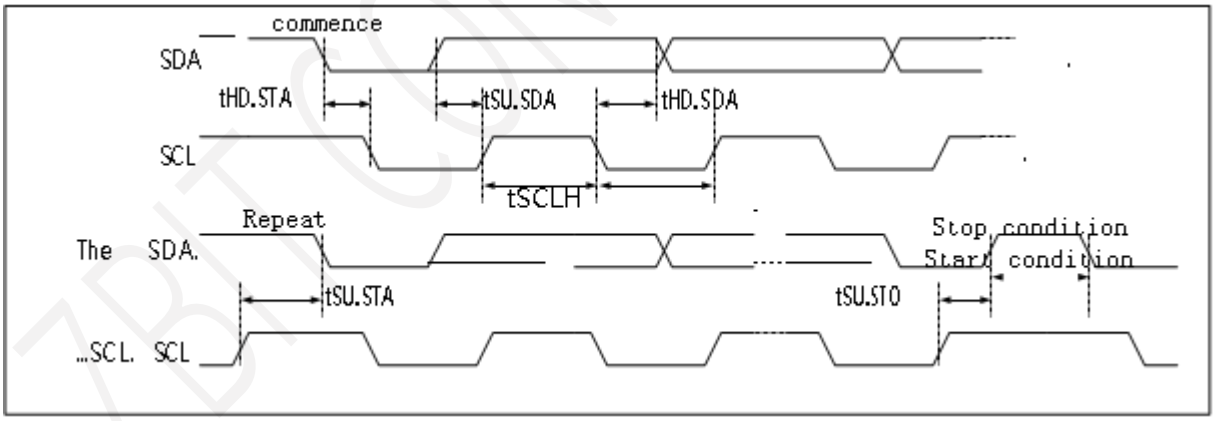


Figure 11 I2C Timing Block Diagram

5.3-17.2 SPI characteristics

Symbol	Parameter	Condition	Min	Max	Unit
tc(SCK)	SCK clock period (frequency)	Master	4*pclk		ns
		Slave	5.3*pclk		ns
tw(SCKH)	SCK clock High period	Master	31		ns
		Slave	42		ns
tw(SCKL)	SCK clock Low period	Master	30		ns
		Slave	41		ns
tsu(SSN)	SEL enable setup time	Slave	2.5		ns
th(SSN)	SEL enable hold time	Slave	90		ns
tv(MO)	Master output data valid Time			5	ns
th(MO)	Master output data hold Time		0		ns
tv(SO)	Slave output data valid Time			32	ns
th(SO)	Slave output data hold Time		30		ns
tsu(MI)	Master Data input setup time		30		ns
th(MI)	Master Data input hold time		25		ns
tsu(SI)	Slave Data input setup time		15+0.5*pclk		ns
th(SI)	Slave Data input hold time		20+1.5*pclk		ns

Note : Guaranteed by design, not tested in production

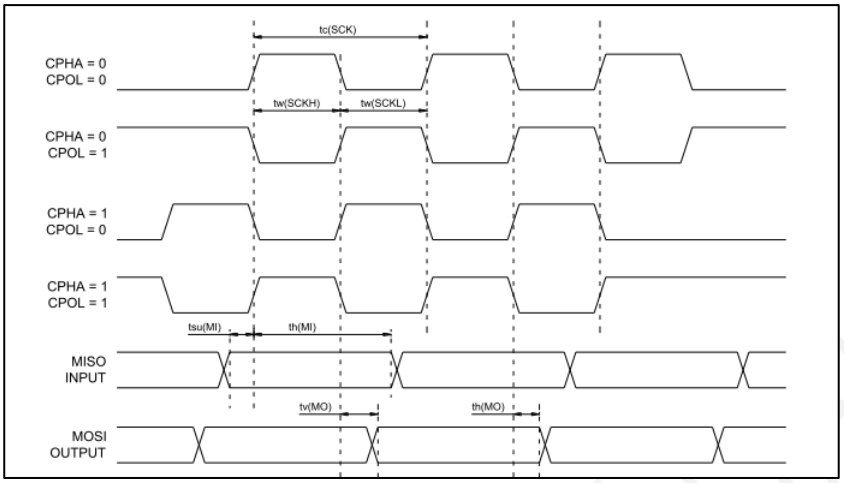


Figure 12 SPI Timing Diagram (Master Mode)

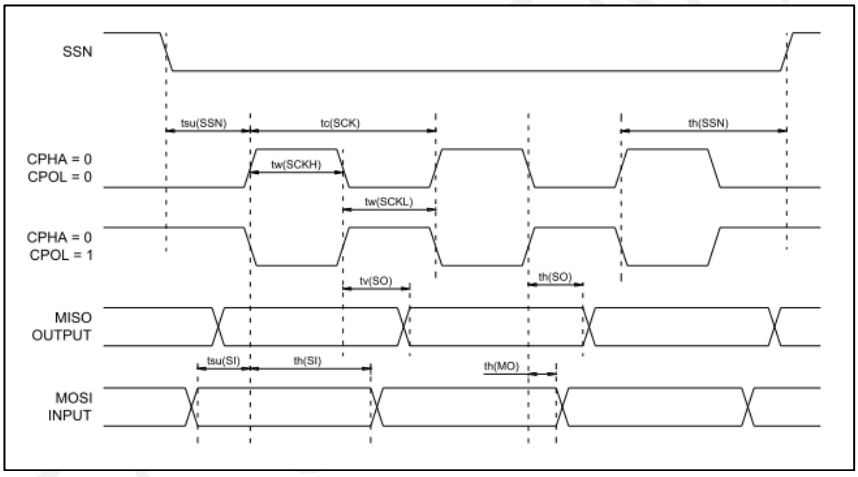


Figure 13 SPI Timing Diagram (Slave Mode CPHA=0)

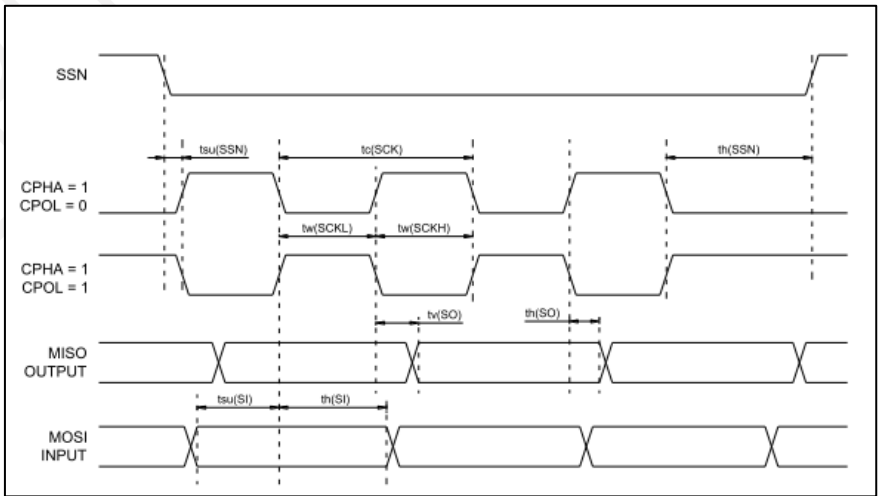


Figure 14 SPI Timing Diagram (Slave Mode CPHA=1)

5.3-17.3 I2S Interface characteristics

Symbol	Parameter	Condition	Min	Type	Max	Unit
DuCy(SCK)	Clock duty cycle	Slave	30		70	%
fCK 1/tc(CK)	Clock frequency	Master (sample size 16bit, sampling rate 48KHz)	1.522		1.525	MHz
		Slave	0		6.5	
tr(CK) tf(CK)	Clock rising and falling time	Capacitive load：C=30pF			8	nS
tv(WS)	WS valid time	Master	1.2			
th(WS)	WS hold time	Master I2S2	0.2			
$tsu_{(WS)}$	WS Establishment time	Slave	1.48			
tsu(WS)	WS setup time	Slave	0 .06			
th(WS)	WS hold time	Master Fpclk=16MHz, sampling rate 48KHz)	329			
tw(CKH)	Clock High/Low period		328			
tw(CKL)	Data Entry Establishment Time	Master Receiver I2S2	14			
tsu(SD_MR)	Data input setup time	Slave	5.3			
$th_{(SD\_MR)}$	Data input validity time	Master	12.8			
tsu(SD_SR)	Data input setup time	Slave	0.6			
th(SD_MR)	Data input hold time	Slave (Enabled)			18	
th(SD_SR)	Data input hold time	Slave (Enabled)	11			
tv(SD_ST)	Data output valid time	Master (Enabled)			3	
th(SD_ST)	Data output hold time	Master (Enabled)	0.18			

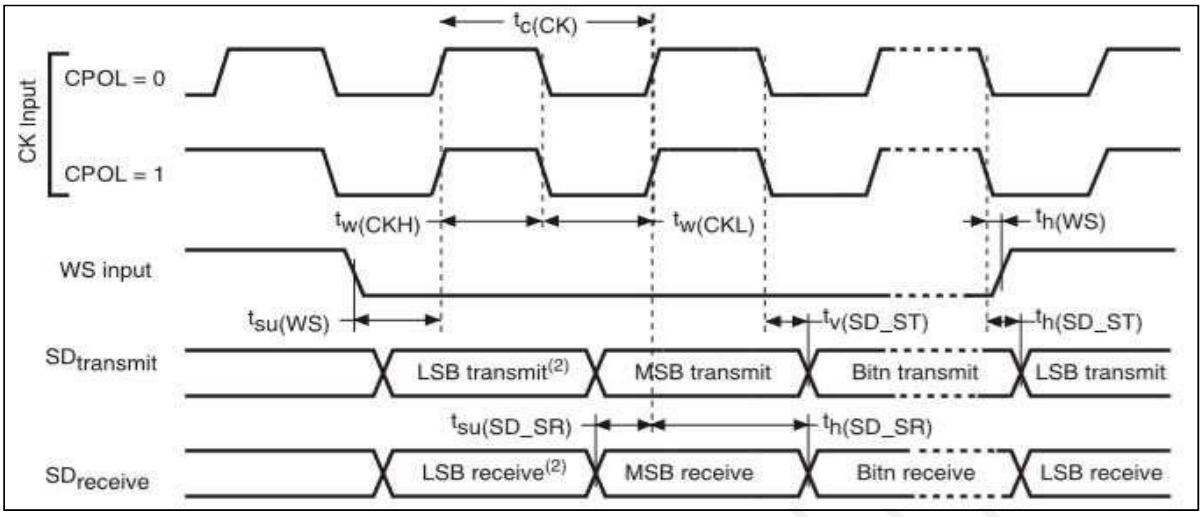


Figure 15 I2S slave timing diagram

Note 1. Measurement point: low level 0.3 × VDD, high level 0.7 × VDD.

Note 2. LSB send/receive previously sent bytes. No LSB send/receive was sent before the first byte was sent.

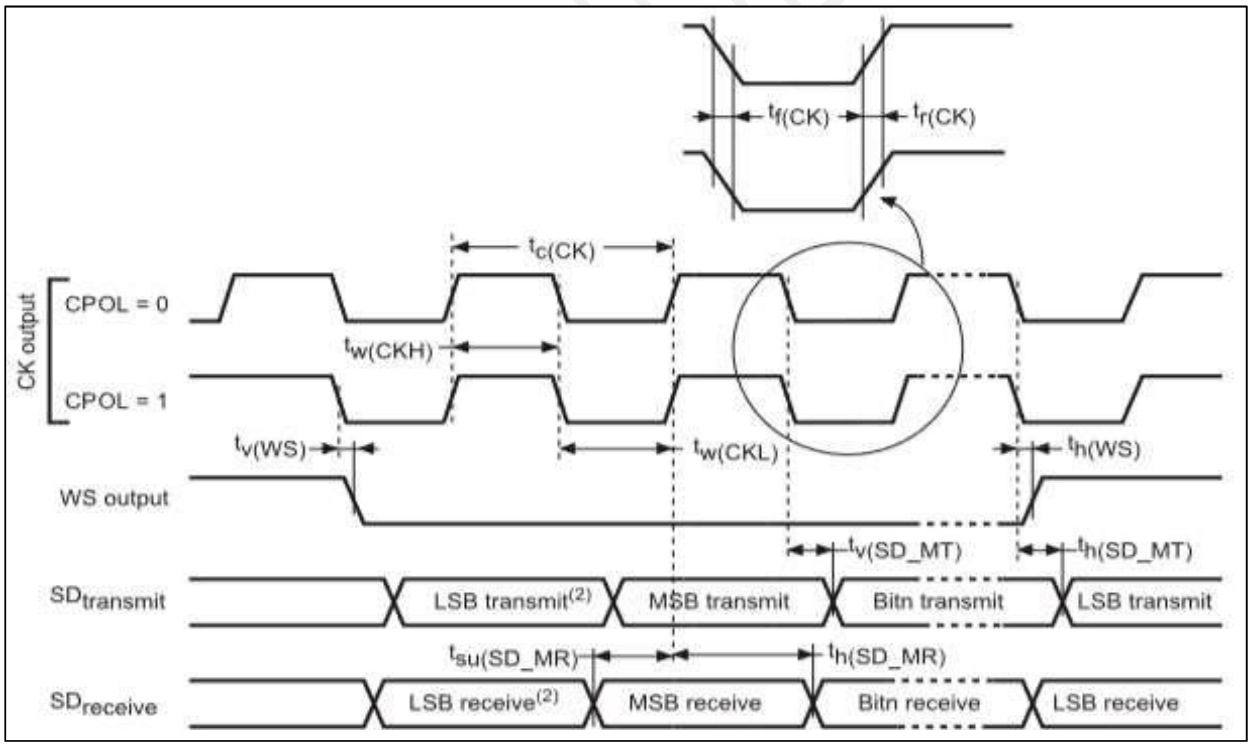


Figure 16 I2S Main Timing Diagram

Note 1. LSB send/receive the previously sent byte. No LSB send/receive is sent before the first byte is sent.

5.3-18 Temperature Sensor Characteristics

Symbol	Parameter	Min	Type	Max	Unit
$TL^{(*1)}$	VSENSE Linearity with respect to temperature	-5		+5	°C
$SP_{AVG}^{(*1)}$	Average slope	3	4	5	mV/°C
Io	Voltage at 25°C (±5°C)	1.156	1.253	1.351	V
T_{START}	Startup time	4			us
T_{S_temp}	ADC sampling time when reading temperature	5			us

Note.

(1*) : Guaranteed by design, not tested in production.

Calculate the actual temperature using the following formula.

$$\text{Temperature}(℃) = \frac{V_{25} - V_{TS}}{\text{Avg\_Slope}} + 25$$

Note:

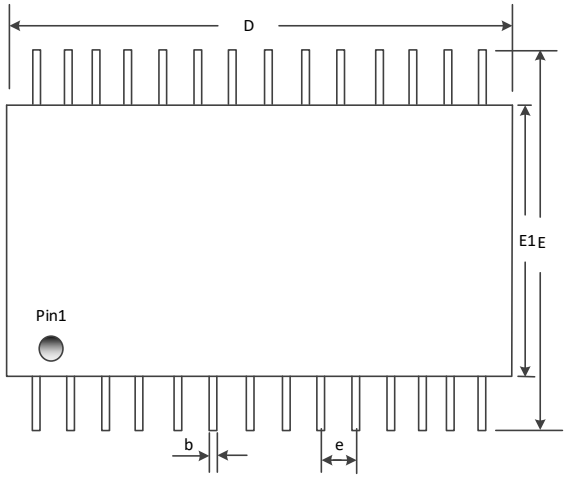
$V_{25} = V_{TS}$ is a temperature value of 25°C

Avg_Slope is the average slope of the temperature sensor

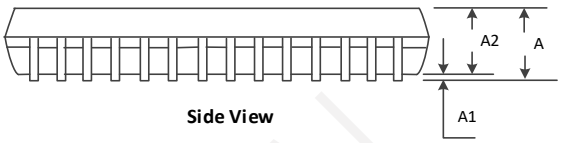
Temperature sensor calibration value Name	Description	Stored address
TS_CAL	VTS ADC raw data acquired at temperature of 25° C, VDD=3.3V	0x1800_0034~0x1800_0035

【6】 Package Characteristics

6.1 TSSOP28 Package



Top View



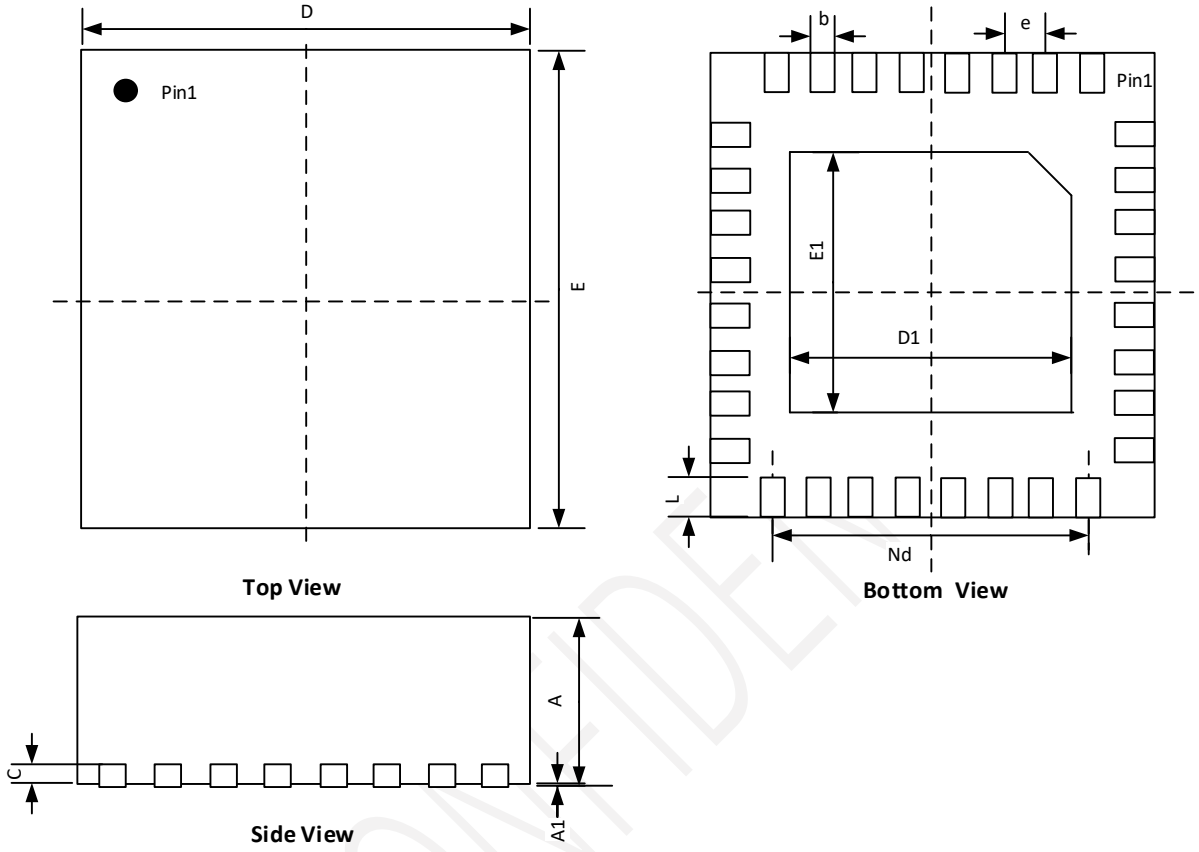
Side View

Bottom View

Dimensions

SYMBOL	MILIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
A3	0.39	0.44	0.49	0.015	0.017	0.019
b	0.18	--	0.30	0.007	--	0.012
c	0.14	--	0.18	0.006	--	0.007
D	9.60	9.70	9.80	0.378	0.382	0.386
E1	4.30	4.40	4.50	0.169	0.173	0.177
E	6.20	6.40	6.60	0.244	0.252	0.260
e		0.65BSC			0.026BSC	
L	0.45	--	0.75	0.018	--	0.030
L1		1.00REF			0.039REF	
θ	0	--	8°	0.000	--	8°

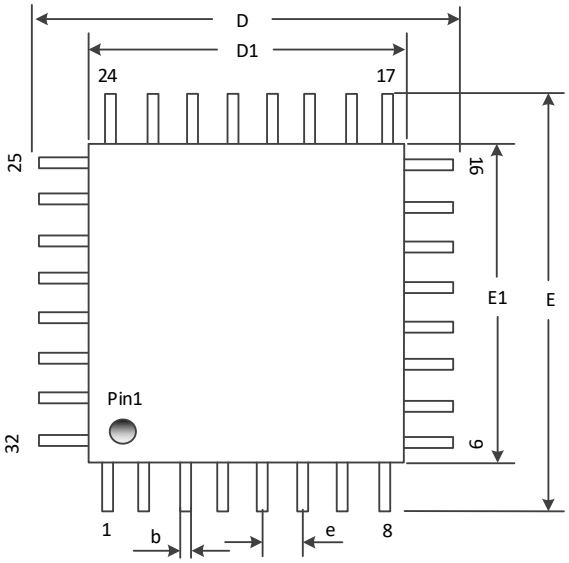
6.2 QFN32 Package



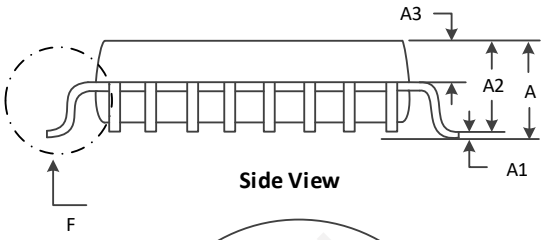
Dimensions

SYMBOL	MILIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0	0.02	0.05	0	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
c	0.18	0.20	0.25	0.007	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	3.55	3.65	3.75	0.140	0.144	0.148
e	0.50REF			0.02REF		
Nd	3.50REF			0.138REF		
E	4.90	5.00	5.10	0.193	0.197	0.201
E1	3.55	3.65	3.75	0.140	0.144	0.148
L	0.30	0.38	0.45	0.012	0.015	0.018

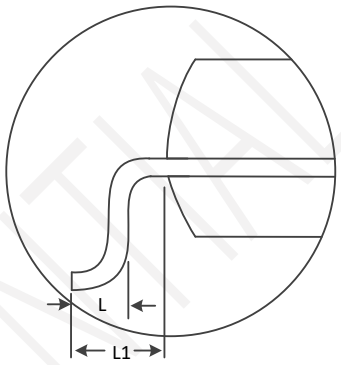
6.3 LQFP32 Package



Top View



Side View

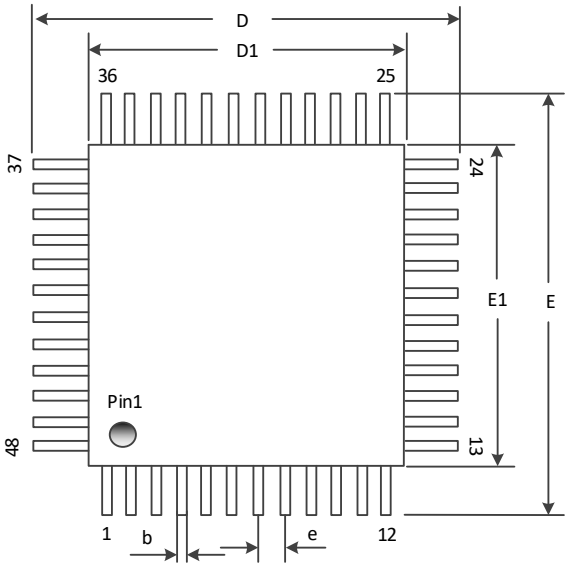


Detail F

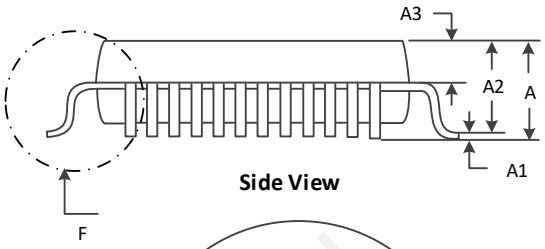
Dimensions

SYMBOL	MILIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	——	——	1.60	——	——	0.063
A1	0.05	——	0.15	0.002	——	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
A3	0.59	0.64	0.69	0.023	0.025	0.027
b	0.31	——	0.43	0.012	——	0.017
D	8.80	9.00	9.20	0.346	0.354	0.362
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.80	9.00	9.20	0.346	0.354	0.362
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.80 BSC			0.0315 BSC		
L	0.45	——	0.75	0.018	——	0.030
L1	1.00 REF			0.039 REF		
θ	0.00	——	7°	0	——	7°

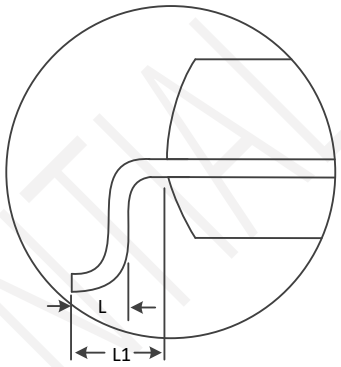
6.4 LQFP48 Package



Top View



Side View



Detail F

Dimensions

SYMBOL	MILIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	——	——	1.60	——	——	0.063
A1	0.05	——	0.15	0.002	——	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
A3	0.59	0.64	0.69	0.023	0.025	0.027
b	0.17	——	0.27	0.007	——	0.011
D	8.80	9.00	9.20	0.346	0.354	0.362
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.80	9.00	9.20	0.346	0.354	0.362
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.50 BSC				0.020 BSC	
L	0.45	——	0.75	0.018	——	0.030
L1	1.00 REF			0.039 REF		
θ	0.00	——	7°	0	——	7°

6.5 Screen Printing Instructions

6.5-1TSSOP28

1. First line: The first 10 positions of the product model + trademark, refer to Chapter 7 Model Naming for details.
2. Second line: The first 6/7 digits represent the Lot ID and the last digit represents the Revision of the product (Revision).
3. Third line: The first 4 digits represent the year and week of production, the fifth digit represents the Packaging and testing facility.

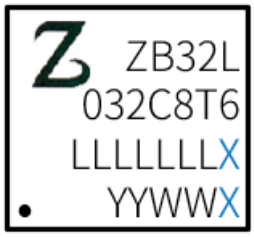
6.5-2 QFN32

1. First line: The 5th to 10th digits of the product model number + trademark, refer to Chapter 7 Model Naming for details.
2. Second line: The first 6/7 digits represent the Lot ID and the last digit represents the Revision of the product (Revision).
3. Third line: The first 4 digits represent the year and week of production, the fifth digit represents the Packaging and testing facility.

6.5-3 LQFP32

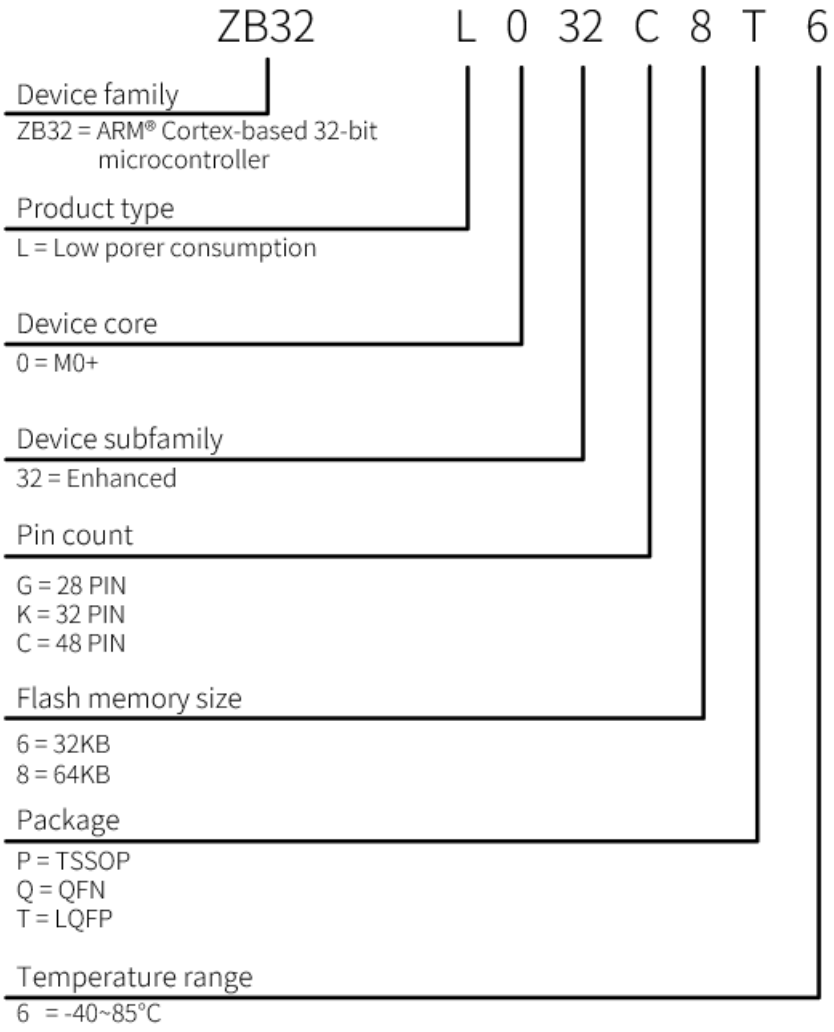
1. First line: The first 5 positions of the product model + trademark.
2. The second line: the 6th to 12th digits of the product model number, refer to Chapter 7 Model Naming for details.
3. Third line: the first 6/7 digits represent the Lot ID, and the last digit represents the version of the product (Revision).
4. Fourth line: the first four digits represent the year and week of production, the fifth digit represents the packaging and testing facility.

6.5-4 LQFP48



1. First line: The first 5 positions of the product model + trademark.
2. The second line: the 6th to 12th digits of the product model number, refer to Chapter 7 Model Naming for details.
3. Third line: the first 6/7 digits represent the Lot ID, and the last digit represents the version of the product (Revision).
4. Fourth line: the first four digits represent the year and week of production, the fifth digit represents the packaging and testing facility.

【7】 Product Naming Rule



【8】 Product Selection Table

Model	Flash (KB)	SRAM (KB)	Package	Wrap	MPQ	MOQ
ZB32L032G8P6T	64	16	TSSOP28	Tape & Reel	9000	72000
ZB32L032K8Q6T	64	16	QFN32	Tape & Reel	5000	40,000
ZB32L032K8T6R	64	16	LQFP32	Tray	2500	15000
ZB32L032C8T6R	64	16	LQFP48	Tray	2500	15000

【9】 Revision History

Version	Date.	Description
V1.0	2023-1206	Initial Release
V1.01	2024-0108	(1) Updated "7 - Product Naming Rule" (2) Updated "2.4 - Pin configuration"