ZB32L003

ARM® Cortex®-M0+ 32 bits

Micro-Controller

Datasheet

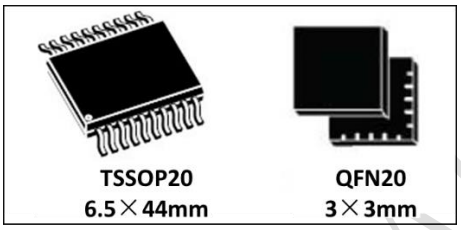
Version 1.0

2024/1/10

ZB32L003

ARM® Cortex®-M0+ 32-bit MCU, up to 64 KB Flash, 4 KB SRAM, 2.5-5.5V, TSSOP-20/QFN-20

Datasheet - production data



- **Core**
  - The ARM cortex-m0+core runs up to 24MHz.
  - A 24-bit system timer
  - Support low power sleep mode
  - Single-cycle 32-bit hardware multiplier
- **Internal Storage**
  - 64K byte embedded Flash with write protection function.
  - 4K byte SRAM
- **Clock and power supply**
  - 4 selectable clock sources
    - External 4MHz~24MHz high-speed crystal oscillator
    - External 32.768KHz crystal oscillator
    - Internal 4MHz~24MHz high-speed clock
    - Internal low-speed 38.4KHz/32.768KHz clock
    - Support hardware clock monitoring
  - Power management
    - Two low-power working modes: Sleep and Deep Sleep Mode.
    - Low voltage detection, which can be configured as interrupt or reset.
- **Suspend**
  - Nested Vector Interrupt Controller (NVIC) is used to control 32 interrupt sources, and each interrupt source can be set to 4 priorities.
  - Support serial debugging (SWD) with 2 observation points /4 breakpoints.
- **General purpose I/O pin**
  - 17 I/O in 20-Pin package
- **Communication Interface**
  - UART0-UART1 standard communication interface
  - Ultra-low power UART supporting low-speed clock
  - SPI standard communication interface, up to 8Mbps.
  - I2C standard communication interface, the master mode supports up to 1Mbps, and the slave mode supports up to 800Kbps.
  - One-Wire communication interface
- **Buzzer frequency generator**
  - Generate a 1KHz, 2KHz, 4KHz buzzer signal.
- **Timer/counter**
  - 1x16-bit advanced control timer: it has 4 channels of PWM output/input capture, supports 3 complementary outputs, and has the functions of dead zone generation and emergency stop.
  - 1x16-bit General-purpose timer, supporting 4 channels of comparison output/input capture, PWM output.
  - 1x16-bit programmable timer array, supporting 5 input capture/comparison output, PWM output.
  - 2x16/32bit basic timer/counter
  - 1x16-bit low power timer
  - Automatic wake-up timer
  - System window watchdog and independent watchdog timer
- **RTC**
  - Support RTC counting (seconds/minutes/hours) and perpetual calendar function (day/month/year)
  - Register supporting alarm function (seconds/minutes/hours/days/months/years)
  - Support RTC to wake up the system from Deep Sleep mode.
- **ADC**
  - 7-channel 12-bit 1Msps sampling rate, 12-bit SAR ADC
- **Voltage comparator (VC)/low voltage detector (LVD)**
- **Hardware CRC-16 module**
- **Working Conditions**
  - Wide voltage working range 2.5V to 5.5v.
  - Wide working frequency up to 24MHz
  - Operating temperature: -40 C to+85 C.
- **16-byte chip unique ID (UID)**
- **Development tools**
  - Full-featured embedded debugging solution
  - In-system programming (ISP programming) scheme
- **Packaging form: TSSOP20, QFN20.**

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【1】 Brief Introduction

ZB32L003 is a microcontroller with ultra-low power consumption, Low Pin Count and wide voltage working range (2.5V～5.5V) embedded with 32-bit ARM Cortex-M0+core. It can run at 24MHz at the highest, with embedded Flash of 64K bytes and SRAM of 4K bytes. It integrates 12-bit 1Msps high-precision SAR ADC, RTC, comparator, multi-channel UART, SPI, I2C and PWM, and has the characteristics of high integration, high anti-interference and high reliability.

ZB32L003 series has the advantages of wide voltage working range, low power consumption, low standby current, high integrated peripherals, high operating efficiency, fast wake-up and high cost performance, and is widely used in the following applications:

Small household appliances, chargers, remote controllers, electronic cigarettes, gas alarms, digital display meters, thermostats, recorders, motor drives, smart door locks, smart sensors, smart homes and smart cities.

	ZB32L003F8
Pin Number	20
GPIO	17
External Interrupt	17
Advanced-control Timer (TIM1)	1
General-purpose Timer (TIM2)	1
PCA	1
TIM10/11	2
LPTIM	1
A/D Channel Number	7
Flash(K bytes)	64
SRAM(K bytes)	4
UART/LPUART	1/1
SPI/I2C	1/1
IWDG/WWDG	1/1
1-WIRE	1
CRC16	1
Buzzer	1
AWK	1
RTC	1
LVD/VC	Support
CPU frequency	ARM® Cortex®-M0+ 24MHz (Max.)
Voltage Range	2.5～5.5V
Operating Temperature	-40～85°C
Flash Protection	Support
Package	TSSOP20、QFN20

【2】 Overview of Product Functions

In the following chapters, we will give a brief overview of the functions and basic features of ZB32L003 series products.

2.1 32-Bit Cortex-M0+Core

ARM Cortex-M0+processor is the latest generation of embedded 32-bit RISC processor, which has fewer pins and low power consumption, and can provide a low-cost platform to meet the needs of MCU implementation, while providing excellent computing performance and advanced interrupt system response. Cortex-M0+processor fully supports debuggers such as Keil and IAR, including a hardware debugging circuit and supports 2-wire SWD debugging interface.

Cortex-M0+features:

Instruction Set	Thumb / Thumb-2
Assembly Line	Two-stage pipeline
Coremark/MHz	2.46
DMIPS/MHz	0.95
Suspend	32 interrupt sources
Interrupt Priority	Configurable 4-level interrupt priority
Enhanced	Single-cycle 32-bit multiplier
Debugging Interface	Support SWD 2 line debugging interface, support 4 hard break point and 2 watch point.

2.2 Memory

2.2-1 Embedded Flash Memory (Flash)

Embedded flash memory is used to store programs and data. Built-in fully integrated Flash controller, no external high voltage input, high voltage generated by all-in circuit for programming, supporting ISP function.

- ZB32L003F8 series supports up to 64K bytes.

2.2-2 Internal SRAM

4K bytes of built-in SRAM.

2.3 Clock System

An external high-speed crystal oscillator HXT with a frequency of 4M ~ 24MHz.
An external low-speed crystal oscillator LXT with a frequency of 32.768KHz.
An internal high-speed crystal oscillator HIRC with a frequency of 4M ~ 24MHz.
An internal low-speed clock LIRC with a frequency of 32.768KHz/38.4KHz.

2.4 Working Mode

ZB32L003 supports three working modes:

1. Active: CPU runs and peripheral functional modules run.
2. Sleep: CPU mode: CPU stops running and peripheral functional modules run.
3. DeepSleep: CPU mode: CPU stops running, system master clock is turned off, and low-power functional modules run.

You can choose which working mode to run in through software. In Sleep mode, the CPU clock is turned off, other parts can still work, and the CPU can be awakened by interruption. In deep sleep mode, the main clock of the system is turned off, and most modules stop working. The system works on the built-in low-speed clock of 38.4KHz/32.768KHz, and the chip can be awakened by RTC interrupt, AWK interrupt or external interrupt. In the normal working mode, you can choose to work in frequency division mode or stop the clocks of some unnecessary modules to realize flexible switching between power consumption and performance.

2.5 Interrupt Controller (NVIC)

Cortex®-M0+processor has built-in embedded vector interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs, has four interrupt priorities, can handle complex logic, and can perform real-time control and interrupt processing.

Please refer to " ARM® Cortex®-M0+ Technical Reference Manual " and " ARM® v6-M Architecture Reference Manual " for details.

32 interrupt sources, such as Table 1 Interrupt source Shown:

Table 1 Interrupt source

External interrupt number (IRQ#)	Interrupt source	Brief introduction	Sleep Mode wake-up	Deep Sleep Mode wake-up	Vector address
0	GPIO_PA	GPIOA interrupt	Y	Y	0x0000 0040
1	GPIO_PB	GPIOB interrupt	Y	Y	0x0000 0044
2	GPIO_PC	GPIOC interrupt	Y	Y	0x0000 0048
3	GPIO_PD	GPIOD interrupt	Y	Y	0x0000 004C
4	Flash	Flash interrupt	N	N	0x0000 0050
5	NRST_input	NRST_input interrupt	Y	Y	0x0000 0054
6	UART0	UART0 interrupt	Y	N	0x0000 0058
7	UART1	UART1 interrupt	Y	N	0x0000 005C
8	LPUART	LPUART interrupt	Y	Y	0x0000 0060
9	Reserve	-	-	-	0x0000 0064
10	SPI	SPI interrupt	Y	N	0x0000 0068
11	Reserve	-	-	-	0x0000 006C
12	I2C	I2C interrupt	Y	N	0x0000 0070
13	Reserve	-	-	-	0x0000 006C
14	TIM10	TIM10 interrupt	Y	N	0x0000 0078
15	TIM11	TIM11 interrupt	Y	N	0x0000 007C
16	LPTIM	LPTIM interrupt	Y	Y	0x0000 0080
17	Reserve	-	-	-	0x0000 007C
18	TIM1	TIM1 interrupt	Y	N	0x0000 0088
19	TIM2	TIM2 interrupt	Y	N	0x0000 008C
20	Reserve	-	-	-	0x0000 0088
21	PCA	PCA interrupt	Y	N	0x0000 0094
22	WWDG	WWDG interrupt	Y	N	0x0000 0098
23	IWDG	IWDG interrupt	Y	Y	0x0000 009C
24	ADC	ADC interrupt	Y	N	0x0000 00A0
25	LVD	LVD interrupt	Y	Y	0x0000 00A4
26	VC	VC interrupt	Y	Y	0x0000 00A8
27	Reserve	-	-	-	0x0000 00A4
28	AWK	AWK interrupt	Y	Y	0x0000 00B0
29	OWIRE	1-WIRE interrupt	Y	N	0x0000 00B4
30	RTC	RTC interrupt	Y	Y	0x0000 00B8
31	CLKTRIM	CLKTRIM interrupt	Y	Ynote	0x0000 00BC

Note: You can only wake up when you select the function of internal low-speed monitoring and external low-speed clock.

2.6 Reset Controller

This product has 9 reset signal sources, each reset signal can make the CPU run again, most registers will be reset, and the program counter PC will be reset to the reset address (0x0000 0000).

Number	Interrupt source
1	Power-on/power-off reset
2	External Reset Pin reset
3	IWDG reset
4	WWDG reset
5	System software reset
6	Undervoltage (LVD) reset
7	LOCKUP reset
8	Register CPURST reset
9	Register MCURST reset

2.7 Universal IO Port (GPIO)

Up to 17 GPIO ports can be provided, some of which are multiplexed with analog ports. Each port is controlled by an independent control register bit. Support edge-triggered interrupt and level-triggered interrupt, which can wake MCU to work mode from various power consumption modes. Support Push-Pull CMOS push-pull output and Open-Drain output. Built-in pull-up resistor and pull-down resistor, with Schmidt trigger input filtering function. The output drive capability can be configured, and the maximum current drive capability can be 12mA. 17 general-purpose IO can support external asynchronous interrupt.

2.8 Timer and Watchdog

ZB32L003 product includes an advanced control timer, a general timer, a programmable counter array, two basic timers, a low-power basic timer, a system window watchdog timer, an independent watchdog timer and a system tick timer.

The following table compares the functions of advanced control timer, general timer and basic timer:

Table 2 Timer characteristic table

Timer type	Name	Counter bit width	Pre-crossover factor	Counting direction	PWM output	Capture/ compare passage	Complementary output
Advanced	TIM1	16 bits	1/2/4/8/16/64/256/1024	Increasing, decreasing, Increasing/decreasing	Yes	4	3 pairs
General	TIM2	16 bits	1/2/4/8/16/64/256/1024	Increasing, decreasing, Increasing/decreasing	Yes	4	None
Programmable counter arrays	PCA	16 bits	2/4/8/16/32	Increasing	Yes	5	None
Low power	LPTIM	16 bits	None	Increasing	None	None	None
Basis	TIM10	16/32 bit	1/2/4/8/16/32/64/128	Increasing	None	None	None
	TIM11	16/32 bit	1/2/4/8/16/32/64/128	Increasing	None	None	None

2.8-1 Advanced Control Timer (TIM1)

One advanced control timer (TIM1) can be regarded as a three-phase PWM generator assigned to six channels, which has complementary PWM outputs with dead-time insertion, and can also be regarded as a complete universal timer. Four independent channels can be used for:

- Input capture
- Output comparison
- Generate PWM (edge or center alignment mode)
- When the monopulse output is configured as a 16-bit standard timer, it has the same function as the TIMx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%).

In debug mode, the counter can be frozen and the PWM outputs are disabled, thus cutting off the switches controlled by these outputs. Many functions are the same as the general TIM timer, and the internal structure is the same, so the advanced control timer can cooperate with other TIM timers through the timer link function to provide synchronization or event link function.

2.8-2 General-purpose Timer (TIM2)

The general timer (TIM2) has a 16-bit automatic loading up/down counter, a 16-bit prescaler and four independent channels, each of which can be used for input capture, output comparison, PWM and monopulse mode output. They can also work together with the advanced control timer through the timer link function to provide synchronization or event link function. In debug mode, the counter can be frozen. Any standard timer can be used to generate PWM output.

2.8-3 Programmable Counter Array (PCA)

PCA (Programmable Counter Array) supports up to five 16-bit capture/comparison modules. The timer/counter can be used as the capture/comparison function of a general clock counter/event counter. Each channel of PCA can be independently programmed to provide input capture/output comparison or pulse width modulation.

2.8-4 Low Power Timer (LPTIM)

The low-power timer is an asynchronous 16-bit optional timer. After the system clock is turned off, it can still be clocked/counted by internal low-speed LIRC or external low-speed crystal oscillator. Interrupt can wake up the system in low power mode.

2.8-5 Basic Timer (TIM10/TIM11)

The basic timer includes two 16/32-bit optional timers TIM10/TIM11. TIM10/TIM11 have exactly the same function, they are all synchronous timers/counters, and they can choose to work in overload mode and non-overload mode. TIM10/TIM11 can count external pulses or realize system timing.

2.8-6 Independent Watchdog (IWDG)

The independent watchdog is a 20-bit down counter. It is clocked by an internal independent LIRC; Because the internal LIRC is independent of the master clock, it can work in shutdown and standby modes. It can be used as a watchdog to reset the device when something goes wrong, or as a free-running timer to provide timeout management for applications. With the option byte, it can be configured in hardware or software. In debug mode, the counter can be frozen.

2.8-7 Window Watchdog (WWDG)

The system window watchdog is based on an 8-bit down counter and supports 20-bit prescale. It is clocked by APB clock (PCLK). It can be used as a watchdog to reset the device when there is a problem in the system, and has the function of early warning interrupt, and the counter can be frozen in debugging mode.

2.8-8 Systick Timer (SYST)

This timer is dedicated to real-time operating systems, but it can also be used as a standard down counter. It has the following characteristics:

- 24-bit down counter
- Automatic overload function
- When the counter is 0, a system interrupt that can be shielded is generated.
- Programmable clock source (HCLK or HCLK/4)

2.9 Real-Time Clock (RTC)

- Support RTC counting (seconds, minutes and hours) and perpetual calendar function (day, month and year)
- Support alarm registers (seconds, minutes, hours, days, months, years)
- RTC can wake up the system from Sleep mode.

2.10 Universal Asynchronous Transceiver (UART0/UART1)

2-way universal asynchronous receiver/transmitter

2.11 Low Power Universal Asynchronous Transceiver (LPUART)

1-way asynchronous receiver/transmitter that can work in low power consumption mode.

2.12 Serial Peripheral Interface (SPI)

1-way Serial Peripheral Interface, supporting master-slave mode.

2.13 I2C Interface (I2C)

1 I2C interface, supporting master-slave mode. The serial synchronous clock enables data transmission between devices at different rates, with a maximum speed of 1Mbps for serial 8-bit bidirectional data transmission.

2.14 One-Wire Interface (OWIRE)

Support One-Wire bus protocol.

2.15 Buzzer (BEEP)

The buzzer module can generate a 1KHz, 2KHz and 4KHz buzzer signal on the BEEP pin to drive the external buzzer.

Two basic timers TIM10/TIM11 and one LPTIM can multiplex the output, providing Buzzer with programmable driving frequency.

Complementary output can be supported without additional triode.

2.16 Self-Wake Timer (AWK)

AWK is used to provide an internal wake-up time reference when MCU enters low power consumption mode. The clock of this time reference is provided by the internal low-speed RC oscillator clock (LIRC) or the pre-divided HXT crystal oscillator clock.

2.17 Clock Calibration/Monitoring Module (CLKTRIM)

Built-in clock calibration circuit can calibrate the internal RC clock through the external accurate crystal oscillator clock, and can also use the internal RC clock to check whether the external crystal oscillator clock works normally.

2.18 Unique ID (UID)

Each chip has a unique 16-byte device identification number when it leaves the factory, including wafer lot information and chip coordinate information.

ID address 0x180000F0-0x180000FF.

2.19 Cyclic Redundancy Check Calculation Unit (CRC)

It conforms to the polynomial $F(x)= X^{16}+X^{12}+X^{5}+1$ given in ISO/IEC13239.

2.20 Analog/Digital Converter (ADC)

Monotonous 12-bit successive approximation analog-to-digital converter, when working under 16MHz ADC clock, the sampling rate reaches 1Msps. The reference voltage can select the power supply voltage. 7 external channels, which can realize single, scanning and cyclic conversion. In scan/cycle mode, the conversion on a selected set of analog inputs is automatically performed.

- Input voltage range: 0 to VDD
- Conversion period: 16/20 clock cycles
- ADC sampling can be triggered from external terminals, internal TIM1, TIM2, TIM10/TIM11, VC and other modules.
- Sampling completion (EOC) interrupt

2.21 Low Voltage Detector (LVD)

Detect the chip power supply voltage or chip pin voltage. 8-step voltage monitoring value (2.5-4.4V). Asynchronous interrupt or reset can be generated according to the rising/falling edge. It has hardware hysteresis circuit and configurable software anti-shake function.

2.22 Voltage Comparator (VC)

Chip pin voltage monitoring/comparing circuit. 3 configurable positive/negative external input channels; 1 internal BGR 2.5V reference voltage. VC output can be used for timer TIM1, TIM10/TIM11, LPTimer and programmable counting array PCA for capture, gating and external counting. Asynchronous interrupt can be generated according to the rising/falling edge to wake up MCU from low power consumption mode. Software anti-shake can be configured.

2.23 Embedded Debugging System

Embedded debugging solution, providing full-featured real-time debugger, and debugging and developing software with standard mature Keil/IAR.
Support 4 hard breakpoints and multiple soft breakpoints.

2.24 Encrypted Embedded Debug Support (DBG)

Encrypted embedded debugging solution, providing full-featured real-time debugger, see the relevant chapters in the user manual for details.

【3】 System and Memory Overview

3.1 System Architecture Diagram

- Main system components:
  - Cortex-M0+
- 6 AHB bus Slave:
  - Internal SRAM
  - Internal Flash
  - AHB to APB Bridge, including all APB interface peripherals.
  - GPIO interface
  - RCC module
  - AHB interface module such as CRC.

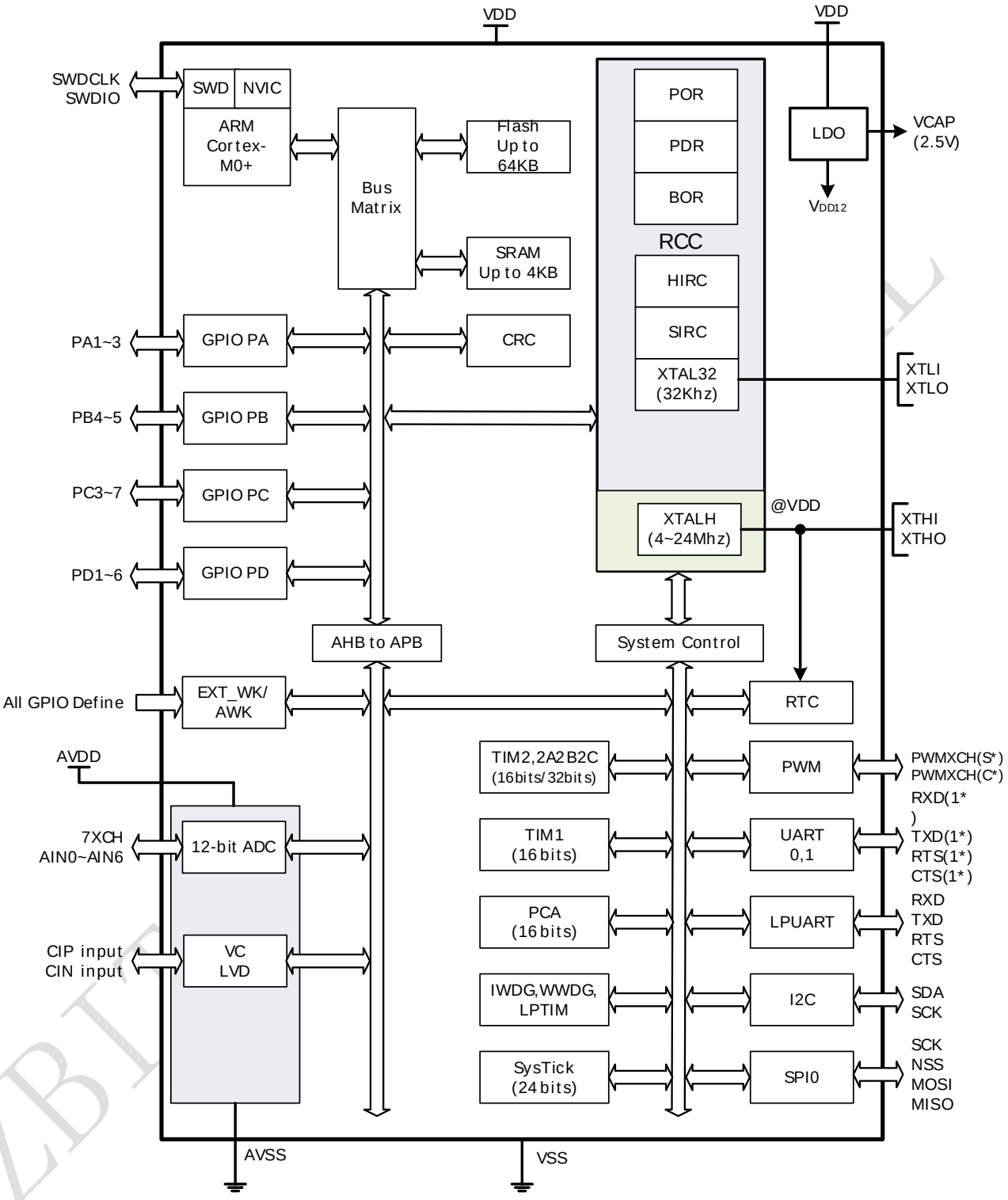


Figure 1 System Diagram

3.2 Memory Image

The total address space of the system is 4GB, including program storage space, data storage space, peripheral module registers, I/O ports, etc. The data uses the small endpoint format, that is, the high byte of data is stored in the high address of memory, and the low byte of data is stored in the low address of memory. The address space of the whole system is divided as shown below. Figure 2 Shown:

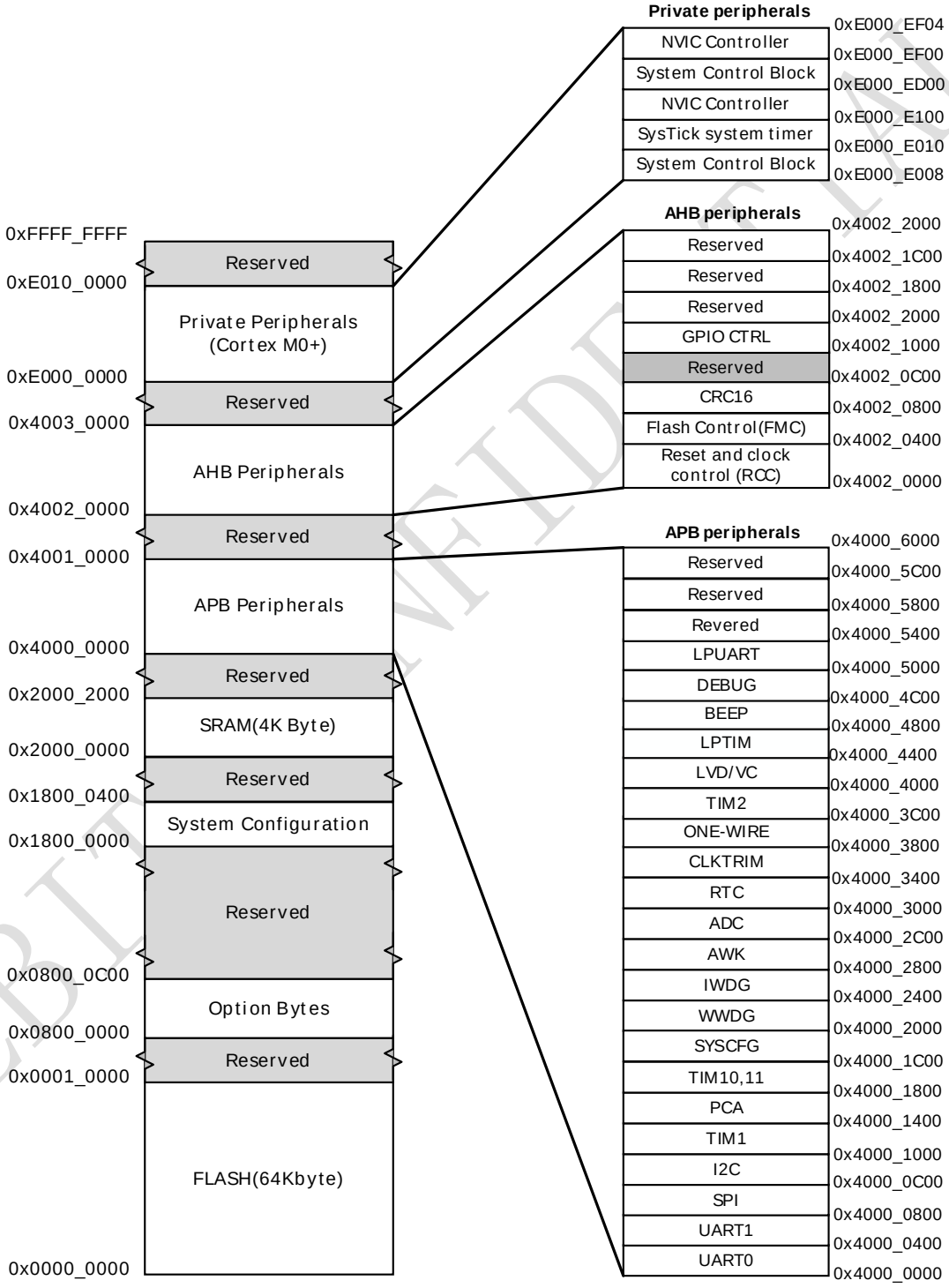


Figure 2 Memory Image

3.3 Storage Space and Module Address

Table 3 below gives the address space and boundary information of each module contained in ZB32L003 device.

Table 3 ZB32L003 Memory Image and Peripheral Register Addressing

Bus	Boundary Address	Space Size (Bytes)	Module
	0xE000_0000 - 0xE00F_FFFF	1M	Coretex-M0+ peripheral
	0x4003_0000 - 0xDFFF_FFFF		Reserve
AHB	0x4002_1000 - 0x4002_1FFF	1K	GPIOD
	0x4002_1000 - 0x4002_1BFF	1K	GPIOC
	0x4002_1000 - 0x4002_17FF	1K	GPIOB
	0x4002_1000 - 0x4002_13FF	1K	GPIOA
	0x4002_0C00 - 0x4002_0FFF	1K	Reserve
	0x4002_0800 - 0x4002_0BFF	1K	CRC16
	0x4002_0400 - 0x4002_07FF	1K	FMC
	0x4002_0000 - 0x4002_03FF	1K	RCC
	0x4000_5400 - 0x4001_FFFF		Reserve
APB	0x4000_5000 - 0x4000_53FF	1K	LPUART
	0x4000_4C00 - 0x4000_4FFF	1K	DEBUG
	0x4000_4800 - 0x4000_4BFF	1K	BEEP
	0x4000_4400 - 0x4000_47FF	1K	LPTIM
	0x4000_4000 - 0x4000_43FF	1K	LVD/VC
	0x4000_3C00 - 0x4000_3FFF	1K	TIM2
	0x4000_3800 - 0x4000_3BFF	1K	OWIER
	0x4000_3400 - 0x4000_37FF	1K	CLKTRIM
	0x4000_3000 - 0x4000_33FF	1K	RTC
	0x4000_2C00 - 0x4000_2FFF	1K	ADC
	0x4000_2800 - 0x4000_2BFF	1K	AWK
	0x4000_2400 - 0x4000_27FF	1K	IWDT
	0x4000_2000 - 0x4000_23FF	1K	WWDT
	0x4000_1C00 - 0x4000_1FFF	1K	SYSCON
	0x4000_1800 - 0x4000_1BFF	1K	TIM10/11
	0x4000_1400 - 0x4000_17FF	1K	PCA
	0x4000_1000 - 0x4000_13FF	1K	TIM1
	0x4000_0C00 - 0x4000_0FFF	1K	I2C
	0x4000_0800 - 0x4000_0BFF	1K	SPI
	0x4000_0400 - 0x4000_07FF	1K	UART1
	0x4000_0000 - 0x4000_03FF	1K	UART0
AHB	0x2000_1000 - 0x3FFF_FFFF		Reserve
	0x2000_0000 - 0x2000_0FFF	4K	SRAM
	0x1800_0100 - 0x1FFF_FFFF		Reserve
	0x1800_0000 - 0x1800_00FF	256	System Configuration
	0x0800_0200 - 0x17FF_FFFF		Reserve
	0x0800_0000 - 0x0800_01FF	512	Option Bytes
	0x0001_0000 - 0x07FF_FFFF		Reserve
	0x0000_0000 - 0x0000_FFFF	64K	Main Array (Flash)

【4】 Pin Configuration and Function Description

4.1 ZB32L003 TSOP20/QFN20 Configuration

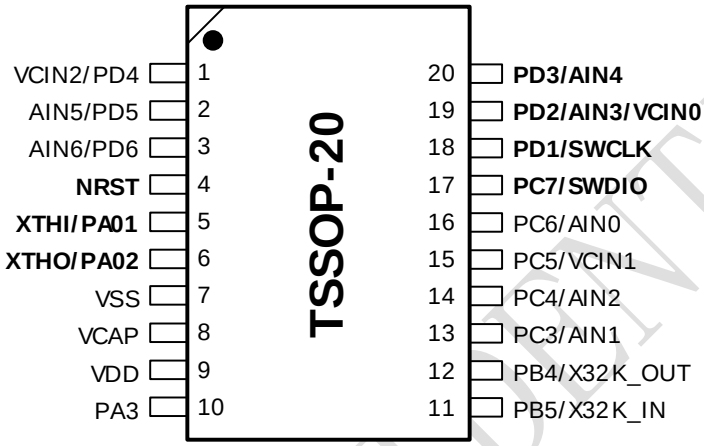


Figure 3 TSSOP20 Pin Configuration

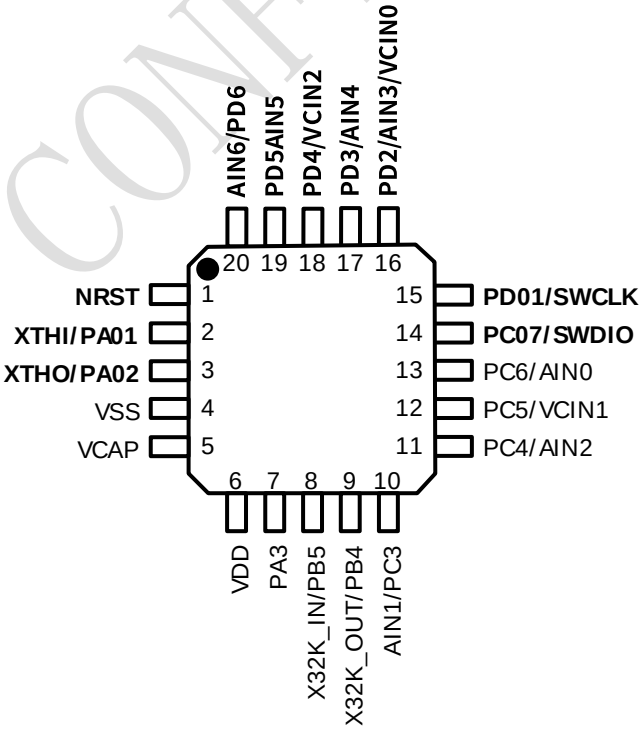


Figure 4 QFN20 Pin Configuration

4.2 ZB32L003 Pin Multiplexing

Table 4 Pin Function Multiplexing

Package			GPIOx_AFR[i+3:i]									
TSSOP20	QFN20	Config	0	1	2	3	4	5	6	7	8	F
1	18		PD4	TIM1_CH1	PCA_CH0	RTC_1HZ	TIM10_TOG	UART0_TXD	TIM10_EXT	BEEP	TIM2_CH1	VCIN2
2	19		PD5	TIM1_CH1N	PCA_CH4	SPI_MISO	I2C_SCL	UART1_TXD	TIM10_GATE	UART0_TXD	TIM2_CH4	AIN5
3	20		PD6	TIM1_CH2	PCA_CH3	SPI_MOSI	I2C_SDA	UART1_RXD	LPTIM_EXT	UART0_RXD	TIM2_CH2	AIN6
4	1	NRST(INPUT)										
5	2	OSC_IN	PA1	TIM1_CH2N		SPI_CLK	I2C_SDA	UART0_RXD	TIM10_TOG	UART1_RXD		
6	3	OSC_OUT	PA2	TIM1_CH3		SPI_NSS	I2C_SCL	UART0_TXD	TIM10_TOGN	UART1_TXD	TIM2_CH2	
7	4	VSS										
8	5	VCAP										AIN7
9	6	VDD										
10	7		PA3	TIM1_CH3N	PCA_CH2	SPI_NSS	RTC_1HZ	LPUART_RXD	PCA_ECI	VC0_OUT	TIM2_CH3	
11	8	X32K_IN	PB5	TIM1_BKIN	PCA_CH4	SPI_CLK	I2C_SDA	UART0_RXD	TIM11_TOG	LVD_OUT	TIM2_CH1	
12	9	X32K_OUT	PB4	LPTIM_GATE	PCA_ECI	SPI_NSS	I2C_SCL	UART0_TXD	TIM11_TOGN			
13	10		PC3	TIM1_CH3	TIM1_CH1N		I2C_SDA	UART1_TXD	PCA_CH1	1-WIRE	TIM2_CH3	AIN1
14	11		PC4	TIM1_CH4	TIM1_CH2N		I2C_SCL	UART1_RXD	PCA_CH0	CLK_MCO	TIM2_CH4	AIN2
15	12		PC5	TIM1_BKIN	PCA_CH0	SPI_CLK	I2C_SDA	LPUART_TXD	TIM11_GATE	LVD_OUT	TIM2_CH1	VCIN1
16	13		PC6	TIM1_CH1	PCA_CH3	SPI_MOSI	I2C_SCL	LPUART_RXD	TIM11_EXT	CLK_MCO	TIM2_CH4	AIN0
17	14	SWDIO	PC7	TIM1_CH2	PCA_CH4	SPI_MISO		UART1_RXD	LIRC_OUT	LXT_OUT		
18	15	SWDCLK	PD1		PCA_ECI			UART1_TXD	HIRC_OUT	VC0_OUT		
19	16		PD2	TIM1_CH2	PCA_CH2	SPI_MISO	RTC_1HZ	LPUART_TXD	LPTIM_TOG	1-WIRE		AIN3/VCIN0
20	17		PD3	TIM1_CH3N	PCA_CH1	SPI_MOSI	HXT_OUT	UART0_RXD	LPTIM_TOGN		TIM2_CH2	AIN4

4.3 ZB32L003 Pin Function Description

Pin No. (TSSOP-20)	Pin No. (QFN-20)	Pin Name	Pin Type	Description
1	18	PD4	PD4	PD4 universal digital input/output pin
			TIM1_CH1	TIM1 PWM output 1
			PCA_CH0	PCA capture input/comparison output 0
			RTC_1HZ	RTC 1HZ output
			TIM10_TOG	TIM10 flip output
			UART0_TX	UART0 TX
			TIM10_EXT	TIM10 external pulse input
			BEEP	BEEP output
			TIM2_CH1	TIM2 Capture Input/Compare Output 1
			VCIN2	Voltage comparator input channel 2
2	19	PD5	PD5	PD5 universal digital input/output pin
			TIM1_CH1N	TIM1 PWM output 1 inverted
			PCA_CH4	PCA capture input/comparison output 4
			SPI_MISO	SPI module master input slave output signal
			I2C_SCL	I^2C clock
			UART1_TX	UART1_TX
			TIM10_GATE	TIM10 gating
			UART0_TX	UART0 TX
			TIM2_CH4	TIM2 Capture Input/Compare Output 4
			AIN5	ADC analog input channel 5
3	20	PD6	PD6	PD6 universal digital input/output pin
			TIM1_CH2	TIM1 PWM output 2
			PCA_CH3	PCA capture input/comparison output 3
			SPI_MOSI	SPI module master outputs slave input signal.
			I2C_SDA	I2C data
			UART1_RX	UART1 RX
			LPTIM_EXT	LPTIM external pulse input
			UART0_RX	UART0 RX
			TIM2_CH2	TIM2 Capture Input/Compare Output 2
			AIN6	ADC analog input channel 6
4	1	NRST	NRST	Reset input port, active low, chip reset
			INPUT	Input pin

Pin No. (TSSOP-20)	Pin No. (QFN-20)	Pin Name	Pin Type	Description
5	2	PA1	OSC_IN	External crystal oscillator input
			PA1	PA1 Universal Digital Input/Output Pin
			TIM1_CH2N	TIM1 PWM output 2 inverted
			SPI_CLK	SPI module clock signal
			I2C_SDA	I²C data
			UART0_RX	UART0 RX
			TIM10_TOG	TIM10 flip output
			UART1_RX	UART1 RX
6	3	PA2	OSC_OUT	External crystal oscillator output
			PA2	PA2 Universal Digital Input/Output Pin
			TIM1_CH3	TIM1 PWM output 3
			SPI_NSS	SPI module slave chip selection signal
			I2C_SCL	I²C clock
			UART0_TX	UART0 TX
			TIM10_TOGN	TIM10 flips the inverting output
			UART1_TX	UART1 TX
			TIM2_CH2	TIM2 Capture Input/Compare Output 2
7	4	VSS	GND	Chip ground
8	5	VCAP	Power	LDO core power supply (Internal circuit only, external connection capacitor)
9	6	VDD	Power	Chip power supply
10	7	PA3	PA3	PA3 Universal Digital Input/Output Pin
			TIM1_CH3N	TIM1 PWM output 3 inverted
			PCA_CH2	PCA capture input/comparison output 2
			SPI_NSS	SPI module slave chip selection signal
			RTC_1HZ	RTC 1HZ output
			LPUART_RX	LPUART RX
			PCA_ECI	PCA external clock
			VC0_OUT	Voltage comparator 0 output
			TIM2_CH3	TIM2 Capture Input/Compare Output 3

Pin No. (TSSOP-20)	Pin No. (QFN-20)	Pin Name	Pin Type	Description
10	7	PA3	PA3	PA3 Universal Digital Input/Output Pin
			TIM1_CH3N	TIM1 PWM output 3 inverted
			PCA_CH2	PCA capture input/comparison output 2
			SPI_NSS	SPI module slave chip selection signal
			RTC_1HZ	RTC 1HZ output
			LPUART_RX	LPUART RX
			PCA_ECI	PCA external clock
			VC0_OUT	Voltage comparator 0 output
			TIM2_CH3	TIM2 Capture Input/Compare Output 3
11	8	PB5	X32K_IN	External 32K crystal oscillator input
			PB5	PB5 universal digital input/output pin
			TIM1_BKIN	TIM1 brake signal input
			PCA_CH4	PCA capture input/comparison output 4
			SPI_CLK	SPI module clock signal
			I2C_SDA	I²C data
			UART0_RX	UART0 RX
			TIM11_TOG	TIM11 flip output
			LVD_OUT	Low voltage detection comparator output
			TIM2_CH1	TIM2 Capture Input/Compare Output 1
12	9	PB4	X32K_OUT	External 32K crystal oscillator output
			PB4	PB4 universal digital input/output pin
			LPTIM_GATE	LPTIM gating
			PCA_ECI	PCA external clock
			SPI_NSS	SPI module slave chip selection signal
			I2C_SCL	I²C clock
			UART0_TX	UART0 TX
			TIM11_TOGN	TIM11 flips the inverting output

Pin No. (TSSOP-20)	Pin No. (QFN-20)	Pin Name	Pin Type	Description
13	10	PC3	PC3	PC3 universal digital input/output pin
			TIM1_CH3	TIM1 PWM output 3
			TIM1_CH1N	TIM1 PWM output 1 inverted
			I2C_SDA	I²C data
			UART1_TX	UART1 TX
			PCA_CH1	PCA capture input/comparison output 1
			1-WIRE	1-wire input and output
			TIM2_CH3	TIM2 Capture Input/Compare Output 3
			AIN1	ADC analog input channel 1
14	11	PC4	PC4	PC4 universal digital input/output pin
			TIM1_CH4	TIM1 PWM output 4
			TIM1_CH2N	TIM1 PWM output 2 inverted
			I2C_SCL	I²C clock
			UART1_RX	UART1 RX
			PCA_CH0	PCA capture input/comparison output 0
			CLK_MCO	CPU clock output
			TIM2_CH4	TIM2 Capture Input/Compare Output 4
			AIN2	ADC analog input channel 2
15	12	PC5	PC5	PC5 universal digital input/output pin
			TIM1_BKIN	TIM1 brake signal input
			PCA_CH0	PCA capture input/comparison output 0
			SPI_CLK	SPI module clock signal
			I2C_SDA	I²C data
			LPUART_TX	LPUART TX
			TIM11_GATE	TIM11 gating
			LVD_OUT	Low voltage detection comparator output
			TIM2_CH1	TIM2 Capture Input/Compare Output 1
			VCIN1	analog input

Pin No. (TSSOP-20)	Pin No. (QFN-20)	Pin Name	Pin Type	Description
16	13	PC6	PC6	PC6 universal digital input/output pin
			TIM1_CH1	TIM1 PWM output 1
			PCA_CH3	PCA capture input/comparison output 3
			SPI_MOSI	SPI module master outputs slave input signal.
			I2C_SCL	I²C clock
			LPUART_RX	LPUART RX
			TIM11_EXT	TIM11 external pulse input
			CLK_MCO	CPU clock output
			TIM2_CH4	TIM2 Capture Input/Compare Output 4
			AIN0	ADC analog input channel 0
17	14	PC7	SWDIO	SWD IO
			PC7	PC7 universal digital input/output pin
			TIM1_CH2	TIM1 PWM output 2
			PCA_CH4	PCA capture input/comparison output 4
			SPI_MISO	SPI module master input slave output signal
			UART1_RX	UART1 RX
			LIRC_OUT	Internal low frequency RC clock 38.4KHZ output
			X32K_OUT	External low frequency crystal oscillator output
18	15	PD1	SWDCLK	SWD clock
			PD1	PD1 universal digital input/output pin
			PCA_ECI	PCA external clock
			UART1_TX	UART1 TX
			HIRC_OUT	Internal high frequency RC clock 24MHZ
			VC0_OUT	Voltage comparator 0 output

Pin No. (TSSOP-20)	Pin No. (QFN-20)	Pin Name	Pin Type	Description
19	16	PD2	PD2	PD2 universal digital input/output pin
			TIM1_CH2	TIM1 PWM output 2
			PCA_CH2	PCA capture input/comparison output 2
			SPI_MISO	SPI module master input slave output signal
			RTC_1HZ	RTC 1HZ output
			LPUART_TX	LPUART TX
			LPTIM_TOG	LPTIM flip output
			1-WIRE	1-wire input and output
			VCIN0	Voltage comparator input channel 0
			AIN3	ADC analog input channel 3
20	17	PD3	PD3	PD3 universal digital input/output pin
			TIM1_CH3N	TIM1 PWM output 3 inverted
			PCA_CH1	PCA capture input/comparison output 1
			SPI_MOSI	SPI module master outputs slave input signal.
			HXT_OUT	External high frequency crystal oscillator output
			UART0_RX	UART0 RX
			LPTIM_TOGN	LPTIM flip inverted output
			TIM2_CH2	TIM2 Capture Input/Compare Output 2
			AIN4	ADC analog input channel 4

【5】 Electrical Specification

5.1 Test Condition

Unless otherwise specified, all voltages are based on VSS.

5.1-1 Minimum and Maximum Values

Unless otherwise specified, all the minimum and maximum values will be guaranteed under the worst environmental temperature, power supply voltage and clock frequency conditions by testing 100% products at ambient temperatures Ta = 25 C and $T_A=T_{op,Max}$ ($T_{op,Max}$ depends on the temperature range corresponding to the selected Part Number).

The notes at the bottom of each table indicate that the data obtained through comprehensive evaluation, design simulation and/or process characteristics will not be tested on the production line; On the basis of comprehensive evaluation, the minimum and maximum values are obtained by taking the average value and then adding and subtracting three times the standard distribution (average ±3Σ) after sample testing.

5.1-2 Typical Value

Unless otherwise specified, typical data are based on ta = 25 c and VDD=3.3V (2.5V≤VDD≤5.5V). These data are only used for design guidance and have not been tested.

Typical ADC accuracy values are obtained by sampling a standard batch and testing in all temperature ranges. The error of 95% products is less than or equal to the given value (average 2 σ).

5.2 Absolute Maximum Rating

Symbol	Parameter	Condition	Min	Type	Max	Unit
VDD	Supply voltage		2.5		5.5	V
V_{IO}	Voltage of IO		-0.3		VDD+0.3	V
T_{STG}	Storage temperature		-40	25	150	°C
T_{OP}	Working temperature		-40	25	85	°C
F_{CPU}	CPU working frequency		32.768K	4M	24M	Hz
$V_{ESD, HBM}$	See5.12					
$V_{ESD, CDM}$	See5.12					
$V_{ESD, MM}$	See5.12					

Note:

1. Temperature test method: CP stage test chip level test with high temperature of 85 C, low temperature of-40 C and high temperature of 85 C is only tested in laboratory and Production Quality Qualification.
2. Frequency test method: 24MHz frequency is tested in CP stage, and Final Test only focuses on the defects of packaging process.

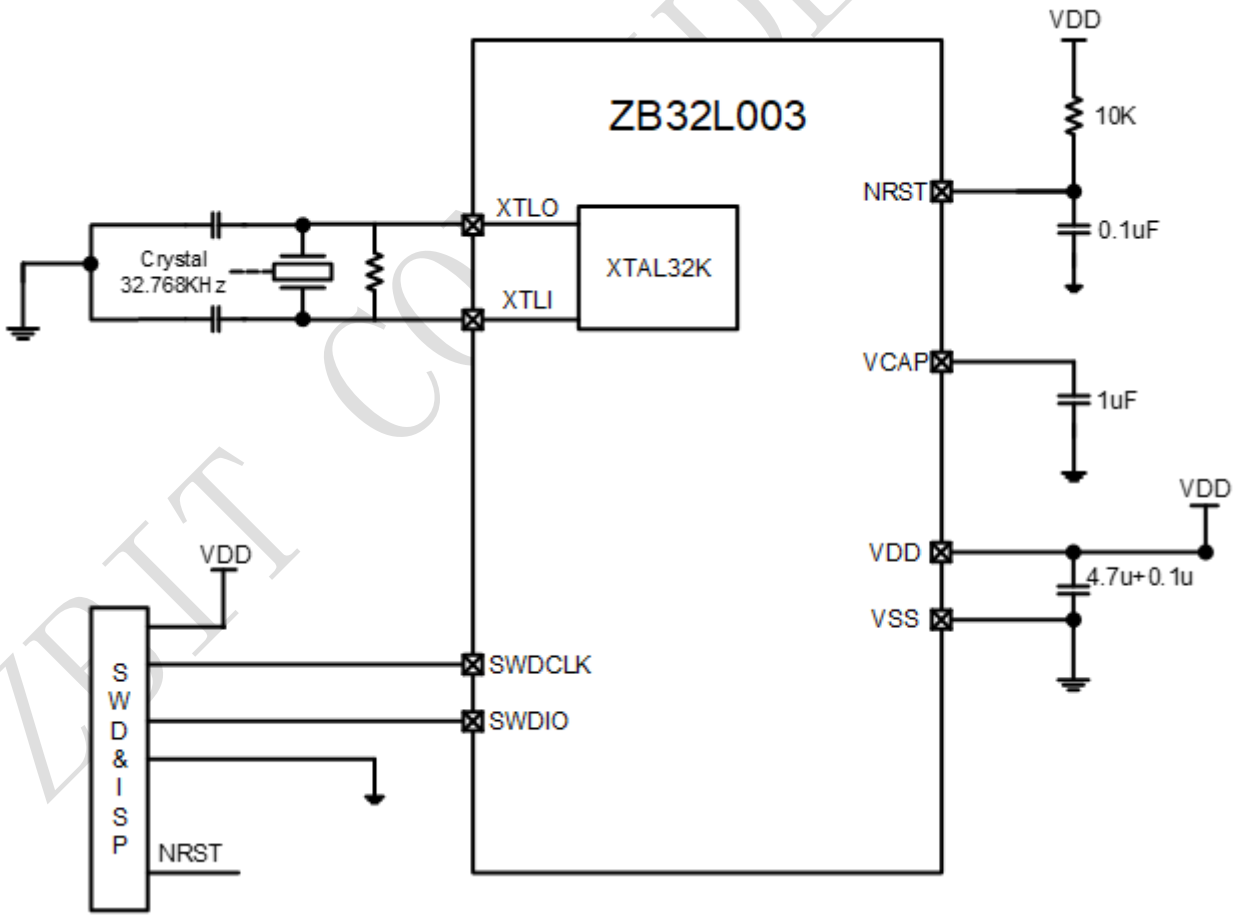
5.3 Recommended Working Conditions

Symbol	Parameter	Condition	Min	Max	Unit	Reference
VDD	Power supply voltage	-	2.5	5.5	V	
C_s	VCAP capacitance	-	0.47	2.2	μF	Recommended 1.0μF
T_{OP}	Operating temperature	-	-40	85	°C	

Note:

1. Recommended working conditions are the conditions to ensure the normal operation of semiconductor chips. Within the recommended working conditions, all specifications of electrical characteristics can be guaranteed. Always use semiconductor chips under recommended working conditions. Use beyond this condition may affect the reliability of the semiconductor.
2. The company does not guarantee the use of items, conditions of use or logical combinations not recorded in this data manual. If users consider using this chip outside the listed conditions, please contact the sales representative in advance.

5.4 Typical Application Block Diagram



5.5 DC Characteristics

5.5-1 Operating current characteristics

Symbol	Parameter	Condition			Type	Max	Unit
I_{DD} (Run Mode in RAM)	All Peripherals clock OFF, Run while(1) in RAM	V_{core} =1.2V VDD=2.5V-5.5V	Clock source: HIRC	4M	180	289	μA
				8M	225	225	
				16M	315	315	
				24M	409	409	
I_{DD} (Run Mode in Flash)	All Peripherals clock ON, Run while(1) in Flash	V_{core} =1.2V VDD=2.5V-5.5V	Clock source: HIRC	4M	561	601	μA
				8M	985	1047	
				16M	1833	1938	
				24M	2708	2860	
	All Peripherals clock OFF, Run while(1) in Flash	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: HIRC	4M	497	529	μA
				8M	857	901	
				16M	1576	1645	
				24M	2318	2411	
	All Peripherals clock ON, Run while(1) in Flash	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LXT 32.768KHz Driver=1	Ta=-40°C	62.9	75.2	μA
				Ta=25°C	67	76.5	
				Ta=50°C	66.3	78.3	
				Ta=85°C	74.5	89	
	All Peripherals clock OFF, Run while(1) in Flash	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LXT 32.768KHz Driver=1	Ta=-40°C	62.5	74.5	μA
				Ta=25°C	66.3	75.8	
				Ta=50°C	65.6	77.6	
				Ta=85°C	73.9	88.8	
I_{DD} (Sleep Mode)	All Peripherals clock ON	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: HIRC	4M	230	258	μA
				8M	326	354	
				16M	517	545	
				24M	719	754	
	All Peripherals clock OFF	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: HIRC	4M	166	194	μA
				8M	197	225	
				16M	258	287	
				24M	323	350	
	All Peripherals clock ON	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LXT 32.768KHz Driver=1	Ta=-40°C	60.2	72.2	μA
				Ta=25°C	63.8	73.4	
				Ta=50°C	63.4	75.4	
				Ta=85°C	71.5	86	
	All Peripherals clock OFF	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LXT 32.768KHz Driver=1	Ta=-40°C	59.6	71.6	μA
				Ta=25°C	63.2	72.9	
				Ta=50°C	62.8	74.6	
				Ta=85°C	70.8	85.3	

Symbol	Parameter	Condition			Type	Max	Unit
I_{DD} (Deep Sleep Mode)	All Peripherals clock OFF, except RTC,IWDG, LPTIM, AWK	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LIRC 32.768KHz	Ta=-40°C	0.7	0.8	μA
				Ta=25°C	0.9	1.1	
				Ta=50°C	1.4	1.9	
				Ta=85°C	4.3		
	All Peripherals clock OFF, except RTC	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LIRC 32.768KHz	Ta=-40°C	0.7	0.8	μA
				Ta=25°C	0.9	1.1	
				Ta=50°C	1.3	1.9	
				Ta=85°C	4.3	10.6	
	All Peripherals clock OFF, except IWDG	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LIRC 32.768KHz	Ta=-40°C	0.7	0.8	μA
				Ta=25°C	0.9	1.1	
				Ta=50°C	1.4	1.9	
				Ta=85°C	4.3	10.6	
	All Peripherals clock OFF, except LPTIM	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LIRC 32.768KHz	Ta=-40°C	0.7	0.8	μA
				Ta=25°C	0.9	1.1	
				Ta=50°C	1.4	1.9	
				Ta=85°C	4.3	10.6	
	All Peripherals clock OFF, except AWK	V_{core} =1.2V VDD =2.5V-5.5V	Clock source: LIRC 32.768KHz	Ta=-40°C	0.7	0.8	μA
				Ta=25°C	0.9	1.1	
				Ta=50°C	1.4	1.9	
				Ta=85°C	4.3	10.6	
	All Peripherals clock OFF,	V_{core} =1.2V VDD =2.5V-5.5V		Ta=-40°C	0.4	0.5	μA
				Ta=25°C	0.6	0.8	
				Ta=50°C	1.1	1.7	
				Ta=85°C	4	10.2	

Note:

1. The data are based on TT Wafer assessment results and are not tested in production.
2. Unless otherwise specified, the Typical value (Typ) is measured under the conditions of ta = 25°C and VDD=3.3V.
3. Unless otherwise specified, the Maximum value (max) is the maximum value measured under the conditions of ta =-40°C~85°C and VDD=2.5V~5.5V.
4. When LXT 32.768KHz is used, an external crystal oscillator is connected in parallel with a 3MΩ resistor.

5.5-2 Power On Reset/Brown Out Reset

Symbol	Parameter	Condition	Min	Type	Max	Unit
VPOR VBOR	POR release voltage (power-on process) BOR detection voltage (power failure process)		2.2	2.25	2.3	V

Note: It is guaranteed by design and not tested in production.

5.6 AC Characteristics

5.6-1 Output Characteristics-Ports PA, PB, PC, PD

Symbol	Parameter	Condition	Min	Max	Unit
V_{OH}	High level output voltage Source Current	Sourcing 2.8 mA, VDD = 3.3 V (see Note 1)	VDD-0.2		V
		Sourcing 4.2 mA, VDD = 3.3 V (see Note 2)	VDD-0.3		
V_{OL}	Low level output voltage Sink Current	Sinking 2.8 mA, VDD = 3.3 V (see Note 1)		VSS+0.2	V
		Sinking 4.2 mA, VDD = 3.3 V (see Note 2)		VSS+0.3	
V_{OHD}	High level output voltage Double Source Current	Sourcing 5.2 mA, VDD = 3.3 V (see Note 1)	VDD-0.2		V
		Sourcing 7.8 mA, VDD = 3.3 V (see Note 2)	VDD-0.3		
V_{OLD}	Low level output voltage Double Sink Current	Sinking 5.6 mA, VDD = 3.3 V (see Note 1)		VSS+0.2	V
		Sinking 8.4 mA, VDD = 3.3 V (see Note 2)		VSS+0.3	

Note:

1. The maximum current of a single output PIN is 8.4mA, IVDD Max = 80mA and IVSS Max = 100mA.
2. From the comprehensive evaluation, it is not tested in production.

5.6-2 Input Characteristics-Ports PA, PB, PC, PD

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IT+}	Positive-going input threshold voltage	VDD=2.5	1.33	1.365		V
		VDD=3.3	1.74	1.773		V
		VDD=5	2.64	2.66		V
V_{IT-}	Negative-going input threshold voltage	VDD=2.5		1.01	1.04	V
		VDD=3.3		1.324	1.36	V
		VDD=5		2.016	2.06	V
V_{hys}	Input voltage hysteresis (VIT+ - VIT-)	VDD=2.5	0.31	0.354		V
		VDD=3.3	0.4	0.448		V
		VDD=5	0.59	0.623		V
$R_{pullhigh}$	Pullup Resistor	VDD=5 VIN=0	49	60	75	Kohm
		VDD=3 VIN=0	80	107	130	
$R_{pulllow}$	Pulldown Resistor	VDD=5 VIN=5	58	68	82	
		VDD=3 VIN=3	34	42	49	
C_{input}	Input Capacitance			5		pf

Note: Based on comprehensive evaluation, it is not tested in production.

5.6-3 Port Leakage Characteristics-PA, PB, PC, PD

Symbol	Parameter	Condition	VDD	Max	Unit
I_{lkg}	Leakage current	See Note 1, 2	2.5V / 3.6V	±50	nA

Notes:
1. The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.
3. From the comprehensive evaluation, it is not tested in production.

5.6-4 Timer/Counter Input Sampling Requirements

Symbol	Parameter	Condition	Min	Max	Unit
T(int)	External interrupt timing	External trigger signal for the interrupt flag(see Note1)	760		ns
T(cap)	Timer Captuter timing	TIM1/TIM2 capture pulse width Fsystme =4MHz	2.4		μs
f_{EXT}	Timer clock frequency applied to pin	TIM1,TIM2,TIM10,TIM11 external clock input Fsystme =4MHz	0	$f_{TIMxCLK}/2$	MHz
T(PCA)	PCA clock frequency applied to pin	PCA external clock input Fsystme =4MHz	0	$f_{TIMxCLK}/8$	MHz

Note:

1. The external signal sets the interrupt flag every time the minimum t(int) parameters are met. It may be set even with trigger signals shorter than t(int).
2. From the comprehensive evaluation, it is not tested in production.

5.6-5 Internal HIRC Oscillator

Symbol	Parameter	Condition	Min	Type	Max	Unit
F_{MCLK}	Internal RC Oscillation frequency		4.0	4.0 8.0 16.0 24	24	MHz
I_{Mstart}(1)	Start-up time Not including software calibration	F_{MCLK}=4MHz	3.25	4.03	5.05	μs
		F_{MCLK}=8MHz	3.43	4.07	5.16	μs
		F_{MCLK}=16MHz	3.41	4	5.1	μs
		F_{MCLK}=24MHz	3.32	4.04	5.1	μs
I_{MCLK}	Current consumption	F_{MCLK}=4MHz	72.31	83.78	99.65	μA
		F_{MCLK}=8MHz	88.77	94.65	104.19	μA
		F_{MCLK}=16MHz	97.19	105.19	118.1	μA
		F_{MCLK}=24MHz	112.89	121.79	131.53	μA
DC_{MCLK}	Duty cycle		45	50	55	%
D_{evM}	Frequency Deviation	VDD = 2.5V~5.5V Ta = -40°C ~ 85°C	-2.5		+2.5	%

Note: The data are based on the assessment results and are not tested in production.

5.6-6 Internal LIRC Oscillator

Symbol	Parameter	Condition	Min	Type	Max	Unit
F_{ACLK}	Internal RC Oscillation frequency		38.15 32.474	38.4 32.768	38.74 32.86	KHz
T_{Astart}(1)	Start-up time: 32.768K 38.4K		 90 75	 120 106	 150 125	μs
IACLK	Current consumption 32.768K 38.4K		 0.26 0.34	 0.35 0.43	 0.48 0.51	μA
DC_{ACLK}	Duty cycle		43.14	50	53.25	%
D_{evA}	Frequency Deviation	VDD = 2.5V～5.5V Ta = -40°C～85°C	-10		+10	%

Note: The data are based on the assessment results and are not tested in production.

5.6-7 External LXT Crystal Oscillator

Symbol	Parameter	Condition	Min	Type	Max	Unit
F_{SCLK}	Crystal frequency		32.75	32.768	32.79	KHz
ESR_{SCLK}	Supported crystal equivalent series resistance		40	65	85	KOhm
C_{SCLK}(1)	Supported crystal external load range	There are two C_{SCLK} on 2 crystal pins respectively		12		pF
Idd(2)	Current consumptionwhen stable	ESR=65KOhmC_{SCLK}=12 pF	200	250	350	nA
DCSCLK	Duty cycle		48.85	50	52.35	%
Tstart(3)	Start-up time	ESR=65KOhm CSCLK=12pF40%～60% duty cycle reached	0.44	1	1.7	s

Note:

1. It is recommended to use crystals to give reference values.
2. RCC_LXTCR.LXTDRV=0011, ESR=65K
3. The data are based on the assessment results and are not tested in production.

5.6-8 External HXT Crystal Oscillator

Symbol	Parameter	Condition	Min	Type	Max	Unit
F_{FCLK}	Crystal frequency		4	16	24	MHz
ESR_{FCLK}	Supported crystal equivalent series resistance		30	60	1500	Ohm
C_{FCLK}(1)	Supported crystal external external load range	There are 2 C_{FCLK} on 2 crystal pins individually		12		pF
Idd(2)	Current consumption	24MHz Xtal ESR=30Ohm C_{FCLK}=12pF		300		μA
DC_{FCLK}	Duty cycle		50	50	51.8	%
T_{start}	Start-up time	24MHz	442.59	500	554.94	μs

Note:

1. It is recommended to use crystals to give reference values.
2. Current consumption could vary with oscillating frequency, RCC_HXTCR.HXTDRV=110.
3. The data is based on the assessment results and is not tested in production.

5.7 I2C Interface Characteristics

Symbol	Parameter	Standard mode (100K)		Fast mode (400K)		High speed mode (1M)		Unit
		Min	Max	Min	Max	Min	Max	
tSCLL	SCL clock low time	4.95		1.15		0.495		us
tSCLH	SCL clock high time	4.95		1.15		0.495		us
tSU.SDA	SDA setup time	5		5		5		ns
tHD.SDA	SDA holding time	5		5		5		ns
tHD.STA	Start condition holding time	3*pclk		3*pclk		3*pclk		us
tSU.STA	Repeated start condition establishment time	12*pclk		12*pclk		2*pclk		us
tSU.STO	Stop condition establishment time	2*pclk		2*pclk		2*pclk		us
tBUF	Bus idle (stop condition to start condition)	14*pclk		14*pclk		4*pclk		us

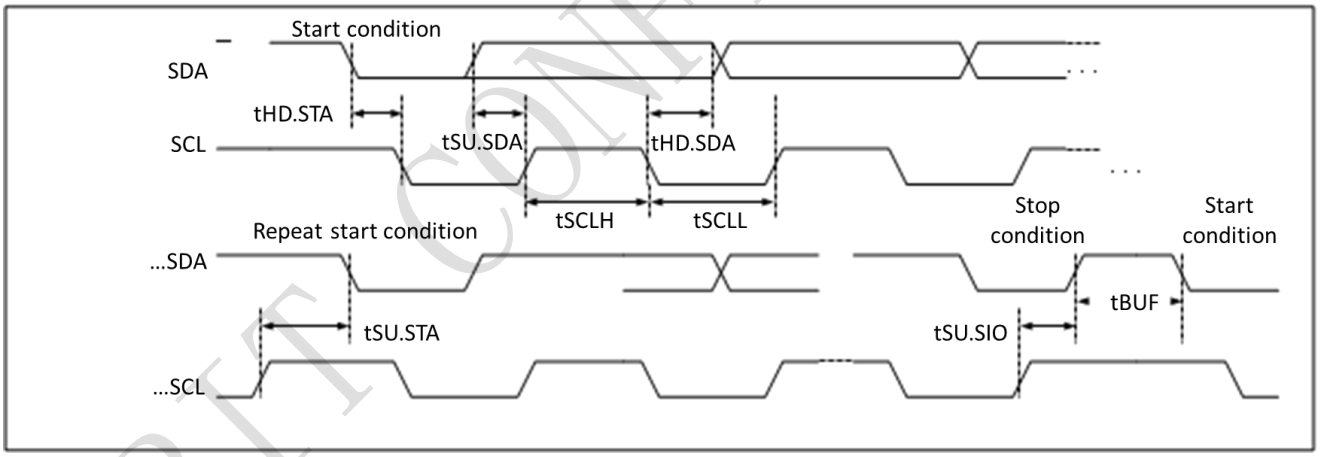


Figure 5 I2C timing block diagram

5.8 SPI Interface Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{c(SCK)}$	Period of serial clock	Master mode	2*pclk		ns
		Slave mode	4*pclk		ns
$t_{w(SCKH)}$	High Time of Serial Clock	Master mode	1*pclk		ns
		Slave mode	2*pclk		ns
$t_{w(SCKL)}$	Low level time of serial clock	Master mode	1*pclk		ns
		Slave mode	2*pclk		ns
$t_{su(SSN)}$	Set-up time of slave selection	Slave mode	3*pclk		ns
$t_{h(SSN)}$	Slave selected hold time	Slave mode	3*pclk		ns
$t_{v(MO)}$	Effective time of Master data output			5	ns
$t_{h(MO)}$	Holding time of Master data output		0		ns
$t_{v(SO)}$	Effective time of slave data output			30+1.5*pclk	ns
$t_{h(SO)}$	Holding time of slave data output		0.5*pclk		ns
$t_{su(MI)}$	Setup time of Master data input		30		ns
$t_{h(MI)}$	Holding time of Master data input		0		ns
$t_{su(SI)}$	Set-up time of slave data input		0		ns
$t_{h(SI)}$	Holding time of slave data input		10+1.5*pclk	-	ns

Note: Guaranteed by design, not tested in production.

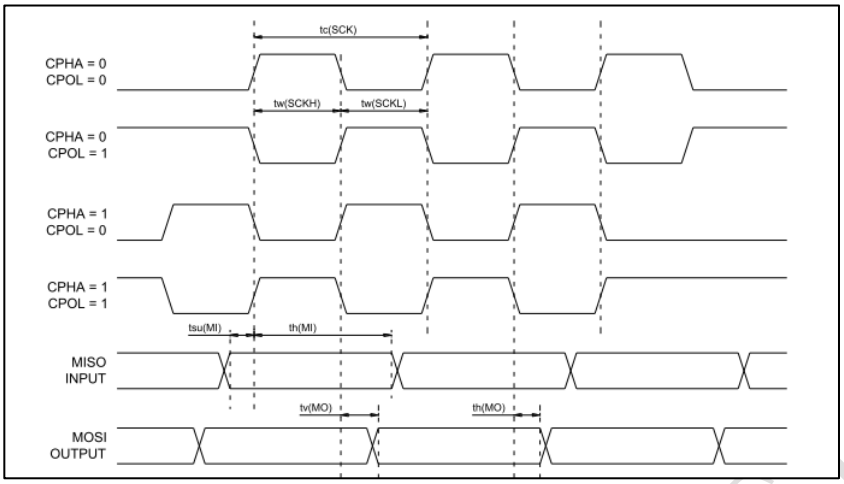


Figure 6 SPI timing diagram (Master mode)

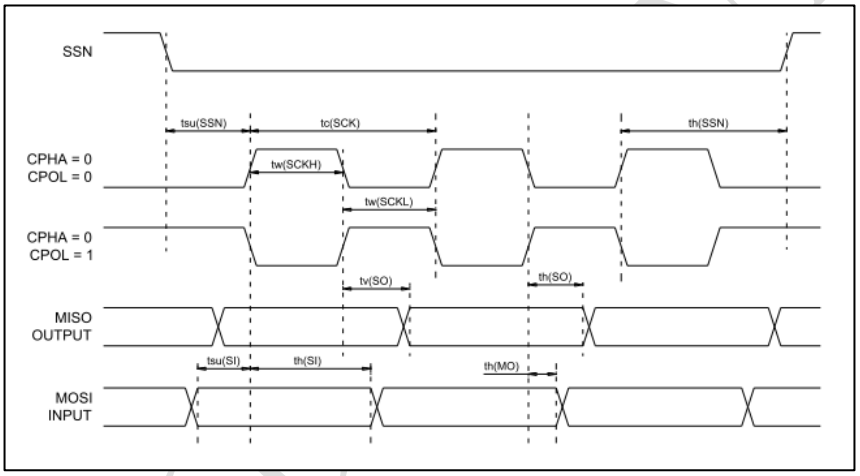


Figure 7 SPI timing diagram (Slave mode CPHA=0)

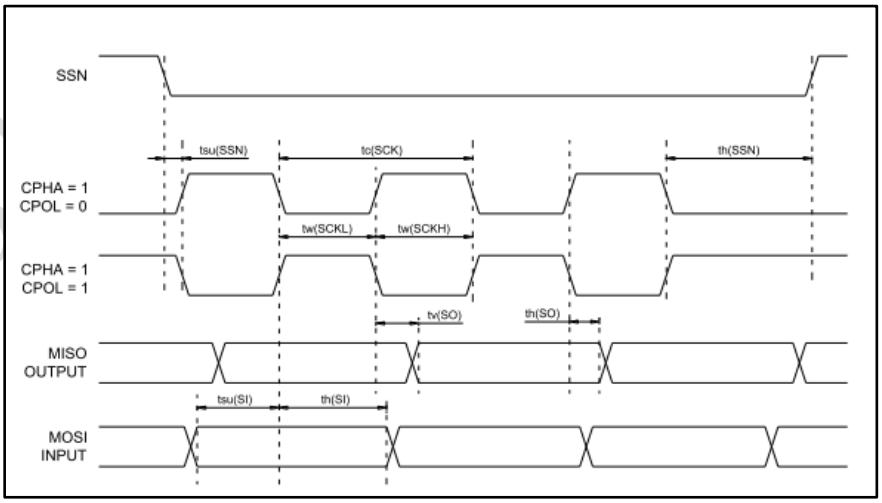


Figure 8 SPI timing diagram (Slave mode CPHA=1)

5.9 12-Bit A/D Converter

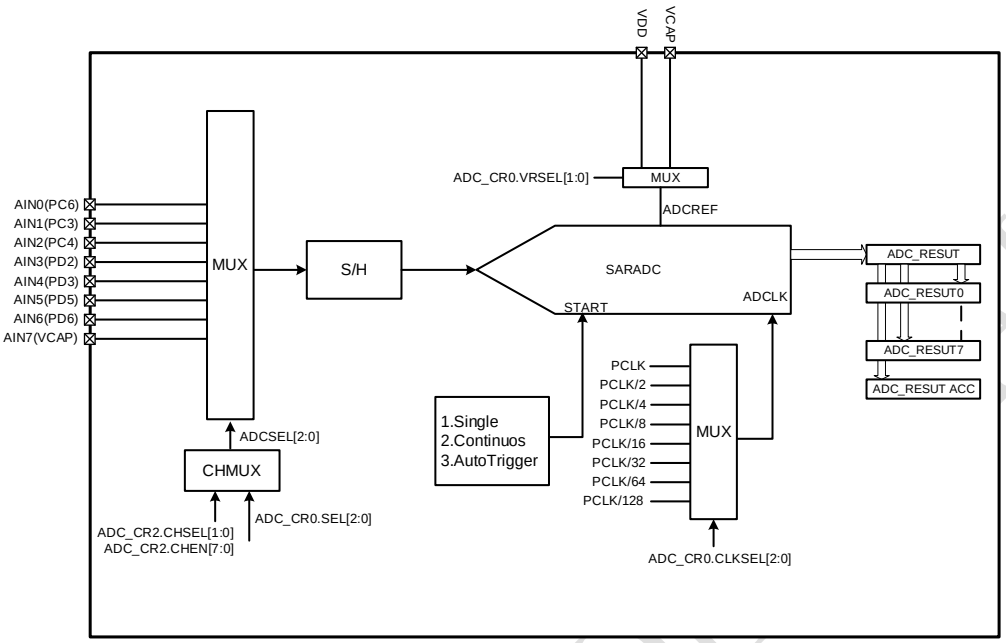


Table 5 ADC Characteristic Table

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{ADCIN}	Input voltage range	Single	0		VREF	V
V_{REF}	ADC reference Voltage VDD			VDD		V
	ADC reference Voltage VCAP			2.5		V
I_{ADC}			0.7	0.9	1.2	mA
C_{ADC}	ADC input capacitance			16	18.4	pF
R_{ADC}	ADC sampling switch impedance			0.6		kΩ
R_{AIN}	External resistance on V_{IN}			0.1	50	kΩ
f_{ADCCLK}	ADC clock Frequency		0.5	4	16	MHz
$T_{ADCSTART}$	Startup time of ADC bias current		2	3	4	μs
$T_{ADCCONV}$	Conversion time		16	16	20	cycles
ENOB			9.5	10	10.4	Bit
DNL	Differential non-linearity	VREF = VDD		±1	2	LSB
INL	Integral non-linearity		-10	±1	10	LSB
E_o	Offset error		-9.06	±1	9	LSB
E_g	Gain error		-9	±1	9	LSB
DNL	Differential non-linearity	VREF = VCAP		±1	3	LSB
INL	Integral non-linearity		-20	±1	20	LSB
E_o	Offset error		-19.16	±1	19	LSB
E_g	Gain error		-16	±1	16	LSB

Note: It is guaranteed by design and not tested in production.

Refer to the figure below for the typical application diagram of ADC.

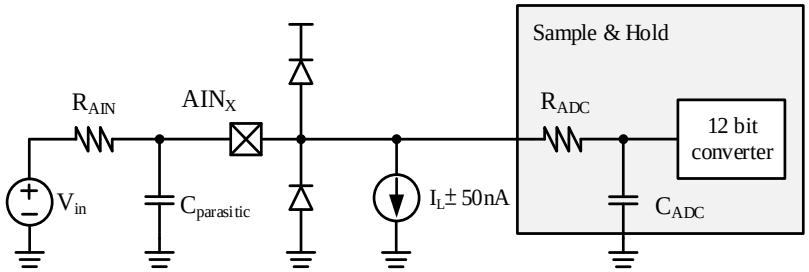


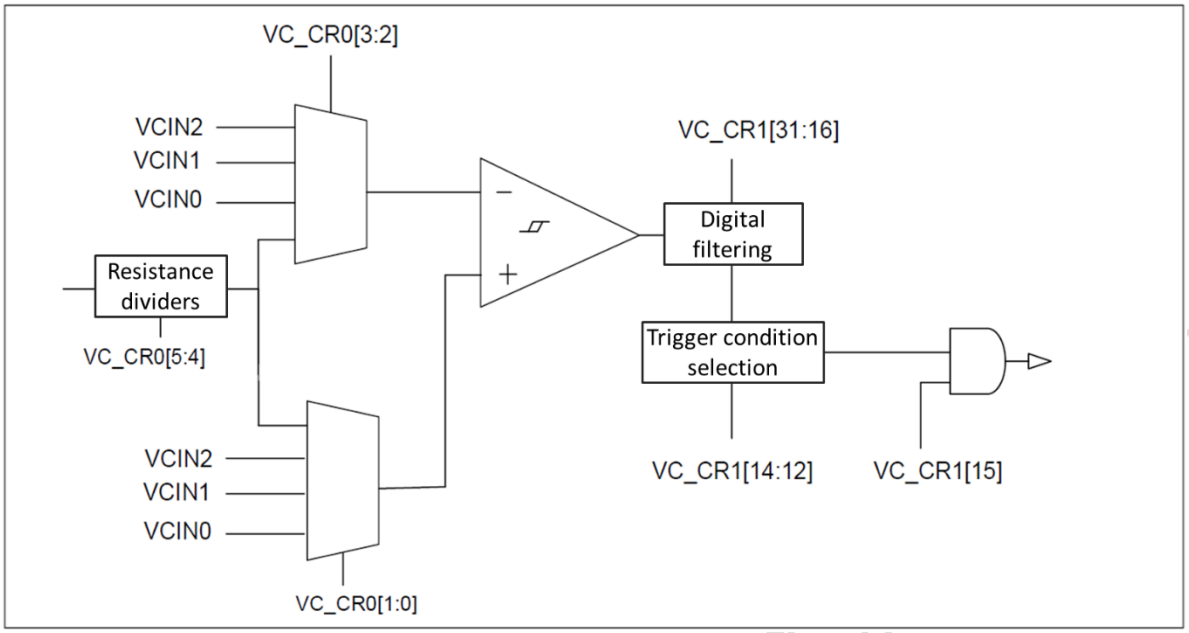
Figure 9 Typical application of ADC

1. $C_{parasitic}$ is the capacitance on PCB, and its capacitance value depends on PCB line configuration (about 7pF). If the capacitance value is too large, the ADC accuracy will be reduced, or the ADC clock frequency needs to be reduced to maintain the ADC accuracy.
2. Table 5.7.2. The maximum RAIN value is obtained by referring to CADC and RADC in ADC characteristic table (Table 5.7.1) and Figure 9.

Table 6 Maximum RAIN value corresponds to fADCCLK and ts.

t_s(μs)	f_{ADCCLK}(Hz)	SAM	R_{AIN}(kΩ)
0.167	24M	4	0.1
0.333	12M	4	0.8
0.667	6M	4	2.2
2.67	3M	8	10.8
5.33	1.5M	8	22.2
10.7	0.75M	8	45
21.3	0.375M	8	50

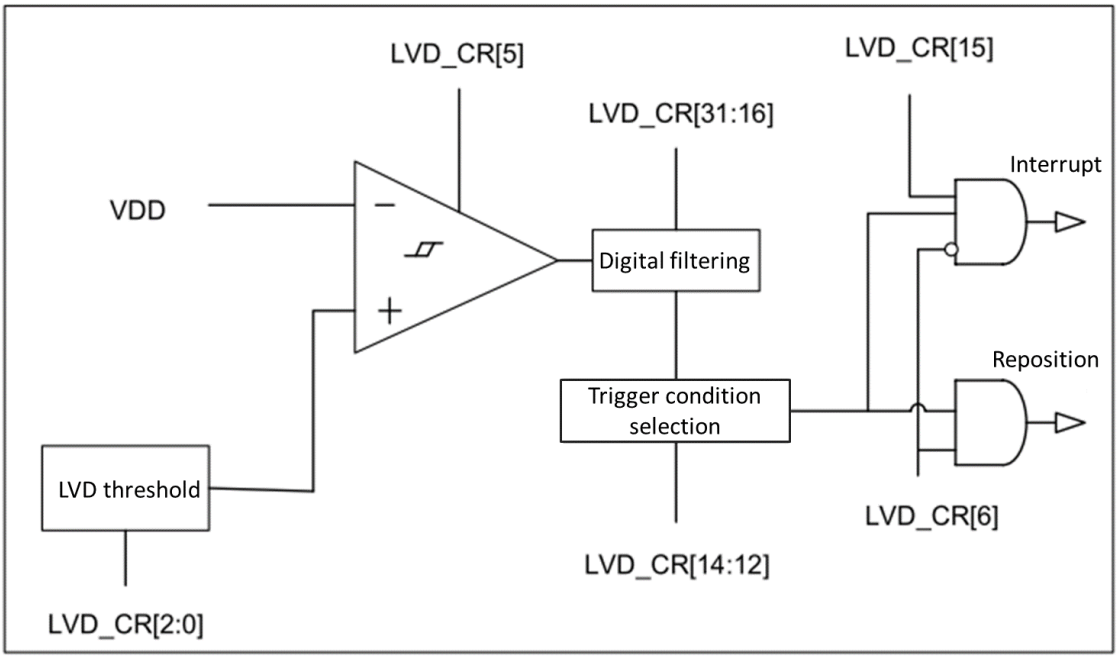
5.10 Analog Voltage Comparator



Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{in}	Input voltage range		0		5.5	V
V_{incom}	Input common mode range		0		5.5	V
V_{offse}	Input offset	@-40~125℃	-10	±5	10	mV
I_{comp}	Comparator’s current		8.55	9.28	17.2	μA
$T_{response}$	Comparator’s response		43.2	100	362	ns

Note: The data is based on the assessment results and is not tested in production.

5.11 Low Voltage Detection Characteristics



Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{level}	VDD Detectable threshold	LVD_CR[2:0] = 000 (4.4V)	4.215	4.352	4.58	V
		LVD_CR[2:0] = 001 (4.0V)	3.795	3.917	4.114	
		LVD_CR[2:0] = 010 (3.6V)	3.448	3.562	3.709	
		LVD_CR[2:0] = 011 (3.3V)	3.163	3.266	3.436	
		LVD_CR[2:0] = 100 (3.1V)	2.919	3.014	3.173	
		LVD_CR[2:0] = 101 (2.9V)	2.71	2.799	2.942	
		LVD_CR[2:0] = 110 (2.7V)	2.53	2.613	2.751	
		LVD_CR[2:0] = 111 (2.5V)	2.37	2.45	2.578	
I_{comp}	Detector' s current		0.981	1.076	1.1	μA
$T_{response}$	Detector' s response time when VDD fall below or rise abovethe threshold		1.34	1.547	1.5468	μs
T_{setup}	Detector' s setup time when ENABLE.VDD unchanged.		3.81	4	4.03	μs

Note: The data are based on the assessment results and are not tested in production.

5.12 Memory Erase/Write Characteristics

Symbol	Parameter	Condition	Min	Type	Max	Unit
EC_{flash}	Sector Endurance		20k			cycles
RET_{flash}	Data Retention		20			Years
T_{prog}	Byte/Half Word/Word ProgramTime		30	51.7	60	μs
$T_{Sector-erase}$	Sector Erase Time		3.5	4.26	4.5	ms
$T_{Chip-erase}$	Chip Erase Time		20	34.5	40	ms

5.13 Wake-Up Time from Low Power Mode

Wake-up time is the time when the chip wakes up from external interrupt and deep sleep mode. Clock source is HIRC, VDD=3.3V.

Symbol	Parameter	Condition	Min	Type	Max	Unit
T_{wakeup}	Deep sleep mode to active mode	HIRC Frequency: HIRC = 24MHz, HCLK = 4MHz	55	60	65	μs

Note: The data are based on the assessment results and are not tested in production.

5.14 Electromagnetic Sensitivity Characteristics

5.14-1 ESD

Symbol	Parameter	Condition	Min	Type	Max	Unit
$V_{ESD, HBM}$	ESD @ Human Body Mode		2			KV
$V_{ESD, CDM}$	ESD @ Charge Device Mode		2			KV
$V_{ESD, MM}$	ESD @ Machine Mode		150			V
$I_{Latchup}$	Latch up current			100		mA

5.14-2 Static Latch-up

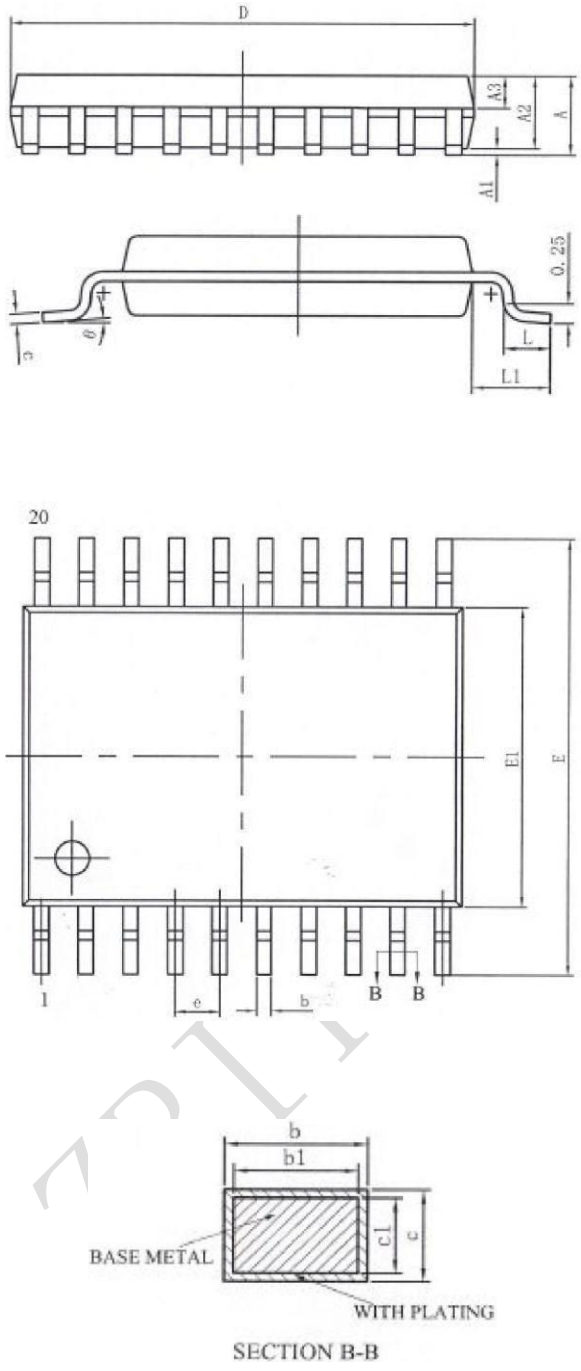
In order to evaluate the latching performance, two complementary static latching tests are required on three samples:

- For each power supply pin, the supply voltage exceeding the limit is provided.
- Current is injected at each input, output, and configurable I/O pin. This test is compliant with the EIA/JESD78A integrated circuit latching standard.

Symbol	Parameter	Condition	Type
LU	Static latch-up class	TA = +25 °C conforming to JESD78A	Class I Level A

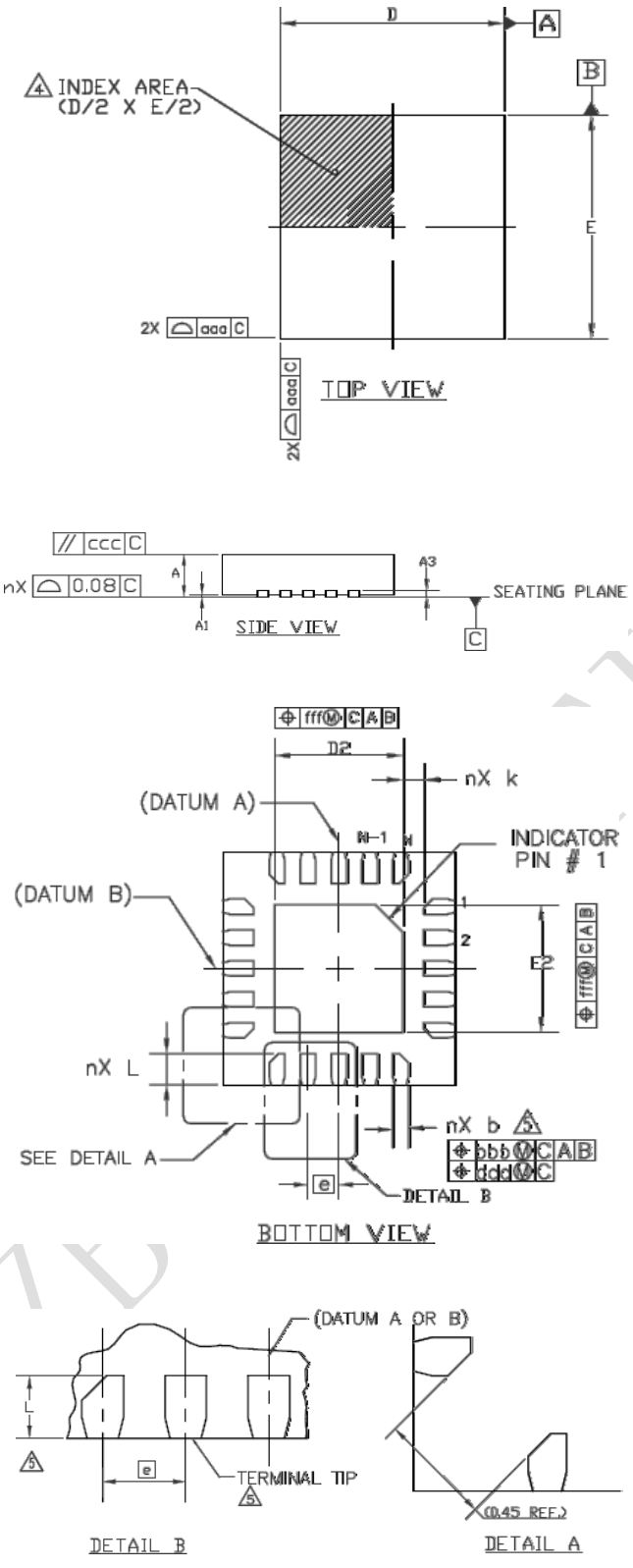
【6】 Packaging Characteristics

6.1 TSSOP20 Package



TSSOP20			
Symbol	**Min**	**Nominal**	**Max**
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC.		
L	0.45	0.60	0.75
L1	1.00 BSC.		
θ	0	-	8°

6.2 QFN20 Package



QFN20			
Symbol	**Min**	**Nominal**	**Max**
A	0.70	0.75	0.80
b	0.15	0.20	0.25
D		3.00 BSC.	
D2	1.55	1.65	1.75
E		3.00 BSC.	
E2	1.55	1.65	1.75
e		0.40 BSC.	
L	0.30	0.40	0.50
n		20	
nD		five	
nE		five	
A1	0	0.02	0.05
A3		0.203 REF.	
K	0.20	-	-
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	

6.3 Screen Printing Instructions

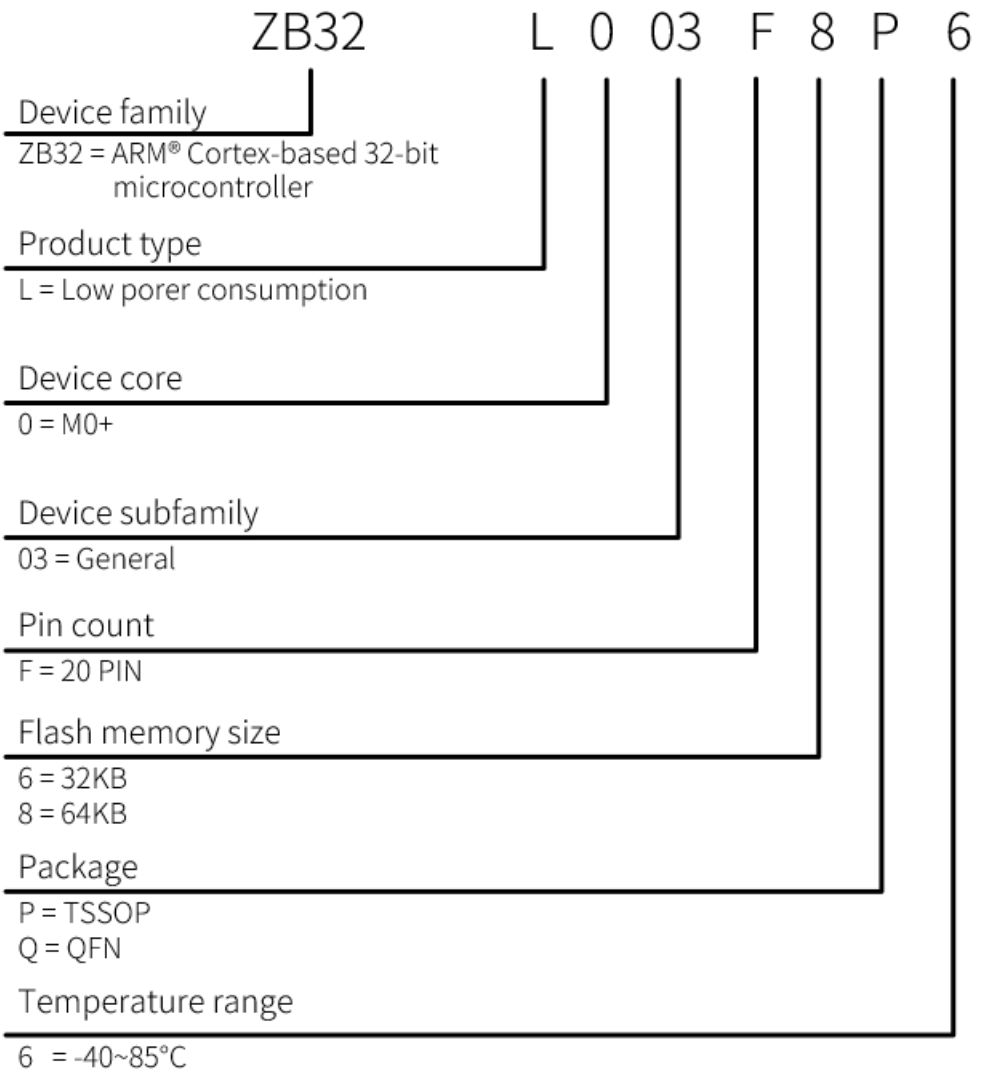
6.3-1 TSSOP20

1. The first line: the 1st to 10th characters of the product model, refer to Chapter 7 for details.
2. The second line: the first 6/7 digits represent the Lot ID, and the last 1 digit represents the product version.
3. The third line: the first 4 digits represent the year and week of production, and the 5th digit represents the packaging and testing factory.

6.3-2 QFN20(3x3)

1. The first line: ZB+ characters from the 6th to the 10th of the product model, refer to Chapter 7 for details.
2. The second line: the first 6/7 digits represent the Lot ID, and the last 1 digit represents the product version.
3. The third line: the first 4 digits represent the year and week of production, and the 5th digit represents the packaging and testing factory.

【7】 Product Naming Rule



【8】 Product Selection Table

Model	Flash (KB)	SRAM (KB)	Encapsulation	Package	Minimum Packing Quantity (MPQ)	Minimum order quantity (MOQ)
ZB32L003F8Q6T	64	4	QFN20	Tape & Reel	5000	40000
ZB32L003F8P6T	64	4	TSSOP20	Tape & Reel	4500 note (1)	72000

Note:

1. Try to arrange 9000 as the minimum delivery unit.
2. Please contact a sales representative.

【9】 Revision History

Version	Revision date	Summary of revisions
V1.0	2024-0110	Initial Release