Chapter 4

Memory Management

One-mark Questions

1. A system uses FIFO policy for page replacement. It has 4 pages frames with no page loaded to begin with. The system first access 100 distinct pages in some order then access the same 100 pages but now in the reverse order. How many page faults will occur? **[2010]**

(a) 196 (b) 192
(c) 197 (d) 195

Solution: (a)

Given that page frame size = 4.

As there are 100 distinct pages which are first accessed → 100 page fault when it accessed → the same 100 pages but now in the reverse order → (100 – 4), as page frame size is four.

Therefore, Total number of page faults

→ 100 + (100 – 4) = 196

Hence, the correct option is (a).

2. A system uses 3 page frames for storing process pages in main memory. It uses the LRU page replacement algorithm policy. Assume that all the page fault that will occur while processing the page reference string given below. **[2010]**

4, 7, 6, 1, 7, 6, 1, 2, 7, 2

Solution: (6)

Assume pure demand paging initially the first three references causes page fault and from the remaining reference using LRU policy there more page faults occurs making the count to 6.

3. How many 32 Kx1 RAM chips are needed to provided a memory capacity of 256K bytes? **[2009]**

(a) 8 (b) 32
(c) 64 (d) 128

Solution: (c)

Hence, the correct option is (c).

4. In which of the following page replacement policies, Belady's anomaly may occur? **[2009]**

(a) FIFO (b) Optimal
(c) LPU (d) MRU

Solution: (a)

Hence, the correct option is (a).

5. The essential contents in each entry of a page table is/are **[2009]**

(a) Virtual page number
(b) Page frame number
(c) Both virtual page number and page frame number
(d) Access right information

Solution: (b)

Hence, the correct option is (b).

6. What is the swap space in the disk used for? **[2005]**

(a) Saving temporary html pages
(b) Saving process data
(c) Storing the super – block
(d) Storing device drivers

Solution: (b)

Hence, the correct option is (b).

7. Consider a program P that consists of two source modules M1 and M2 contained in two different files. If M1 contains a reference to a function defined in M2, the reference will be reSolutionved at **[2004]**

(a) Edit time (b) compile time
(c) Link time (d) Load time

Solution: (c)

Hence, the correct option is (c).

8. Which of the following addressing modes are suitable for program relocation at run time? **[2004]**

i) AbSolution addressing
ii) Based addressing
iii) Relative addressing
iv) Indirect addressing

(a) i & iv (b) i & ii
(c) ii & iii (d) i,ii & iv

Solution: (c)

Hence, the correct option is (c).

9. The minimum number of page frames that must be allocated to a running process in a virtual memory environment is determined by **[2004]**

(a) the instruction set architecture
(b) page size
(c) physical memory size
(d) number of processes in memory

Solution: (a)

Hence, the correct option is (a).

10. In a system with 32 bit virtual addresses and 1 KB page size, use of one – level tables for virtual to physical address translation is not practical because of **[2003]**

(a) the large amount of internal fragmentation.
(b) the large amount of external fragmentation .
(c) the large memory overhead in maintaining page tables.
(d) the large computation overhead in the translation process.

Solution: (c)

Hence, the correct option is (c).

11. Which of the following is not form of memory? **[2002]**

(a) Instruction cache
(b) Instruction register
(c) Instruction opcode
(d) Translation look aside buffer

Solution: (c)

Hence, the correct option is (c).

12. The optimal page replacement algorithm will select the page that. **[2002]**

(a) Has not been used for the longest time in past.
(b) Will not be used for the longest time in the future.
(c) Has been used for the least number of times.
(d) Has been used for the most number of times.

Solution: (b)

Hence, the correct option is (b).

13. Which of the following statements are FALSE? **[2001]**

(a) Virtual memory implements the translation of program's address space in to physical memory address space.
(b) Virtual memory allows each program to exceed the size of the primary memory.
(c) Virtual memory increases the degree of multiprogramming.
(d) Virtual memory reduces the context switching overhead.

Solution: (a and b)

Hence, the correct option is (a and b).

14. The process of assigning the load address to the various part of the program and adjusting the code and data in the program to reflect the assigned address is called **[2001]**

(a) Asembly
(b) Parsing
(c) Relocation
(d) Symbol resolution

Solution: (c)

Hence, the correct option is (c).

15. Consider a virtual memory system with FIFO page replacement policy. For an arbitrary page access pattern, increasing the number of page frames in main memory will **[2001]**

(a) always decrease the number of page faults,
(b) always increase the number of page faults,
(c) sometimes increase the number of page fault ,
(d) never affect the number of page fault,

Solution: (c)

due to Balady anomaly.

Hence, the correct option is (c).

15. In a resident OS computer, which of the following system software must reside in the main memory under all situations? **[1998]**
(a) Assembler (b) Linker
(c) Loader (d) Compiler

Solution: (c)

A loader is used to load the program and data on to memory and will reside in main memory.

Hence, the correct option is (c).

16. Locality of reference implies that the page reference being made by a process **[1997]**
(a) will always be to the page used in previous page reference.
(b) is likely to be to one of the pages used in last few pages reference.
(c) will always be to one of the pages existing in memory.
(d) will always lead to page fault.

Solution: (b)

Localty of reference also known as the principal of locality is the phenomena of the same value storage location being related storage location frequency.

Hence, the correct option is (b).

17. Thrashing **[1997]**
(a) Reduces page I/O
(b) Decrease the degree of multiprogramming
(c) Implies excessive page I/O
(d) Improve the system performance

Solution: (c)

In thrasing, paging activity is more as compared to execution.

Hence, the correct option is (c).

18. Dirty bit for page in a page table **[1997]**
(a) helps avoid unnecessary writes on paging device.
(b) helps maintain LRU information.
(c) allows only read on a page.
(d) None of the above

Solution: (a)

Dirty bit indicates whether page is clean or modified.

Hence, the correct option is (a).

19. A ROM is used to store the table for multiplication of two 8 bits unsigned integers. The size of ROM required is **[1996]**
(a) 256×16 (b) $64K \times 8$
(c) $4K \times 16$ (d) $64K \times 16$

Solution: (d)

The size of ROM required is $64K \times 16$.

Hence, the correct option is (d).

20. The principal of locality justifies the use of **[1995]**
(a) Interrupts (b) DMA
(c) Polling (d) Cache memory

Solution: (d)

Hence, the correct option is (d).

21. In a paged segmented scheme of memory management, the segment table itself must have a page table because: **[1995]**
(a) The segment table is often too large to fit in one page
(b) Each segment is spread over number of pages.
(c) Segment tables point to page table and not to the physical locations of the segment.
(d) The processor's description base register points to a page table.

Solution: (a)

Segment table must be paged in order to be accommodates in one page.

Hence, the correct option is (a).

22. A linker is given object modules for a set of programs that were compiled separately. What information need to be included in an object module? **[1995]**
(a) Object code
(b) Relocation bit
(c) Names and locations of all external symbols defined in the object module
(d) Absolute addresses of internal symbols

Solution: (d)

Hence, the correct option is (d).

23. Which page replacement policy sometimes leads to more page fault when size of memory is increased? **[1992]**
(a) Optimal (b) LPU
(c) FIFO (d) None of these

Solution: (c)

Belady's anamaly: When we increase the number of page frames while using FIFO page replacement algorithm, the number of page fault will also increase.

Hence, the correct option is (c).

Two-marks Questions

1. Consider the virtual page reference string **[2014]**

1, 2, 3, 4, 1, 3, 2, 4, 1

On demand paged virtual memory system running on a computer system that has main memory size of 3 page frames which are initially empty. Let LRU, FIFO and OPTIMAL denote the number of page faults under the corresponding page replacement policy, then

(a) Optimal < LRU < FIFO
(b) Optimal< FIFO < LRU
(c) Optimal = LRU
(d) Optimal = FIFO

Solution: (b)

Hence, the correct option is (b).

2. Assume that there are 3 page frames which are initially empty. If the page reference string is 1, 2, 3, 4, 2, 1, 5, 3, 2, 4, 6, then the number of page fault using the optimal replacement policy is_____ **[2014]**

Solution: (7)

Applying pure demand paging the first three references causes page – faults, and therefore from the remaining reference by applying optimal replacement where in that page is selected which will not be referred for the longest duration of time in the future.

3. A computer has twenty physical page frames which contains page numbered 1, 2,….,100 in that order and repeats the access sequence thrice. Which one of the following page replacement policies experiences the same number of page faults as the optimal page replacement policy for this program? **[2014]**

(a) LRU
(b) FIFO
(c) LIFO
(d) Most recently used

Solution: (d)

Initially the first 20 references will cause fault replacing the page in order from 101 – 120. This is just like fault without replacement. Thereafter, the next page fault is for page number 21 which should result in replacing the page 20 as it is the last one to occur once the pattern is repeated thrice. Same thing happens in the case of MRU.

Hence, the correct option is (d).

4. Consider a paging hardware with TLB. Assume that the entire page table and all the pages are in the physical memory. It takes 10 ms to search the TLB and 80 ms to access the physical memory. If the TLB hit ratio is 0.6, the effective memory access time (in ms) is _____ **[2014]**

Solution: (123)

EMAT = $x\,(c + m) + (1 - x)\,c + 2m$;

where $c = 10$, $m = 80$, $x = 0.6$ generates 122 ms.

5. A multi level page table is preferred in comparison to a single level page table for translating virtual address to physical address because **[2009]**

(a) it reduces the memory access time to read or write a memory location.
(b) it helps to reduce the size of page table needed to implement the virtual address space of a process.
(c) it is required by the translation look aside buffer.
(d) it helps to reduce the number of page faults in page replacement algorithms.

Solution: (b)

The basic objective of multi – level paging is to reduce the page table size overhead. A multi level page table saves space over a single page table because only the parts that are need to be allocated. As the most processes only use a small fraction of the address space, only a small fraction of the page table needs to be allocated.

Hence, the correct option is (b).

6. Consider the virtual page reference string **[2009]**

1, 2, 3, 2, 4, 1, 3, 2, 4, 1

On demand paged virtual memory system running on a computer system that has main memory size of 3 page frames which are initially empty. Let LRU, FIFO and OPTIMAL denote the number of page faults under the corresponding page replacement policy, then

(a) Optimal < LRU < FIFO
(b) Optimal< FIFO < LRU
(c) Optimal = LRU
(d) Optimal = FIFO

Solution: (b)

The given string is

1, 2, 3, 2, 4, 1, 3, 2, 4, 1

Optimal 1, 2, 3, 2, 4, 1, 3, 2, 4, 1

1	1	1	1	1	1	1	1	1	1
	2	2	2	4	4	4	4	4	4
		3	3	3	3	3	2	2	2
F	F	F	F			F			

Page fault = 5

LRU 1, 2, 3, 2, 4, 1, 3, 2, 4, 1

1	1	1	1	4	4	4	2	2	2
	2	2	2	2	2	3	3	3	1
		3	3	3	1	1	1	4	4
F	F	F	F	F	F	F	F	F	

Page fault = 8

FIFO 1, 2, 3, 2, 4, 1, 3, 2, 4, 1

1	1	1	1	4	4	4	4	4	4
	2	2	2	2	1	1	1	1	1
		3	3	3	3	3	2	2	2
F	F	F		F	F	F			

Page fault = 6

From the above Solution if we consider the page faults

OPTIMAL < FIFO < LRU

Hence, the correct option is (b).

7. A processor used 36 bit physical addresses and 32 bit virtual addresses, with a page frame size of 4KB. Each page table entry is of size 4 bytes. A three level page table is used for virtual to physical address translation, where the virtual address is used as follows: **[2008]**

- Bits 30 are used to index into the first level page table.
- Bits 21 are used to index into second level page table.
- Bits 12 are used to index into third level page table.
- Bits 0 are used as offset within the page.

The number of bits required for addressing the next – level page table(or page frame) in the page table entry of the first, second and third level page tables are, respectively

(a) 20, 20 and 20 (b) 24, 24 and 24
(c) 24, 24 and 20 (d) 25, 25 and 24

Solution: (b)

Number of bits required for first lent = 24

Number of bits required for second lent = 24

Number of bits required for third lent = 24

Hence, the correct option is (b).

8. A virtual memory system uses FIFO page replacement policy and allocates a fixed number of frames to a process. Consider the following statements:

P: Increasing the number of page frames allocates to a process sometimes increases the page fault rate. **[2007]**

Q: Some programs do not exhibit locality of reference.

Which of the following is TRUE?

(a) Both P & Q are true, and Q is the reason for P.
(b) Both P and Q are true, but Q is not the reason for P.
(c) P is false but Q is true.
(d) Both P and Q are false.

Solution: (b)

Hence, the correct option is (b).

Common Data for Question 9 and 10

A process has been allocated 3 page frames. Assume that none of the pages of the process are available in memory initially. The process makes the following sequence of page reference (reference string):

1, 2, 1, 3, 7, 4, 5, 6, 3, 1

9. If optimal page replacement policy is used, how many page faults occur for the above reference string? **[2007]**

(a) 7 (b) 8
(c) 9 (d) 10

Solution: (a)

Given the reference string

1, 2, 1, 3, 7, 4, 5, 6, 3, 1

1, 2, 1, 3, 7, 4, 5, 6, 3, 1

1	2	1	3	7	4	5	6	3	1
1	1	1	1	1	1	1	1	1	1
	2	2	2	7	4	5	6	6	6
			3	3	3	3	3	3	3
F	F	F	F	F	F	F			

Total number of page fault: = 7.

Hence, the correct option is (a).

10. Least Recently Used (LRU) page replacement policy is practical approximation to optimal page replacement. For the above reference string, how many more page fault occur with LRU than with the optimal page replacement policy?

(a) 0 (b) 1
(c) 2 (d) 3

Solution: (c)

Given the reference String

1, 2, 1, 3, 7, 4, 5, 6, 3, 1

1	2	1	3	7	4	5	6	3	1
1	1	1	1	1	4	4	4	3	3
	2	2	2	7	7	7	6	6	6
			3	3	3	5	5	5	1
F	F	F	F	F	F	F	F	F	

Total number of page fault: = 9.

Page fault in LRU – page fault in Optimal = 9 – 7 = 2

Hence, the correct option is (c).

11. A computer system supports32 bit virtual addresses as well as 32 bit virtual addresses. Since the virtual address space is of the same size as the physical address apace, the operating system designers decide to get rid of the virtual memory entirely. Which one of the following is true? **[2006]**

(a) Efficient implementation of multi user support is no longer possible.
(b) The processor cache organization can be made for more efficient now.
(c) Hardware support for memory management is no longer needed.
(d) CPU scheduling can be made more efficient now .

Solution: (c)

Hence, the correct option is (c).

12. Consider a system with a two level paging scheme in which a regular memory access takes 150 nanoseconds, and servicing a page fault takes 8 ms. An average instruction takes 100 ns of CPU time, and two memory access. The TLB hit ratio is 90% and the page fault rate is one in every 10,000 instructions. What is the effective average instruction execution time? **[2004]**

(a) 645 ns (b) 1050 ns
(c) 1215 ns (d) 1230 ns

Solution: (a)

Effective instruction time = 100ns + 2 * EMAT ~ 640 ns

EMAT = 0.9 (150ns) + 0.1

[10 ^ – 4*8ms + (1 – 10 ^ – 4)*300 ns]

Hence, the correct option is (a).

Common Data For Questions 13 and 14 [2003]

A processor uses 2 level page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both 32 bits wide. The memory is byte addressable. For virtual to physical address translation, the 10 most significant bits for the virtual address are used as index into the first level page table while the next 10 bits are used as index into the second level page table. The 12 significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both level of page tables are 4 bytes wide. Further, the processor has a translation look aside a buffer with a hit rate of 96%. The TLB caches recently used virtual page numbers and the corresponding virtual page numbers. The processor also has a physical address cache with a hit rate of 90%. Main memory access time is 10ns, cache success time is 1ns, and TLB access time is also 1ns.

13. Assuming that no page fault occur, the average time taken to access a virtual address is approx(to the nearest)

(a) 1.5 ns (b) 2 ns
(c) 3 ns (d) 4 ns

Solution: (d)

EMAT = 0.96 [1ns + 0.9 (1 ns) + 0.1 (1 ns + 10 ns)] + 0.04

[1ns + 10 ns + 10 ns + 0.9 (1ns) + 0.1(1ns + 10ns)]

EMAT = 0.96 [1ns + 0.9 (1ns) + 0.1 (1ns + 10ns)] + 0.04 [1ns + 10ns + 10ns + 0.9 (1ns) + 0.1 (1ns + 10ns)]

Hence, the correct option is (d).

14. Suppose a process has only the following pages in its virtual address space: two contiguous code pages starting at virtual address 0x00000000, two contiguous data pages starting at virtual address 0x00400000 and a stack page starting at virtual address 0xFFFFF000. The amount of memory required for storing the page tables of this process is

(a) 8 KB (b) 12 KB
(c) 16 KB (d) 20 KB

Solution: (c)

First level page table size = 4KB in the second level, we require 3 pages of the inner page table. One for the code, another for data and last one for stack. Sizes of each page is 4KB; outer page table is also 4\KB.

Hence, the correct option is (c).

15. Which of the following is not an advantage of using statically linked libraries as opposed to using statically linked libraries? **[2003]**

(a) Smaller size of executable files.
(b) Lesser overall page fault rate in the system.
(c) Faster program startup.
(d) Existing programs need not be re – linked to take advantage of newer versions of libraries.

Solution: (b)

Page fault rate may increase due to dynamic locality

Hence, the correct option is (b).

16. Dynamic linking can cause security concerns because **[2002]**

(a) security is dynamic.
(b) the path for searching dynamic libraries is not known till runtime.
(c) linking is insecure.
(d) cryptographic procedures are not available for dynamic linking.

Solution: (b)

Linking is done at runtime.

Hence, the correct option is (b).

17. Consider a machine with 64MB physical memory and a 32 – bit virtual address space. What is the approximate size of the page table? **[2001]**

(a) 16 MB (b) 8 MB
(c) 2 MB (d) 24 MB

Solution: (c)

Hence, the correct option is (c).

18. Suppose the time to service a page fault is on the average 10 milliseconds, while a memory access takes 1 microsecond. Then the 99.99% hit ratio results in average memory access of time. **[2000]**

(a) 1,9999 ms (b) 1 ms
(c) 9999 ms (d) 1,9999 ms

Solution: (d)

By using formula EMAT = $P \times S + (1 - p)\, m$

Where P is the page fault rate and S is the page fault service line m is main memory access time.

Hence, the correct option is (d).

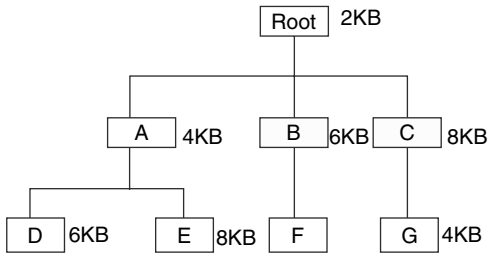
19. Which of the following is/are advantages of virtual memory? **[1999]**

(a) Faster access to memory on an average.
(b) Processes can be given protected address space.
(c) Linker can assign addresses independent of where the program will be loaded in physical memory.
(d) Programs larger than the physical memory size can be run.

Solution: (b and d)

Hence, the correct option is (a and d).

20. The overlay tree for a program is shown below: **[1998]**



What will be the size of the partition (in physical memory) required to load (and run) this program?

(a) 12KB (b) 14KB
(c) 10KB (d) 8KB

Solution: (b)

Hence, the correct option is (b).

21. If an instruction takes i microsecond and page fault takes an additional j microseconds, the effective instruction time if on the average a page fault occurs every k instruction is: **[1998]**

(a) $i + (j/k)$ (b) $i + j*k$
(c) $(i + j)/k$ (d) $(i + j)*k$

Solution: (a)

Use the formula for eff. Inst. Time = p*time with page fault + $(i - p)$*time without page fault.

Hence, the correct option is (a).

22. A 1000 Kbyte memory is managed using variable partition but to compaction. It currently has two partition of sizes 200Kbytes and 260Kbytes, respectively. The smallest allocation request in Kbytes that could be denied for **[1996]**

(a) 151 (b) 181
(c) 231 (d) 541

Solution: (d)

Remaining all are satisfiable in one or the other partition, but 541 is never satisfiable.

Hence, the correct option is (d).

23. The capacity of memory units is defined by the number of works multiplied by the number of bits/work. How many separate address and data lines are needed for a memory of 4K × 16? **[1995]**

(a) 10 address, 16 data lines
(b) 11 address, 8 data lines
(c) 12 address, 16 data lines
(d) 12 address, 12 data line

Solution: (c)

Memory specification = No. of words × width of word.

Hence, the correct option is (c).

24. The address sequence generated by tracing a particular program executing in a pure demand paging system with 100 records per page with 1 free main memory frame is recorded as follows. What is the number of page faults? **[1995]**

0100, 0200, 0430, 0499, 0510, 0530, 0560, 0120, 0220, 0240, 0260, 0320, 0370

(a) 13 (b) 8
(c) 7 (d) 10

Solution: (c)

Find the reference string first the number of page fault = length of reference string in this case as the number of frames is one.

Find the reference string first:

It is 1, 2, 4, 5, 1, 2, 3

The number of page fault = length of reference string in this case as the no. of frame is one.

Hence, the correct option is (c).

25. In a virtual memory system, the address space specified by the address lines of the CPU must be……. than the physical memory size…….. than the secondary storage size. **[1995]**

(a) Smaller, smaller (b) Smaller, larger
(c) Larger, smaller (d) Larger, larger

Solution: (c)

Hence, the correct option is (c).

26. A memory page containing a heavily used variable, that was initialized very clearly and is in constant use, is removed when **[1994]**

(a) LRU, page replacement algorithm is used
(b) FIFO, page replacement algorithm is used
(c) LFU, page replacement algorithm is used
(d) None of the above

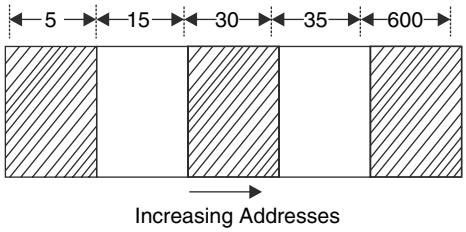
Solution: (b)

Initialized early means, it is FCFS.

If FIFO page replacement algorithm is used, then a memory page containing a heavily used variable that was initialized very early and is in constant use is removed.

Hence, the correct option is (b).

27. Consider the following heap(figure) in which blank regions are not in use and hatched regions are in use. **[1994]**



The sequence of requests for blocks of size 300, 25, 12550 can be satisfied if we use:
(a) Either first fit or best fit
(b) First fit but not best fit policy
(c) Best fit but first fit policy
(d) None of the above

Solution: (b)

Using first fit, all the requests will be satisfied. But best fit will not satisfy the last request as the memory is not contagious. The optimal page replacement algorithm will select the page that will not be used for the longest time in future.

Hence, the correct option is (b).

28. A Simple two pass assembler does the following in the first pass: **[1993]**
(a) It allocates space for the literals.
(b) It computes the total length of the program.
(c) It builds the symbol table for the symbol and their value.
(d) It generates code for all the load and store register instruction.

Solution: (c)

Hence, the correct option is (c).

29. A part of the system software, which under all circumstances, must reside in the main memory is **[1993]**
(a) Text editor (b) Assembler
(c) Linker (d) Loader

Solution:(d)

Loader is frequently required system software.

Hence, the correct option is (d).

30. Match the pairs in the following question **[1991]**

GROUP–I
(A) Buddy system (B) Interpretation
(C) Pointer type (D) Virtual memory

GROUP–II
(p) Run – time type specification
(q) Segmentation
(r) Memory allocation
(s) Garbage collection

Solution: (A – r, B – p, C – s, D – q)

31. The total size of address space in a virtual memory system is limited by **[1991]**
(a) the length of MMR.
(b) the available secondary storage .
(c) the available main memory.
(d) All of the above.

Solution: (b)

Virtual memory is implemented on secondary storage.

Hence, the correct option is (b).

32. The 'link editor' is a program that: **[1991]**
(a) Matches the parameters of micro definition with locations of parameters of the micro call.
(b) Matches external names of one of the program with their location in other programs.
(c) Matches the parameters of subroutine definition with locations of parameters of the subroutine call.
(d) Acts as link between text editor and the user.
(e) Acts as link between compiler and user program.

Solution: (b)

Hence, the correct option is (b).

33. Indicate all the FALSE statement from the statements given below. **[1991]**
(a) The amount of virtual memory available is limited by the availability of secondary storage
(b) Any implementation of a critical section requires the use of an indivisible machine – instruction such as test and set.
(c) The use of monitors ensures that no deadlock will be caused.
(d) The LRU page – replacement policy may cause thrashing for some type of programs.
(e) The best fit techniques for memory allocation ensures the memory will never be fragmented.

Solution:

(a): True

(b): False

(c): True

(d): True

(e): False

34. State whether the following statements are TRUE/FALSE with reason. **[1990]**

Transferring data in blocks from the main memory unit to the cache memory enables an inter – leaved main memory unit to operate units at its maximum.

Solution: (TRUE)

35. State whether the following statements are TRUE/ FALSE with reason. **[1990]**

The link load and go loading scheme requires less storage space than the link – and – go loading scheme.

Solution: (TRUE)

36. In a two level virtual memory. The memory access time for main memory $t_{A1} = 10^{-8}$ sec, and the memory access time for secondary memory, tag = 10^{-8}. What must be the hit ratio H, such that the access efficiency is within 80 percent of its maximum value? **[1990]**

Solution:

Hit ratio must be less than or equal to 80% in order to ensure that the access efficiency is within 80% of its maximium value.

37. Under paged memory management scheme, simple lock and key memory protection arrangement may still be required if the …… processors do not have address mapping hardware. **[1990]**

Solution: (input/output)

38. Match the following. **[1990]**

GROUP – I

(a) critical region (b) Wait/signal
(c) Working set (d) Deadlock

GROUP – II

(p) Hoare monitor (q) Mutual exclusion
(r) Principle of locality (s) Circular wait

Solution: (a – q, b – p, c – r, d – s)

39. Match the following. **[1989]**

GROUP – I

(a) Virtual memory
(b) Shared memory
(c) Look ahead buffer
(d) Look aside buffer

GROUP – II

(p) Temporal locality
(q) Spatial locality
(r) Address translation
(s) Mutual exclusion

Solution: (a – q, b – s , c – p, d – r)

Five-marks Questions

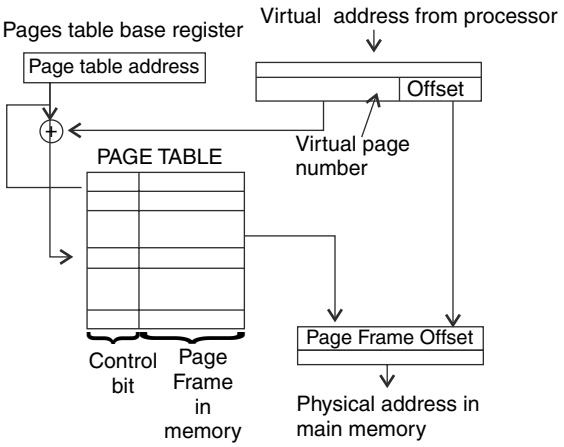
1. A computer system uses 32 bit virtual address, 32 bit physical address. The physical memory is byte addressable, and to page size is 4k bytes. It is decided to use two level page table to translate from virtual address to physical address. Equal number of bits should be used for indexing first level and second level page table, and the size of each page table entry is 4 bytes. **[2002]**

(a) Give a diagram showing how a virtual address would be translated into physical address.

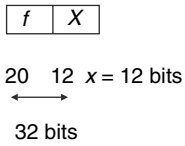
(b) What is the number of page table entries that can be contained in each page?

(c) How many bits are available for storing protection and other information in each page table entry?

Solution: (a)



(b) $2^{10} = 1K$



Hence, the correct option is (a)

2. A certain computer system has segmented paging architecture for virtual memory. The memory is byte addressable. Both virtual and physical address spaces contain 2^{16} bytes each. The virtual address space is achieved is divided in 8 non overlapping equal size segments. The Memory Management Unit (MMU) has a hardware segment table, each entry of which contains the physical address of the page table for the segment. Page tables are stored in the main memory and consists of 2 bytes page tables entries. **[1999]**

(a) What is the minimum page size in bytes so that the page table for a segment requires atmost on page to store it? Assume that the page size can only be power of 2.

(b) Now suppose that the page size is 512 bytes. It is proposed to provide a TLB (transaction look – aside buffer) for speeding up address translation. The proposed TLB will be capable of storing page table entries for 16 recently referenced virtual page, in last cache that will use the direct mapping scheme. What is the number of tag bits that will need to be associated with each cache entry ?

(c) Assume that each page table entry contains (besides other information), 1 valid bit, 3 bit for page protection and dirty bit. How many bits are available in a page table entry for storing the aging information of page? Assume that the page size is 512 bytes.

Solution:

Minimum page size = 128 bytes.

Let page size = 2^k Bytes

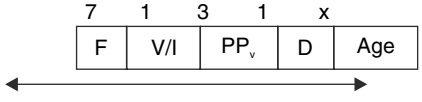
Page table size = 2^{13} = (2^{13-k}) x2 bytes = 2^{14-k} bytes.

by given condition $14 - k = 2^k$, $k = 7$

and page size = 27 = 128 bytes.

(b) Please refer the cache organization in the computer architecture course.

(c)



Page table entry structure

f = frame No. = $2^{16} = 2^7 = 7$ bits.

3. In a computer system where the best – fit algorithm is used for allocating jobs to memory partitions, the following situation was encountered: **[1998]**

Student ID	Student Name	Student Email	Student Age	CP I
2345	Shanker	shankar@math	X	9.4
1287	Swati	swati@ee	19	9.5
7853	Shankar	shankar@ese	19	9.4
9876	Swati	swati@mech	18	9.3
8765	Ganesh	ganesh@civil	10	8.7

When will the 20K job complete?

Solution:

Job 20K completes at 31 use best fit only with fixed partitions and FCFS scheduling. As an alternative, one can try with variable partitions with best available fir and FCFS algorithm.

The 20K partition will be occupied by the 14K job which will require 10 units of time for execution. After its completion the 10K job will be occupying this 20K partition. And on its completion, 20K will be taking up the partition.

Hence total time = 10 + 1 + 8 = 19 units.

Other job will be occupying the other partitions.

4. A demand paged virtual memory system uses 16 bit virtual address, page size of 256 bytes, and has 1K bytes of main memory. LRU page replacement is implemented using a list whose current status (page number in decimal) is **[1996]**

17	1	63

↑

LRU page

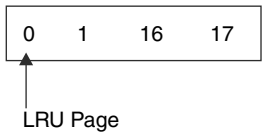
For each hexadecimal address in the address sequence given below, 00FF, 010D, 10FF, 11B0

Indicate,

i) The new status of the list
ii) Page faults, if any, and
iii) Page replacements, if any

Solution:

i) New status of pages in memory



ii) Page fault = 3
iii) Page replacement = 2

For all the above bits, make a note that the page number in decimal are 0, 1, 16, 17 for the given hexadecimal addresses.

5. A computer installation has 1000K of main memory. The jobs arrive and finish in the following sequence. **[1995]**

Job 1 requiring 200k arrives

Job 2 requiring 350k arrives

Job 3 requiring 300k arrives

Job 1 finish

Job 4 requiring 120k arrives

Job 5 requiring 150k arrives

Job 6 requiring 80k arrives

(a) DRAW the memory allocation table using best fit and first fit algorithm.
(b) Which algorithm performs better for this sequence?

Solution:

BEST FIT

	30k
J4	120k
J3	300
J2	
J5	150k

FIRST FIRST

J4	1000k
J6	80k
J2	350k
J3	300k
J5	150k

J6 has to wait.

With first fit, it is possible to satisfy all the requests.

6. The following page addresses, in the given sequence, were generated by a program: **[1993]**

1 2 3 4 1 3 5 2 1 5 4 3 2 3

This program is run on a demand paged virtual memory system, with main memory size equal to 4 pages. Indicate the page reference for which

page faults occur for the following page replacement algorithms:

(a) LRU (b) FIFO

Assume that the main memory is empty initially.

Solution:

(a) 9 Page fault with LRU

(b) 7 page fault with FIFO

Apply given page replacement algorithm to find page faults.

(a) LRU

1	2		3		4	1	3	5	2	1	5	4	3	2	3
1	1	1	4	4	4	5	5	5	5	5	5	2	2		
	2	2	2	1	1	1	2	2	2	4	4	4	4		
		3	3	3	3	3	3	1	1	1	3	3	3		
F	F	F	F		F		F	F	F	F	F	F			

No. of page fault = 11.

(b) FIFO

1	2	3		4	1	3	5	2	1	5	4	3	2	3	
1	1	1	4	4	4	4	4	4	4	4	4	4	4	4	
	2	2	2	1	1	1	2	2	5	5	5	2	2		
		3	3	3	3	5	5	1	1	1	3	3	3		
F	F	F	F	F	F		F	F			F	F	F		

No. of page fault = 11.

7. Let the page reference and working set window be c c d b c e c e a d and 4 respectively. The initial working set at time 1 = 0 contains the pages {*a*, *d*, *e*} where a was referenced at time *t* = 0, *d* was referenced at time *t* = – 1, and *e* – was referenced at time *t* = – 2. Determine the total number of page frames used by computing the working set at each reference. **[1992]**

Solution: Number of page fault = 4

Average number of page frame used are 4.

Chapter 5

File System and Device Management

One-mark Questions

1. Suppose a disk has 201 cylinders numbered from 0 to 200. At some time the disk arm is at cylinder 100, and there is a queue of disk access requests for cylinders 30, 85, 90, 100, 105, 110, 135 and 145. If Shortest Seek Time First (SSTF) is being used for scheduling the disk access, the request for cylinder 90 is serviced after servicing _____ nuber of requests. **[2014]**

(A) 1 (B) 2

(C) 3 (D) 4

Solution: (3)

From the current position 100, it will serve the requests in order 100, 105, 110 and then 90.

2. A based file system is being used and the total overhead of each entry in the FAT is 4 bytes in size. Given a 100×10^6 bytes disk on which the file system is stored and data block size is 103 bytes, the maximum size of a file that can be stored on this disk in units of 10^6 bytes is _____. **[2014]**

Solution: 99.6

number of blocks on the disk is 100×10^3 ;

The size of FAT = $4 \times 100 \times 10^3$.

Bytes = 0.4×10^6 Bytes

Subtracting this value from the size of is the case of size which is 99.6×10^6

3. Assuming P ≠ NP, which of the following is TRUE? **[2012]**

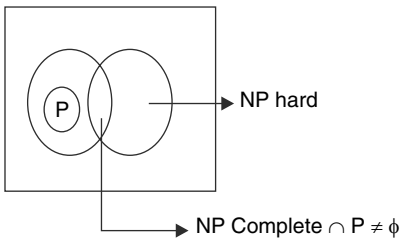
(a) NP - complete = NP

(b) NP - Complete ∩ P = φ

(c) NP - Hard = NP

(d) p = NP - complete

Solution: (b)



Look at the diagram showing the relationship between the class of P, NP and NPH problems for the case when P is not equal to NP;

Hence, the correct option is (b).

4. The data block of a very large file in UNIX file system are allocated using **[2008]**

(a) Contiguous allocation

(b) Linked allocation

(c) Indexed allocation

(d) An extension of indexed allocation.

Solution: (d)

Hence, the correct option is (d).

5. Consider a disk pack with 16 surfaces, 128 tracks per and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively: **[2007]**

(A) 256Mbyte, 19 bits

(B) 256Mbyte, 28 bits

(C) 512Mbyte, 20 bits
(D) 64Gbyte, 28 bits

Solution: (a)

Disk capacity = $16 \times 128 \times 256 \times 512$ MB.

Sector address = $4 + 7 + 8 = 19$ bits.

Hence, the correct option is (a)

6. Normally user programs are prevented from handling I/O directly by I/O instructions in them. For CPUs having explicit I/O instructions, such I/O protection is ensured by having the I/O instructions privileged. In a CPU with memory mapped I/O, there is no explicit I/O instruction. Which one of the following is for a CPU with memory mapped I/O? **[2005]**

(a) I/O protection is ensured by operating system routine(s)
(b) I/O protection is ensured by a hardware trap
(c) I/O protection is ensured during system configuration
(d) I/O protection is not possible

Solution: (a)

Hence, the correct option is (a).

7. Consider an operating system capable of loading and executing a single sequential user process at a time. The head scheduling algorithm is used is First Come First Serve. If FCFS is replaced by Shortest Seek Time First (SSTF), claimed by the vendor to give 50% better benchmark results what is expected improvement in the I/O performance of user programs? **[2004]**

(a) 50% (b) 40%
(c) 25% (d) 0%

Solution: (d)

When there is only one process in the system then the disk scheduling technique has no role.

Hence, the correct option is (d)

8. Using a larger block size in a fixed block size file system leads to **[2003]**

(a) better disk throughput but poorer disk space utilization .
(b) better disk throughput and better disk space utilization.
(c) poorer disk throughput but better disk space utilization.
(d) poorer disk throughput and poorer disk space utilization.

Solution: (a)

Large block size results in more internal fragmentation and reading a larger block results in reading a larger block results in reading more data, and hence higher throughput.

Hence, the correct option is (a)

9. Which of the following require a device driver? **[2001]**

(a) Register (b) Cache
(c) Main memory (d) Disk

Solution: (d)

Hence, the correct option is (d).

10. Listed below are some operating system abstractions (in the left column) and the hardware components. Which matching pairs are correct? **[1999]**

I

(a) Thread
(b) Virtual address space
(c) File
(d) Signal

II

(a) Interrupts (b) Memory
(c) CPU (d) Disk

Solution: (a – 3, b – 2, c – 4, d – 1)

Threads are different simultaneous process in the CPU.

Virtual address space is implemented in memory. The file system is the way in which data in a disk is organized.

A signal is acted upon using the mechanism of interrupts.

11. Which of the following disk scheduling strategies is likely to give the best throughput? **[1999]**

(a) Farthest cylinder next
(b) Nearest cylinder next
(c) First
(d) Elevator algorithm

Solution: (b)

Nearest cylinder next is also known as shortest seek time first which is the optimal algorithm.

Hence, the correct option is (b)

12. Which of the following devices should get higher priority in assigning interrupts? **[1998]**

(a) Hard disk (b) Printer
(c) Keyboard (d) Floppy disk

Solution: (c)

Whatever is typed should be given to the process or displayed on the screen.

Hence, the correct option is (c)

13. Which of the following is? **[1998]**

(a) Unless enabled, a CPU will not be able to process interrupts.
(b) Loop instructions cannot be interrupted till they complete.
(c) A processor checks for interrupts before executing a new instruction.
(d) Only triggered interrupts are possible on microprocessors.

Solution: (a, c)

Hence, the correct option is (a, c).

14. The correct matching for the following pairs is **[1997]**

I
(a) DMA I/O
(b) Cache
(c) Interrupt I/O
(d) Condition code register

II
High speed RAM
Disk
Printer
ALU

(a) a – 4, b – 3, c – 1, d – 2
(b) a – 2, b – 1, c – 3, d – 4
(c) a – 4, b – 3, c – 2, d – 1
(d) a – 2, b – 3, c – 4, d – 1

Solution: (b)

Hence, the correct option is (b).

15. The correct matching for the following pairs are **[1997]**

(a) Disk	(1) Round Robin
(b) Batch processing	(2) SCAN
(c) Time sharing	(3) LIFO
(d) Interrupt Processing	(4) FIFO

(a) a – 3, b – 4, c – 2, d – 1
(b) a – 4, b – 3, c – 2, d – 1
(c) a – 2, b – 4, c – 1, d – 3
(d) a – 3, b – 4, c – 3, d – 2

Solution: (c)

Hence, the correct option is (c).

16. I/O redirection **[1997]**

(a) Implies changing the name of a file
(b) Can be employed to use an existing file as input for a program
(c) Implies connection 2 program through a pipe
(d) None of the above

Solution: (b)

Hence, the correct option is (b).

17. When an interrupts occurs, an OS **[1997]**

(a) Ignore the interrupt
(b) Always changes state of interrupt process after processing the interrupt
(c) Always resumes execution of interrupted process after processing the interrupts
(d) May change state of interrupted processes to 'blocked' and schedule another process.

Solution: (c)

Interrupt process resumes execution of interrupted process after processing the interrupts by OS.

Hence, the correct option is (c)

TWO-MARKS QUESTIONS

1. A system contains three programs and each requires three tape units for its operation. The minimum number of tape units which the system must have such that deadlocks never arise is _____. **[2014]**

Solution: 7

Maximum condition for deadlock to occur is 6.

2. A file system with 300 GB uses a file descriptor with 8 direct block address, 1 indirect block address and 1 doubly indirect block address. The size of each disk block is 128 Bytes and the size of each disk block address is 8 Bytes. The maximum possible file size in this file system is **[2012]**

(A) 3
(B) 35
(C) 280 Bytes
(D) Dependent on the size of the disk

Solution: (b)

Max file size in the file = (8*128 + 16*128 + 16*16*128) Bytes.

Hence, the correct option is (b)

3. An application loads 100 libraries at startup. Loading each library requires exactly one disk access. The seek time of the disk to a random location is given as 10ms. Rotational speed of disk is 6000rpm. If all 100 libraries are loaded from random locations on the disk, how long does it take to load all libraries? (The time to transfer data from the disk block once the head has been positioned at the start of the block may be neglected) **[2011]**

(A) 0.50s (B) 1.50s
(C) 1.25s (D) 1.00s

Solution: (b)

$[10ms + 60s/12000] \times 100$

Hence, the correct option is (b)

4. Consider a disk system with 100 cylinders. The requests to access the cylinders occur in following sequence: 4, 34, 10, 7, 19, 73, 2, 15, 6, 20. Assuming that the head is currently at cylinder 50, what is the time taken to satisfy all requests if it takes 1ms to move from one cylinder to adjacent one and shortest seek time first policy is used? **[2009]**

(A) 95ms (B) 119ms
(C) 233ms (D) 276ms

Solution: (b)

Hence, the correct option is (b).

5. For a magnetic disk with concentric circular tracks, the seek latency is not linearly proportional to the seek distance due to **[2008]**

(a) non-uniform distribution of request.
(b) arm starting and stopping inertia.
(c) higher capacity of tracks on the periphery of the platter.
(d) use of unfair arm scheduling policies.

Solution: (c)

Hence, the correct option is (c).

6. Consider a disk drive with the following specifications: **[2005]**

16 surfaces, 512 tracks/surface, 512 sectors/track, 1KB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is:

(A) 10 (B) 25
(C) 40 (D) 50

Solution: (a)

Time to read 4 bytes word form the wish is 390 ~ 400ns. Which corresponds to 10 memory cycles. Out of 10 memory cycles CPU would be blocked.

Hence, the correct option is (a)

7. In the index allocation scheme of blocks to a file, the maximum possible size of the file depends on **[2002]**

(A) the size of the blocks, and the size of the address of the blocks.
(B) the number of blocks used for the index, and the size of the blocks.
(C) the size of the blocks, the number of blocks used for the index, and the size of the address of the blocks.
(D) None of these.

Solution: (c)

Hence, the correct option is (c).

8. Formatting a floppy disk refers to **[1998]**

(a) the data on the disk in contiguous fashion.
(d) the directory.
(c) the system area.
(c) identification information on all tracks and sectors.

Solution: (d)

Hence, the correct option is (d).

9. If the disk in (a) is rotating at 3600rpm, determine the effective data transfer rate which is defined as the of bytes transferred per second between disk and memory. **[1995]**

Solution: 4.8MB/S

10. A certain moving arm disk storage with one head has following specifications: Number of tracks/recording surface = 200 disk rotation speed = 2400 rpm track storage capacity = 62500 bits **[1993]**

The average latency of the device is P msec and the data transfer rate is Q bits/sec.

Write the value of P & Q.

Solution: P – 12.5 ms; Q = 0.3125 MB/S

11. The root directory of a disk should be placed: **[1993]**

(a) At a fixed address in main memory
(b) At a fixed location on the disk
(c) Anywhere on the disk
(d) At a fixed location on the system disk

Solution: (b)

To facilitate/ minimize the disk access time.

Hence, the correct option is (b)

12. State whether the following statements are True or False with reason. **[1990]**

The data transfer between memory and I/O devices using programmed I/O is faster than interrupt - driven I/O.

Solution: False

13. Disk request come to disk driver for cylinders 10, 22, 20, 2, 40, 56 and 38 in that order at a time when the disk drive is reading from cylinder 20. The seek time is 6 msec peer cylinder. Compute the total seek time if the disk arm scheduling algorithm is **[1989]**

(a) FCFS

(b) Closest cylinder next

Solution:

(a) FCFS 876msec

(b) Closest cylinder next - 360 msec.

14. On receiving an interrupt from an I/O device, the CPU **[1987]**

(a) halts for predetermined time.

(b) branches off to the interrupt service routine after completion of the current instruction.

(c) branches off to the interrupt service routine immediately.

(d) hands over control of address bus and data bus to the interrupting device.

Solution: (d)

Hence, the correct option is (d).

Five-marks Questions

1. Consider a disk with following specification: 20 surfaces, 1000 tracks/surface, 16 sectors/track, data density 1KB/sector, rotation speed 3000rpm. The operating system initiates the transfer between the disk and the memory sector-wise. Once the head has been placed on the right track, the disk reads a sector in a single scan. It reads bits from bits from the sector while the head is passing over the sector. The read bits are formed into bytes in a serial = in parallel–out buffer and each byte is then transferred to memory. The disk writing is exactly a complementary process. For part (c) and (d) below, assume memory read - write time = 0.1 microsecond /byte, interrupt driven transfer has an interrupt overhead – 0.4 micro-second, the DMA initialization and termination overhead is negligible compared to the total sector transfer time. DMA requests are always granted. **[2001]**

(a) What is the total capacity of the disk?

(b) What is data transfer rate?

(c) What is the percentage of time the CPU is required for this disk I/O for byte - wise interrupt driven transfer?

(d) What is the maximum percentage of time the CPU is held up for this disk I/O for cycle - stealing DMA transfer?

Solution:

Disk capacity : $20 \times 1000 \times 16 \times 1Kb \sim 500MB$

Trash = 16 KB; rpm = 3000; D.T.R. = 800KB/S

Almost 25% the total time CPU spend on transfer is 0.5 μs for total time of 13μs.

Almost 5.4% time for reading one sector is 1250μs time to copy the section to memory is 100μs.

2. Consider a disk with the 100 tracks numbered from 0 to 99 rotating at 3000rpm. The number of sectors per track is 100. The time to move the head between two successive tracks is 0.2 milliseconds. **[2001]**

(a) Consider a set of disk requests to read data from tracks 32, 7, 45, 5 and 10. Assuming that the elevator algorithm is used to schedule disk requests and the head is initially at track 25 moving upn (towards large track numbers). What is the total seek time for servicing the requests?

(b) Consider an initial set of 100 library disk requests and assume that no new disk requests arrive while servicing these requests. If the head is initially at track 0 and the elevator algorithm is used to schedule disk requests, what is the worst case time to complete all the requests?

Solution:

(a) 34ms; (100 – 25) = (100 – 5) = 170 secs. ST = 170 × 0.2 = 34ms

(b) Time for worst case request = 100 × 0.2ms = 20ms

Time for one request = S.T + L.T + T.T

= 20 + 10 + 0.2 ms = 30.2 ms

Time for all 100 requests

= 100 × 30.2 ms

= 3020ms = 3.02 seconds.

3. A file system with a one-level directory structure is implemented on a disk with disk block size of 4KB. The disk is used as follows: **[1996]**

Disk-block 0: File allocation , consisting of one 8 bit entry per date block the data block address of the next data block in the file:

Disk block 1: Directory, with on 32 bit entry per file:

Disk block 2: Data block 1;

Disk block 3: Data block 2; etc

(a) What is the maximum possible number of files?

(b) What is the maximum possible file size in blocks?

Solution:

No. of files = 4KB/4B = 1K

As there must be one directory entry per file,

number of files

= Directory size/Directory entry size

= 4KB/ 32B = 1024

(b) Maximum possible = $2^8 – 2 = 254$ block file size

A single file can occupy at most as many data blocks as can be addressed by 8 bit FAT entries.

Number of distinct FAT entry representative = $2^8 = 256$.

As some x of these representative must be used to indicate end of file, unusual block, bad block etc.

Maximum possible file size

$= 256 - x$ blocks, For block of small x,

or, (256 – x) * 4 bytes.

4. If the overhead for formatting a disk is 96 bytes for 40000 bytes sector. Compute the unformatted capacity of the disk of the following parameters: **[1995]**

Number of surfaces = 8

Outer diameter of the disk = 12cm

Inner diameter of the disk = 4cm

Inner trace space = 0.1mm

Number of sectors per track = 20

Solution:

No of tracks = (6 – 2)cm = 400

0.1mm inner track space surface capacity = 400*20*4096

Disk capacity = $8 \times 400 \times 200 \times 40 \times 4096$ Bytes = 4GB

5. The head of a moving head disk with 100 tracks numbered 0 to 99 is currently serving a request at track 55. If the queue of requests kept in FIFO order is 10, 70, 75, 23 and 65, which of two disk scheduling algorithm FCFS and SSTF (Shortest Seek Time First) will require less head movement? **[1995]**

Find the total head movement for each of the algorithm.

Solution:

SSTF: 85 movements

FIFO: 199 seeks

SSTF performs better.

6. A certain moving arm disk-storage device has the following specifications: **[1990]**

Number of tracks per surface = 4004

Track storage capacity = 130030

Disk speed = 3600rpm

Average seek time = 30m secs

Estimate the average latency the disk storage capacity and the data transfer rate.

Solution:

Disk capacity is approx 1.2MB

Latency time is 9ms.

Date transfer rate is around 7000 Bytes/sec.

7. Assuming the current disk cylinder to be 50 and the sequence for cylinders to be 1, 36, 49, 65, 53, 1, 2, 3, 20, 55, 16, 65 and 78 **[1990]**

Find the sequence of servicing using

(i) Shortest Seek Time First

(ii) Disk scheduling policies.

Solution:

i) SSTF: 49, 53, 55, 65, 78, 36, 20, 16, 12, 3, 1

ii) Elevator: 53, 55, 65, 78, 49, 36, 20, 12, 3, 1