21st CSEC – Past Year Paper Solution (2020 – 2021 Semester 2)
CE/CZ 1106 – Computer Organization and Architecture

1 (a) (i) The main function of the 64Mbyte NAND flash in the system is as the storage memory. It contains all code/data of all program and data in the computer system.

(ii) Cache acts as a buffer between the SRAM and the CPU. Cache speed up accesses by storing/fetching recently used data so that it potentially improves the overall system performance.

(iii) It has 1000mAh battery that can last for 6 months. The average current consumption of the Trace Together Token is:
1000mAh / (6 months * 30 days * 24 hours) = 0.2315 mA

(iv) The flash type would be the NOR flash. As NOR flash supports XIP (execute in place), it would be suitable to make on-chip Flash.

(b) (i) Baud rate of the transmitter is 4800 bps. Hence, it transfers 4800 bits per second, so the time duration of one UART bit captured in the oscilloscope is 1 bit / 4800 bits per second = 0.00021 s.

(ii) Since the UART receiver is wrongly configured to 9600 bps. It will read every UART bits twice. UART configuration used is 7O1 (one packet is 10 bits). Using this information, we can assume that the first 5 bits sent by the transmitter is received as one packet by the receiver. Starting from the start bit (0) and the other 4 bits will be, 0x01100 will be read as 0x0011110000.

The error of the first data sampled is the stop bit is zero (should be one) and the odd parity scheme (it has even number of ones)

(iii) The second data sampled is the last 5 bits.
Starting from the 6th bits, 0x10111 will be read as 0x1100111111.

The error of the second data sampled is the start bit is one (should be zero) and the odd parity scheme (it has even number of ones)

(c) (i) The first element is stored at locations starting from virtual memory address 0x01111. The virtual memory address requires 20 bits, and the physical memory address requires 16 bits. The virtual page number requires 10 bits, leaving another 10 bits for the offset for the virtual memory address. The number of bits of the offset must not change, thus, 6 bits are used for the physical frame number.

For the first element, the address would be 0x01111, in binary, 0b0000 0001 0001 0001 0001 => first 10 bits are the virtual page number, and the last 10 bits will be the offset. The first 10 bits will be 4 in decimal and from the page table, virtual page 4 will be pointing to physical frame 1. Hence, we will need to erase the first 4 bits (since the physical address is only 16 bits), change the 6 bits into 1 in decimal, and leave the offset remain the same. So, in binary, the physical address will be 0b0000 0101 0001 0001 => in hexadecimal, 0x0511.

For the last element, the address would be 0x0111A, in binary 0b0000 0001 0001 0001 1010. The first 10 bits will be 4 in decimal and from the page table, virtual page 4 will be pointing to physical frame 1. Hence, we will need to erase the first 4 bits (since

the physical address is only 16 bits), change the 6 bits into 1 in decimal, and leave the offset remain the same. So, in binary, the physical address will be 0b0000 0101 0001 1010 => in hexadecimal, 0x051A.

(ii) Assumption used: the entire x[] is not in the cache when the first element read is carried out, after that, the entire x[] is moved to the cache (Locality of Space).

As the first element is not in the cache, it will be a cache miss. When reading the rest of the elements, it will be a cache hit. So, the time required to read the entire array is (5 ns + 100ns) + 9* 5ns =150 ns

(d) Assumption: No resource conflicts, No data dependency, No repairing code

From i1 to i4, it requires 3 cycles to initiate and 4 cycles to be done, thus, it will need 7 cycles.

From i5 to i12, since delayed branching is enabled i11 and i12 will not be discarded, instead, delay slot instructions are always executed. Since R0 is zero, and the loop will stop after R0 is ten, it will loop ten times. So, the total cycles need to execute i5 to 12 for 10 loops is 10*8 cycles = 80 cycles.

At i13, it requires 1 cycle for it to be done.

Hence, the total cycles needed by the CPU to execute the program is 7 cycles + 80 cycles + 1 cycle = 88 cycles.
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2 (a) D
(b) B
(c) C
(d) E
(e) C
(f) C
(g) C
(h) E
(i) E
(j) C

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