

5.1 Input/Output (I/O) Interface

- 1) With reference to the computer system diagram (Figure 1) in the case study notes,
- (a) What are the type (input, output or bi-directional) of processor pins you would connect each of the module's data signal to?

Table 1a

No.	Module	Type (Input, Output or Bidirectional)
i.	Buttons	Input
ii.	Wifi	Bidirectional
iii.	Touch Screen Controller	Input / Bi-directional**
iv.	System Memory	Bidirectional
v.	Display	Output

- (b) Given the following interface requirement, select the appropriate module from the device information list in the case study notes to connect to the processor.

- i. Wifi.
 - a. WIFI0010AC
 - b. 3V electrical interface. VOH, VOL, VIH and VIL compatible with Processor SPI interface.
- ii. Touch Screen Controller
 - a. TS002UART
 - b. 3V electrical interface. VOH, VOL, VIH and VIL compatible with Processor UART interface.
- iii. System Memory
 - a. DRAM0002-16M16, SRAM0002-2M16, NOR0001-1M. Actual choice depends on other requirement such as memory speed (read/write), cost etc.
 - b. 3V electrical interface. VOH, VOL, VIH and VIL compatible with Processor Parallel Bus interface.
 - c. 16 bit data bus compatible with Processor 16 bit parallel bus interface. We can also use 2X 8-bit memory if required.

e 1b

Interface Type
SPI Max clock speed: 50 Mhz
UART Max baud rate: 115200 Kbps
Parallel Bus

- (c) For each of the interface shown in **Table 1b**, is the data transfer serial or parallel?

Serial

- (d) Describe the difference between synchronous and asynchronous interface. Are the interfaces shown in **Table 1b** asynchronous or synchronous? Explain.

With clock (sync) and without (asycn), Sync

- (e) With reference to the SPI wifi module chosen in 1(b) above, what is the maximum speed that data can be transferred between the wifi module and the processor?

Max clock speed: 50 Mbps

- (f) With reference to the device information of the system memory you have chosen in 1(b) above, what is the maximum data transfer rate achievable between the system memory and the processor? Assuming that data on the parallel bus gets transferred on each rising edge of the data strobe.

Maximum data strobe rate = 200Mhz

5.2 Data Transfer

- 2) Fig. 2 shows the logical waveform of an asynchronous data frame.

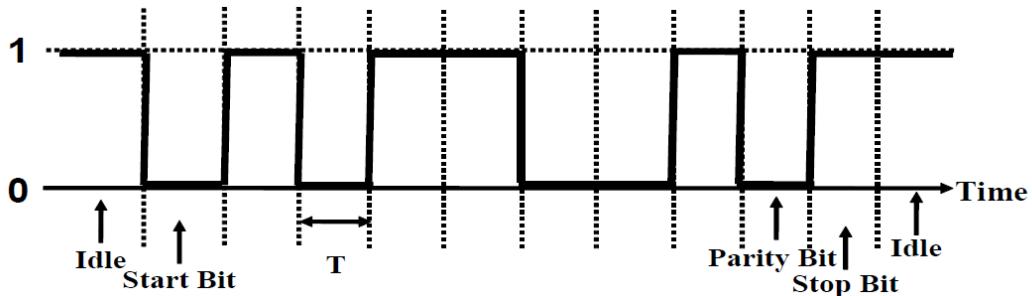


Fig. 2

Answer the following question with reference to Fig. 2:

- (a) Specify the 7-bit ASCII character that is transmitted (LSB is transmitted first).

[1001101 ASCII M](#)

- (b) Assume there are no errors in the transmitted waveform, state whether even or odd parity is being used.

[Even](#)

- (c) Assume two of the bits received in the character are erroneous; can the receiver detect the error? Can you extend the example to determine the limitations of parity checking?

[Can, The source then transmits this data via a link, and bits are checked and verified at the destination.](#)

[Data is considered accurate if the number of bits \(even or odd\) matches the number transmitted from the source.](#)

- (d) If 7-bit ASCII characters are transmitted continuously in the format shown (with no idle periods between the frames) at a baud rate of 9600, calculate the following:

- i. The value of T in Fig 2. $1/9600 = 0.104 \text{ ms or } 1.04 * 10^{-4}$

- ii. The data transfer rate of this serial interface in characters per second (cps).

[960 cps](#)

[1 packet consist of start, data, parity n stop bits](#)

- (e) Re-compute the data transfer rate (cps) if the transmission does not use any parity bit.

Compare the results with those obtained in Q3d(ii), and state your observation(s).

[9600 bits/second /9bits\(1 packet\) = 1066 characters per second. Throughput is higher, but the intergrity of the data pac](#)

- (f) Assume the baud rate of the transmitter is 4800, but the baud rate of the receiver is configured as 9600. Based on Fig. 2, determine, if any, the ASCII character(s) that will be received.

[0011001111 0000110011 ASCII 'f and 'CAN'](#)

(Not necessary to be covered during tutorial)

- 3) There has been a trend of ‘serialization’ of interface bus standard. E.g. USB replacing Parallel Port Interface, SATA replacing IDE in HDD.
 - (a) What are the advantages that Serial Bus has over Parallel Bus interface that enticed industry player to move in this direction?
 - Less Skew and crosstalk
 - Less bulky so easier to route PCB trace and cabling
 - Serial are able to achieve relatively high baud rates
 - (b) What are the scenarios in which Parallel bus will still be preferred over Serial bus?
 - What are the design considerations that need to be put in place in such cases?
 - interfacing to DDR SDRAM.
 - length of parallel bus usually shorter
- 4) In Q3(f) above, a wrong sampling result is observed when a wrong baud rate is used. This can actually be used to implement auto baud rate detection. Briefly describe how this can be done.

A Carriage Return has the ASCII value of 0x0D and would be sampled as different value with different baud rate assumption. If the receiving device knows that the transmitting device sends a 0x0D, then it'll be able to derive the baud rate based on the value sampled. Below is an example for the case when receiving device is sampling at 115200 Baud. If the transmitting device is sending 0x0D at 38400 baud, the data received will be 0x1C. Note that other Ascii characters can also be used as long as that value yields different result when sampled under different baud rate.

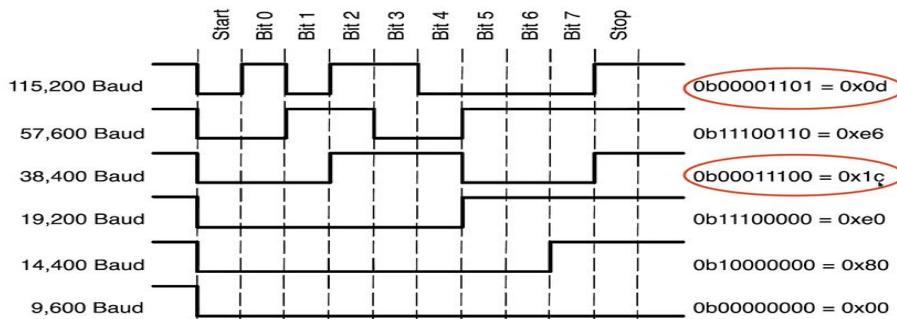


Figure 3. Bit Patterns for Baud Rates Between 115K and 9,600

If data sampled is 0x00. That means baud rate is 9600 or below. In this case, the receiver baud rate has to be adjusted to 9600 and resample the UART data. Below is the chart showing the different values that will be sampled by virtue of the transmitting baud rate.

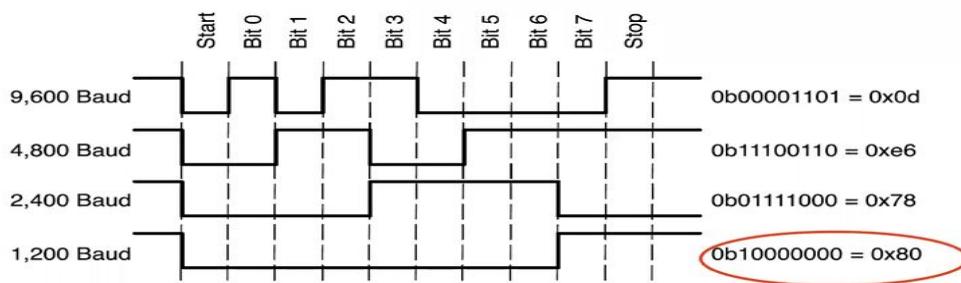


Figure 4. Bit Patterns for Baud Rates Between 9,600 and 1,200

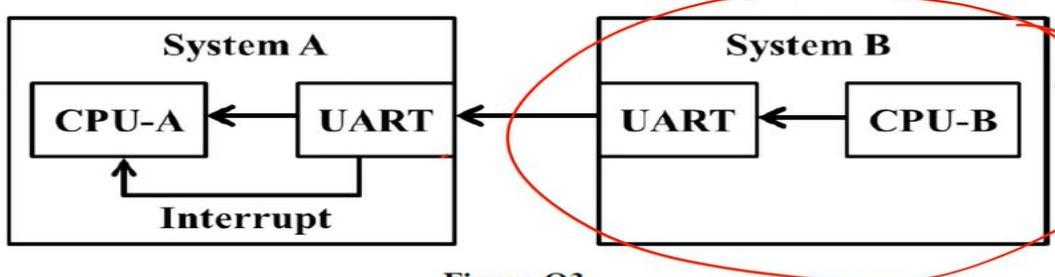


Figure Q3

Table Q3b

System A	System B
CPU Interrupt Latency = 10 instruction cycles	CPU Interrupt Latency = 5 instruction cycles
Number of instructions in UART_RX_ISR = 40	Number of instructions in UART transmit routine = 20
Instruction cycle time = 10µs	Instruction cycle time = 20µs
UART Configuration: 1 Start Bit, 7 data bits, Odd Parity, 1 STOP bit	
Allowable UART baud rate: 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200	

With reference to Figure Q3 and Table Q3b, answer the following questions:

- (i) In order to achieve the maximum transfer rate, the UART packets are being transferred one after another without any delay between the packets. Calculate and explain whether the system in Figure Q3 will be able to support such transfers at a baud rate of 19200.

