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FPGA-Par: An Efficient Algorithm for Elegant Partitioning in Multi-FPGA Systems

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1. Introduction

Circuit partitioning is crucial for prototype validation of multi-FPGA systems. The goal is to optimize two factors: the total weight of edges cut between all subsets (*Cut*) and the maximum weight cut between any two subsets (Cut_{max}), while satisfying resource constraints, minimizing the system's operating frequency. However, existing methods exhibit several limitations when applied to multi-FPGA systems, including low efficiency, difficulty in modeling constraints, reliance on specific conditions, and limited scalability. To address these challenges, we introduce FPGA-Par, an efficient and elegant partitioning algorithm for multi-FPGA systems.

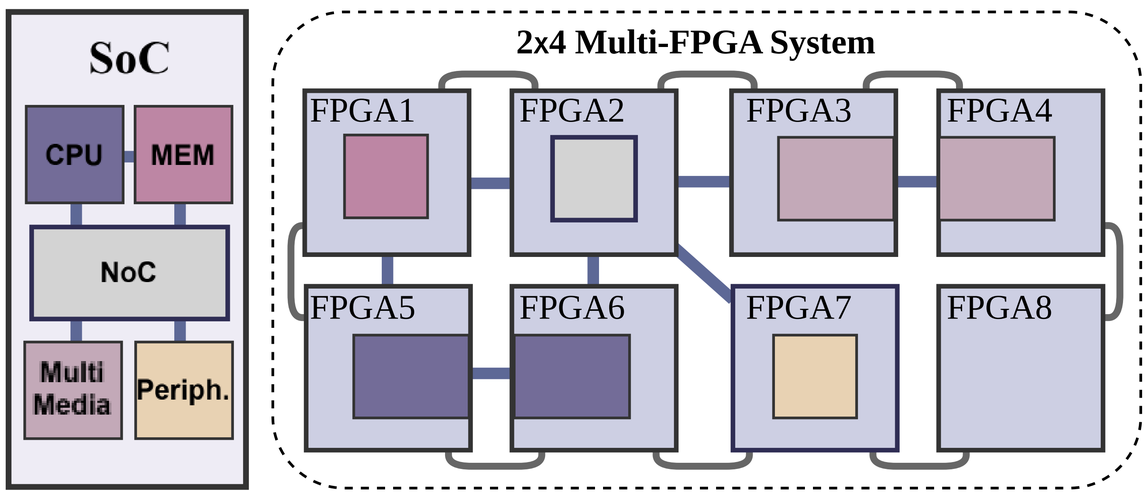

Fig. 1: System on Chip Partitioning for Multi-FPGA Systems

2. Proposed Method

The proposed FPGA-Par algorithm adopts a two-stage framework. In the initial partitioning stage, a Node Resource Fine-tuning Algorithm is used to dynamically resolves resource constraint violations, ensuring partition feasibility while providing a high-quality initial solution for subsequent optimization stage. It enables FPGA-Par to handle partitioning problems under complex multi-dimensional constraints.

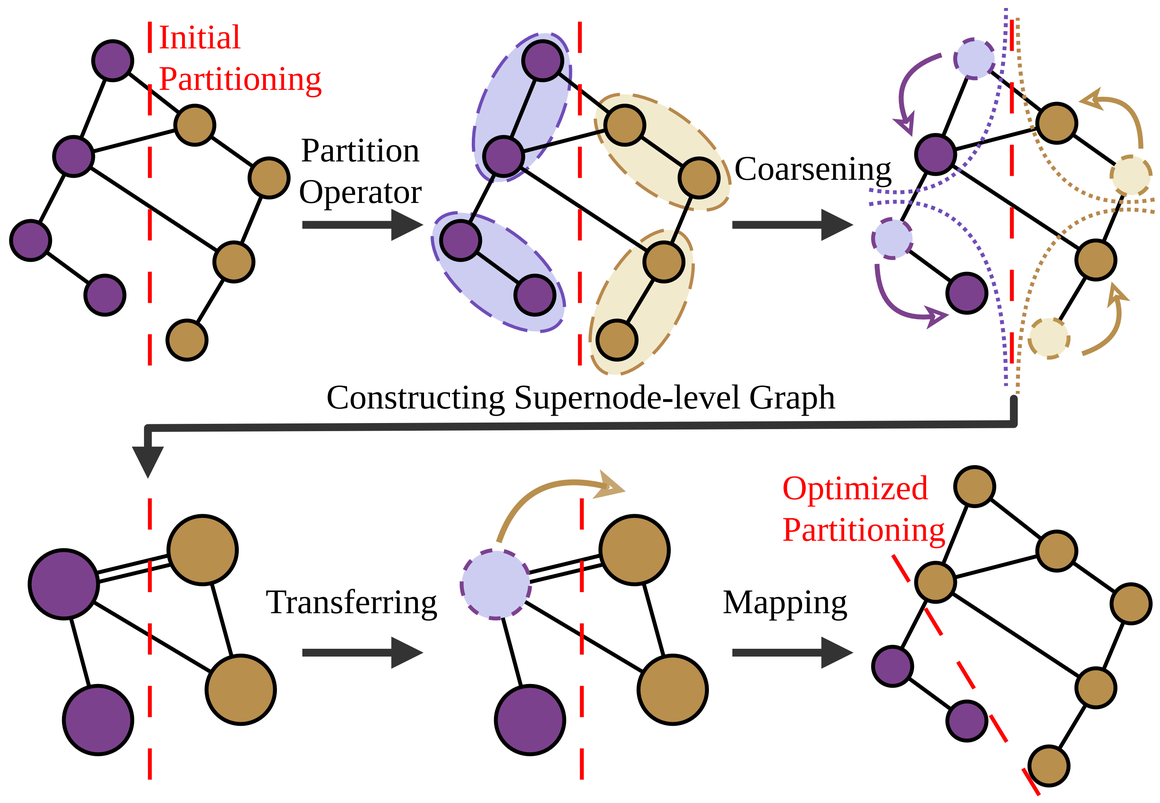

Fig. 2: FPGA-Par Partitioning Algorithm Visualization

3. Experimental Results

We implemented the proposed FPGA-Par algorithm in Python and compared its partition quality, runtime, and operating frequency after deployment to a 5x5 multi-FPGA systems with the state-of-the-art KaHyPar graph partitioning algorithm using six real-world cases provided by S2C.

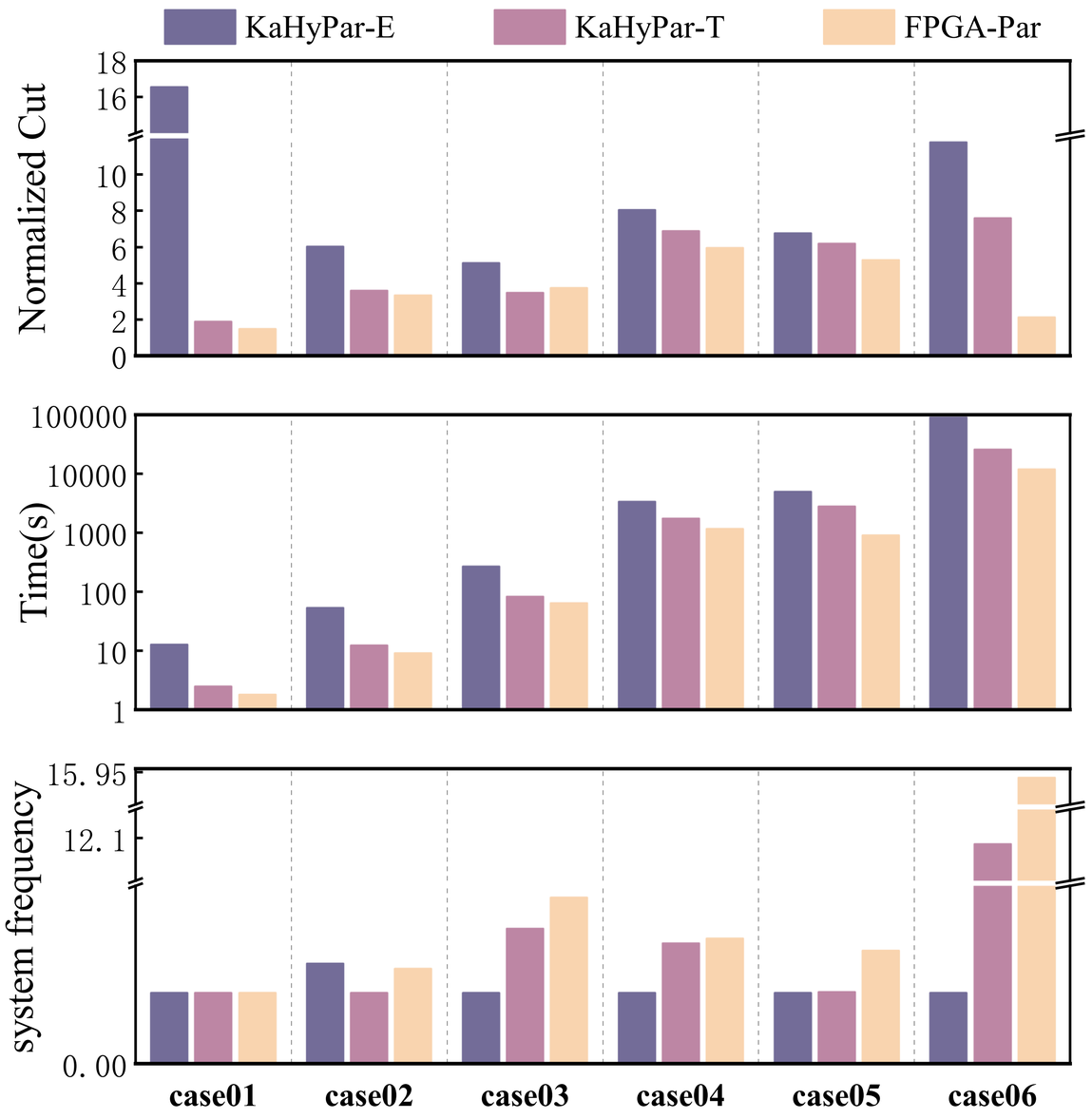

Fig. 4: Experimental Results of Partitioning Methods on S2C Cases

In the iterative partitioning stage, global exploration is performed based on a supernode-level optimization framework. The original nodes are dynamically aggregated into supernodes to construct a higher-order graph representation. A Supernodes Transferring Algorithm is used to adjust the positions of supernodes, significantly improving the partition quality. Additionally, the iterative partitioning process is repeated multiple times at different supernode granularities, guided by a carefully designed dynamic fine-grained parameter strategy, enabling efficient and thorough exploration of the partitioning space.

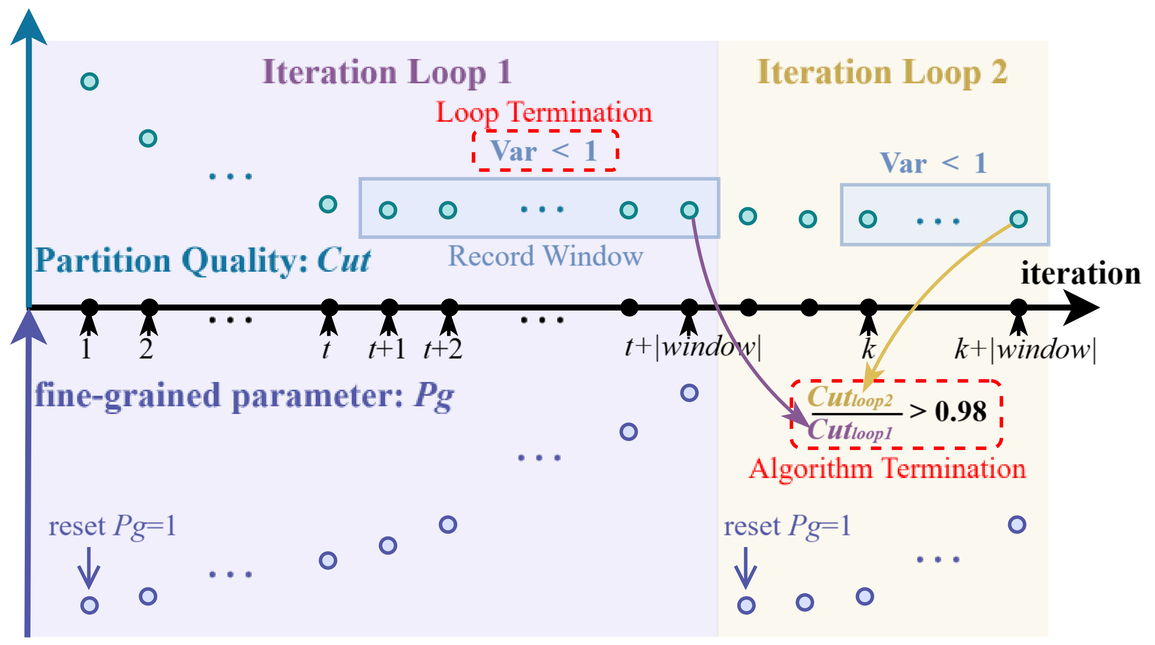

Fig. 3: Diagram of FPGA-Par's Dynamic Granularity Strategy

4. Conclusion

In this work, we propose FPGA-Par, an adaptive graph partitioning algorithm for multi-FPGA systems, which transforms imbalanced partitioning problem into iterative balanced ones. Experiments validate its effectiveness.

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