T12-2

**Impact of Total and Partial Dipole Switching on the Switching Slope of Gate-Last**

**Negative Capacitance FETs with Ferroelectric Hafnium Zirconium Oxide Gate Stack**  P. Sharma1\*, K. Tapily2, A. K. Saha3, J. Zhang1, A. Shaughnessy1, A. Aziz3, G.L. Snider1, S. Gupta3, R. D. Clark2, S. Datta1 1University of Notre Dame, IN; 2TEL Technology Centre, America, LLC, NY; 3Penn State University, University Park, PA.

Email: psharma@nd.edu

**Abstract**: We report, for the first time, a gate last process, used to fabricate Negative Capacitance field effect transistors (NCFETs) with Hf0.5Zr0.5O2 (HZO) as ferroelectric (FE) dielectric in a metal/ferroelectric/insulator/semiconductor (MFIS) configuration. Long channel NCFET’s with HZO thickness down to 5 nm exhibit consistent switching behavior with switching slope (SSrev) below *kT/q* over four decades of drain current. Temperature dependent transport study shows that, the effective mobility of HZO NCFETs is 15 % higher than that of HfO2 based control MOSFETs due to suppression of Hf diffusion into the interfacial SiO2 layer (IL). Using the Preisach hysteresis model, which models dynamics of FE switching through a cluster of independent switching dipoles at arbitrary electric field, we (a) explain the asymmetric SS behavior of NCFETs in MFIS configuration, and (b) establish design guidelines for achieving sub-*kT/q* SS in both forward and reverse sweep direction.

**Introduction:** The negative capacitance FET (NCFET) has generated great interest as a steep slope transistor option since its inception [1]. Hf0.5Zr0.5O2 (HZO), a promising sub-10 nm ferroelectric insulator, is currently being explored as a gate stack for realizing NCFETs [2]. Yet, very few reports exist

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| demonstrating | steep | switching | in | practical | MFIS-type |

configuration (without an intermediate metal electrode between the ferroelectric and the linear dielectric) that is eventually required for a simplified gate stack [3], [4] in scaled nodes. Here, we have integrated HZO/SiO2 gate stack on silicon channel using a gate last scheme which allows optimization of the thermal budget for HZO, thereby enhancing its ferroelectric phase integrity. **Fabrication**: Fig. 1 summarizes the process flow of N-channel NCFETs fabricated using a gate last scheme. For the gate stack, a thin film of Hf0.5Zr0.5O2 (HZO) or HfO2 is grown by ALD and, subsequently, a capping layer of 5 nm thick TiN is deposited by ALD as well. The crystallization of the HZO film is performed using RTP in N2 ambient at 600 0C for 30 s. Fig. 2 shows the high resolution TEM of 5 nm thick HZO stack indicating an interfacial layer of 0.8 nm SiO2 between the HZO and the Si channel.

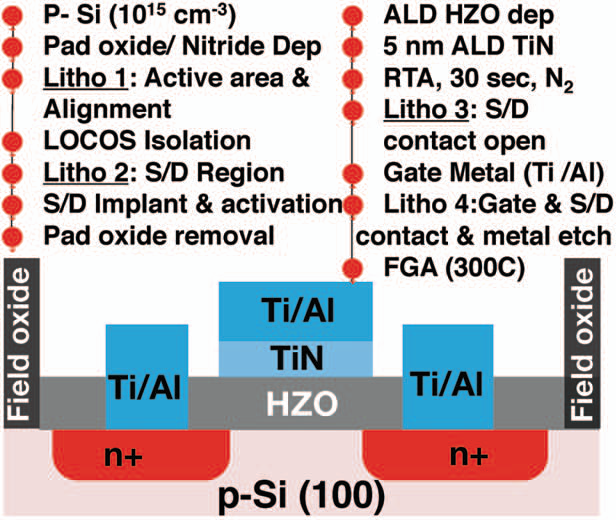
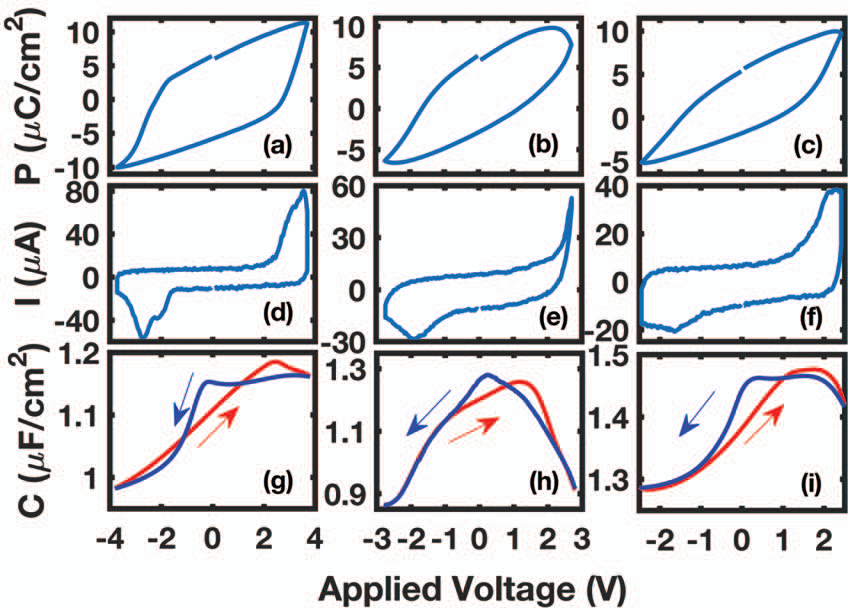
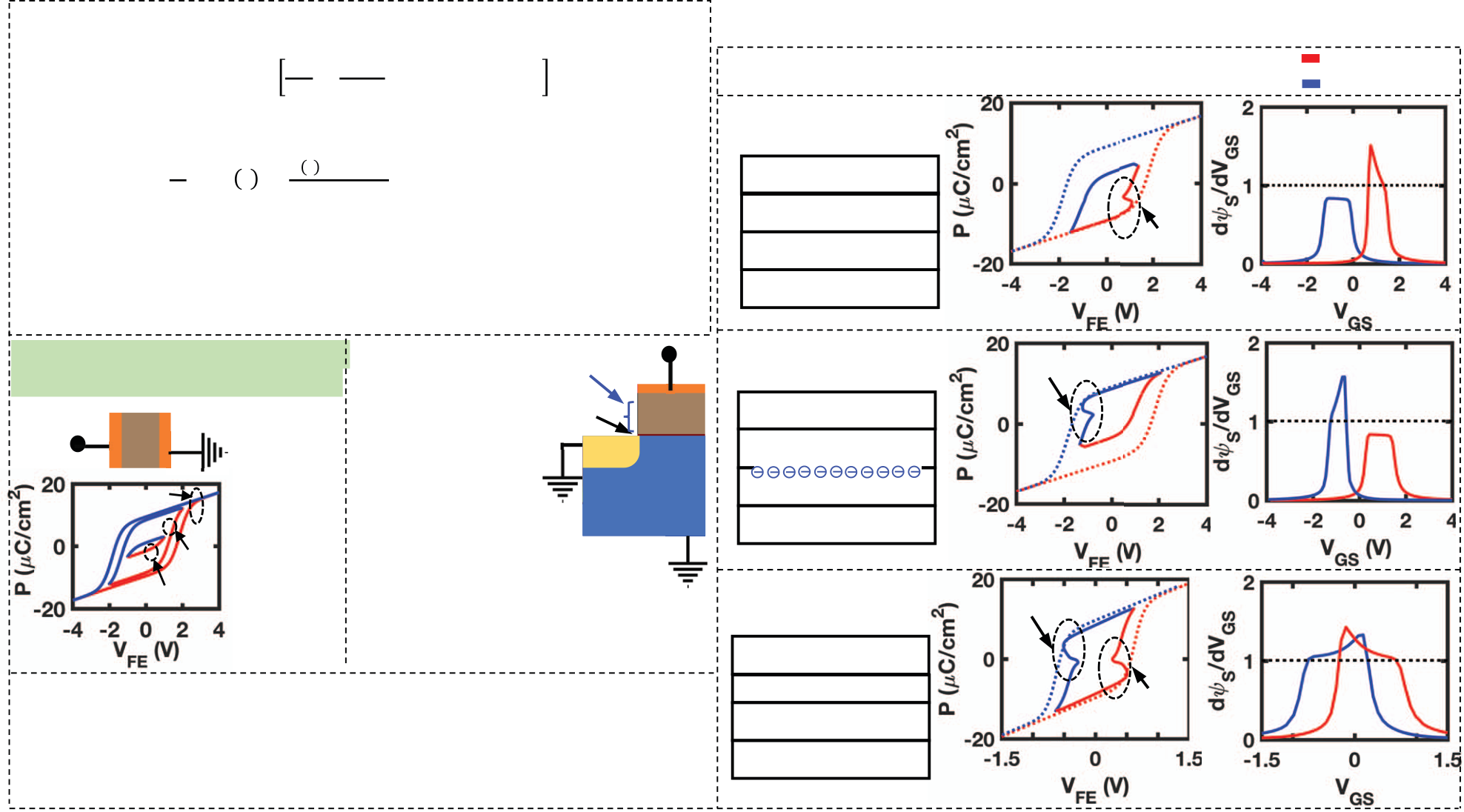
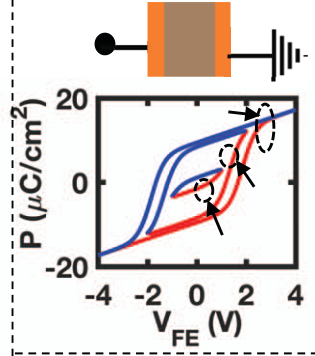
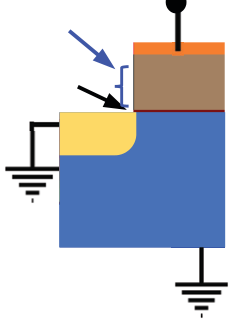
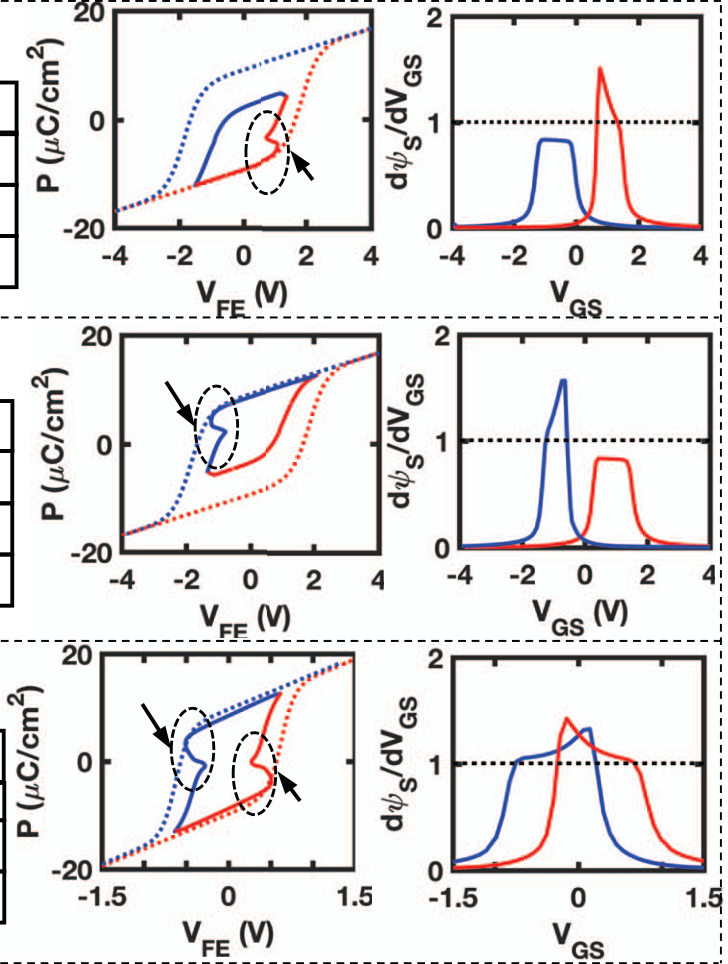
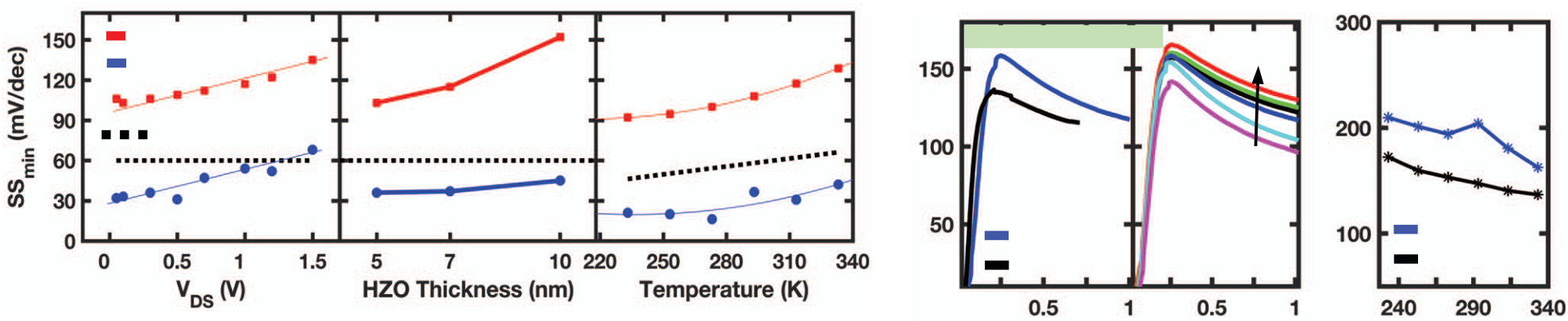
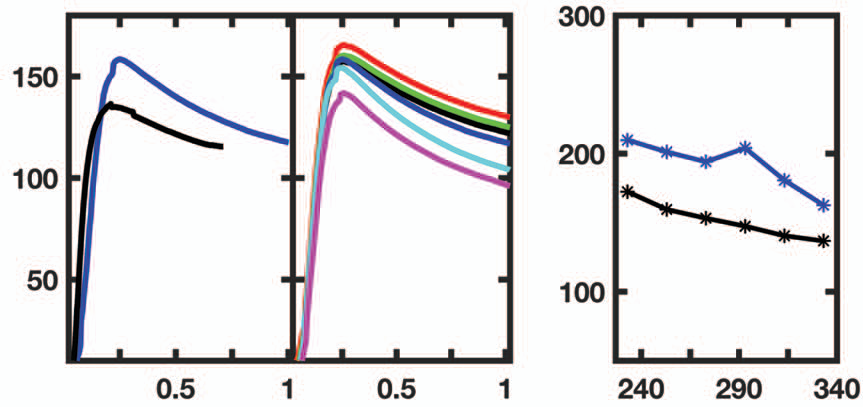
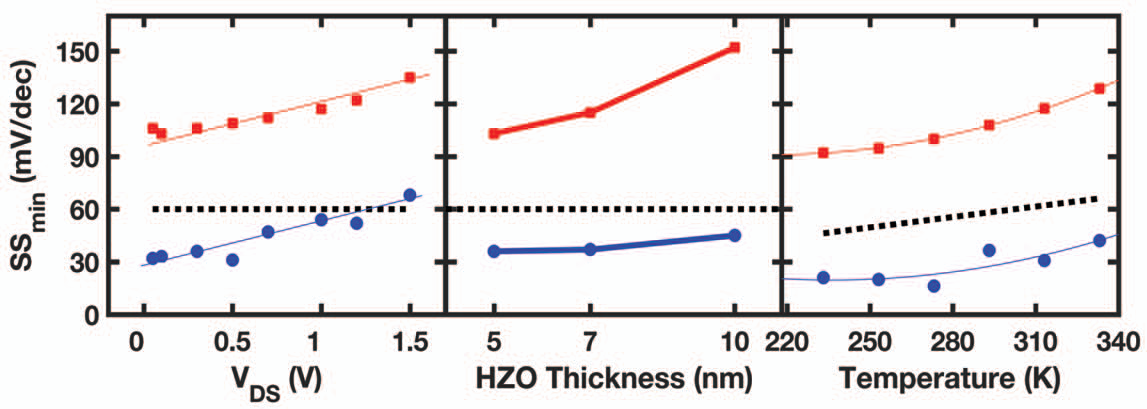
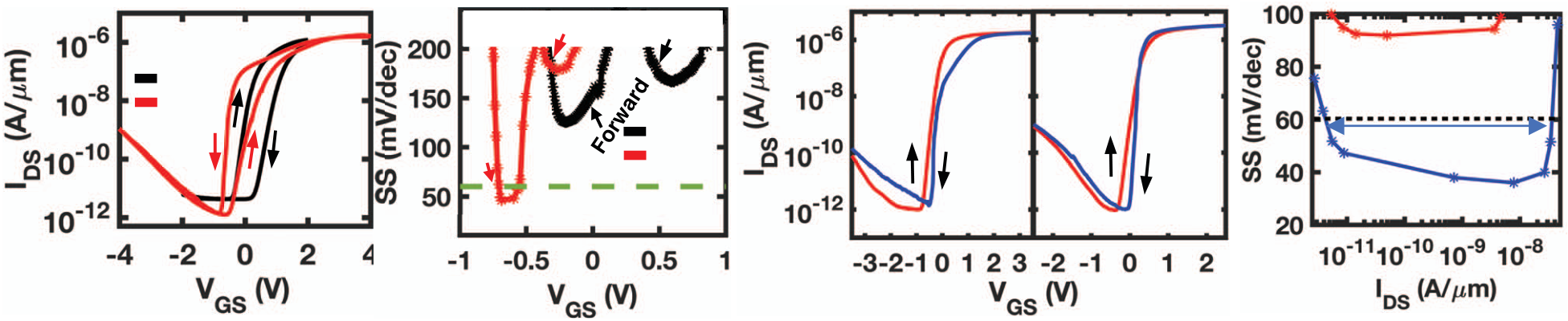
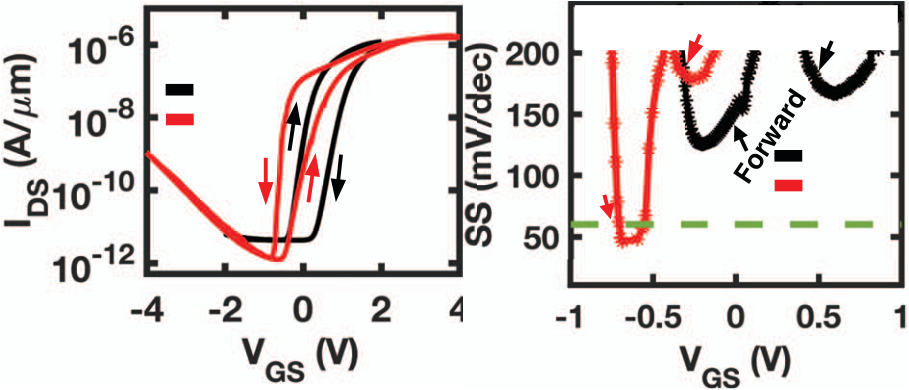
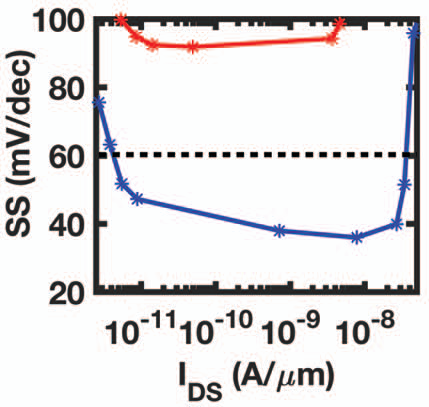
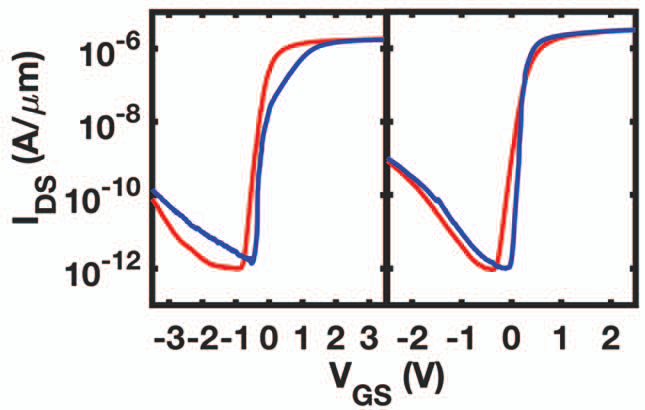
**Results**: The ferroelectric (FE) nature of the films is validated by measuring the polarization charge vs gate voltage on, a metal/HZO/SiO2/n++ doped test structure on the same wafer. The expected hysteresis loop is observed in the large signal polarization-voltage measurement as shown in Fig. 3a-c. Small signal CV measurements (Fig. 3d-f) exhibit typical butterfly-shaped hysteresis loops further validating the FE character of the 10 nm, 7 nm and 5 nm FE gate stacks [2]. Fig. 4a shows the IDS-VGS transfer characteristic of N-channel NCFET with 10 nm thick HZO. When VGS is swept from -2 V to 2 V, the device exhibits clockwise hysteresis due to electron trapping from the channel. However, when swept from -4 V to 4 V, the NCFET shows anti-clockwise hysteresis with steep switching in the reverse direction (Fig. 4b). This leads to the important observation that it is crucial to drive VGS beyond the coercive voltage (~3.5 V in this case) to obtain the steep switching. In addition, it signifies that complete dipole switching is essential for the onset of NC effect. The result motivates future efforts to reduce the coercive field (EC) of HZO’s and scale HZO thickness if low voltage NCFETs with steep switching is to be realized. Similar characteristics is observed for 7 and 5 nm FE films, with steep switching occurring during the reverse sweeps (Fig. 5). This trend of SSrev < SSfor is consistent with previous reports on MFIS type NCFETs [4]. Fig. 6 shows SS vs IDS with record sub--*kT/q* SS spanning over four decades of drain

current. Fig. 7a shows SS as a function of VDS with sub-*kT/q* SS observed until 1.2 V; the degradation in SS with increasing VDS may be attributed to the incomplete switching of dipoles near the drain end. Fig. 7b shows a clear trend in improvement in SS with decreasing HZO thickness. Fig. 7c shows the temperature dependence of SSmin,suggesting no ferroelectric to paraelectric phase transition occurring up to the maximum measured temperature. Fig. 8a compares the effective electron mobility (μeff) of HZO NCFET with that of conventional HfO2 MOSFET. The improved mobility in HZO can be attributed to reduction in soft phonon scattering due to reduced diffusion of the Hf ions into the SiO2 IL, previously observed in[5]. Figs. 8b and 8c, respectively, show temperature dependent μeff and extracted remote-phonon limited mobility for 5 nm HZO at 0.5 MV/cm.

**Modeling**: A possible reason for SSrev < SSfor can be explained by the asymmetry in remnant polarization (Pr(+) ≠ Pr(-)) typically observed in MFIS structures (Fig. 3), which are inherently different from MFM type structures (Pr(+) = Pr(-)). This occurs due to the difficulty (or ease) in completely flipping negatively-oriented domains (switchable with EC (-)) as compared to positively- oriented domains (switchable with EC   
(+)) or vice-versa. Reasons for this asymmetry are due to the distribution of charged defects at top and bottom electrodes, work function difference, electron (or hole) injection from the channel before dipole switching, and the channel doping type (n or p). This effect is studied through numerical simulation of MFM and MFIS stacks, wherein the properties of FE material are modelled using Preisach hysteresis model [6]. Fig. 9 shows the simulated polarization hysteresis loop of MFM stack; with decreasing applied voltages, minor FE hysteresis loops start to appear due to partial dipole switching, consistent with experiments. Fig. 10 shows the different cases for MFIS stack. Due to ease in completely accessing EC (-), full negative saturation polarization is reached for FE in MFIS stack (Case I: 10 nm FE), and, therefore, it follows the major path in the forward direction with visible NC effect. However, due to the work function difference, positive saturation polarization is not reached (incomplete flipping of positively-oriented domains take place) and thus the FE follows the minor path in reverse direction without any NC effect. The opposite effect is illustrated in case II. Due to the presence of negative trapped charge (electrons) at the FE/SiO2 interface, it is difficult for FE to completely surpass EC (-) and, therefore, it follows a minor loop in forward direction (without NC effect) and major loop in reverse direction (with NC effect). Thus, the surface potential gain (Fig. 10e) greater than unity is only observed in the reverse case, explaining the phenomenon of SSrev < SSfor. Employing scaled FE provides the opportunity to observe NC effect in both sweep directions as explained in Fig. 10f-g (Case III: 3 nm FE). With lower coercive voltage in 3 nm thick FE, complete saturation polarization is reached for both forward and reverse direction within the same applied electric field across the gate stack. Our simulated result is consistent with the experimental results of Lee et al ([4]) where sub-*kT/q* SS in both directions was observed only for sub-5 nm HZO films.

**Conclusion**: We demonstrate gate-last MFIS type NCFETs with steep switching over four decades and systematically studied SS behavior experimentally and through simulations. We elucidate the importance of advancing the NCFET technology by developing sub 3 nm thick HZO process with low enough coercive field to allow complete dipole switching, and high quality interface between the HZO and the SiO2 interfacial layer (IL) dielectric.

T154978-4-86348-605-8 ©2017 JSAP 2017 Symposium on VLSI Technology Digest of Technical Papers



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **10 nm** | **Metal/HZO/SiO2/Si(n++)** | | |
| **7 nm** | **5 nm** | |
| **10 nm** | **7 nm** | | **5 nm** |
| **10 nm** | **7 nm** | **5 nm** | |

**Fig. 2:** HRTEM cross-section of   
MFIS gate stack with 5 nm HZO.

**Fig. 1:** Process flow and schematic of n-channel NCFET. After active area patterning and   
LOCOS processing, the S/D regions are patterned, implanted and activated. After the

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| gate-stack formation and crystallization, S/D contact openings are patterned and etched | | | | | | | | | | | |
| by a dry etch process, followed by gate and S/D contact metal dep and etch. Finally, a | | | | | | | **Fig. 3:** (a-c) Polarization (P), (d-f) displacement current (I), and | | | | |
| forming gas anneal at 3000C is performed. | (g-i) small-signal capacitance (C) vs voltage characteristics. | | | | | | | | | | |
| **10 nm HZO** | **Forward** | | **Reverse** | | **7nm HZO** | | | **5 nm HZO** | | **Forward** | |
| **± 2 V** | **Reverse** | **178** | | **170** | | **SSmin** | | **SSmin** | **SSmin** | **SSmin** | **2.3KBT/q** |
| **± 4 V** |
| **125** | | **= 106** | | **= 92** |
| **± 2 V** | | **= 36** | **4 decades** |
| **± 4 V** | | **= 27** |

**Reverse**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **(a)** | | **46 mV/dec** | **2.3KT/q** | | **(b)** | | **(a)** | | | | | **(b)** | | | | |
| **Fig. 4:** (a) IDS vs VGS transfer characteristics at VDS = 50 mV for 10 nm | | | | | | **Fig. 5:** IDS vs VGS at VDS = 50 mV for LG = 2 µm | | | | | | | **Fig. 6:** SS vs IDS at VDS = 50 mV for 5 nm HZO (L = 2 µm | | | |
| HZO NCFET (LG = 3 µm/ W= 20 µm) (b) Corresponding SS vs VGS. | | | | | | /W = 20 µm NCFET with (a) 7 and (b) 5 nm HZO. | | | | | | |
| /W= 20 µm). | | | |
| **Forward** | | **(b)** | | | | | **(c)** | **μeff (cm2/Vs)** | | **15 %HIGHER μeff** | | **−40 0C** | | | **μphon (cm2/Vs)** | **0.5 MV/cm** |
| **Reverse** | |
| **(a)** | | **60 0C** | | | **(c)** |
| **2.3KBT/q** | |
| **(a)** | | **step = 20 0C** | | | | |
| **5 nm HZO 5 nm HfO2** | | **5 nm HZO**   **(b)** | | | **5 nm HZO** |
| **5 nm HfO2** |
| **Fig. 7:** (a) SS vs VDS (L = 2 µm, W =20 µm) for 5 nm HZO. (b) SS vs HZO thickness at VDS = 50 mV (L = 1 µm and W = 20 µm). (c) SS vs temperature for 5 nm HZO at VDS = 50 mV (L = 1 µm /W = 20 µm). | | | | | | | | | **Eeff (MV/cm)** | | | | | **Temperature (K)** | | |
| **Fig. 8:** (a) µeff vs transverse electric field (Eeff) L = 1 µm/W = 20 µm for 5 nm thick HZO and HfO2. (b) µeff vs temperature for 5 nm HZO. (c) Phonon limited mobility vs temperature at 0.5 MV/cm. | | | | | | | |
| **Simulation Methodology:** In TCAD, | | the non-linear and transient | | | | | | |
| response of polarization (P) of FE material is governed by the following | | | | | | | | |
| equation: ���� � � ������� | ����� ����������� �������� � ��� +����, | | | [7] | | | | | **Dotted: Stand-alone FE** | | | | | | | **Forward** |
| **Solid: FE in MFIS Stack** | | | | | | | **Reverse** |
| where �� is the saturation polarization, the term *c* is a constant related to the history of FE, and ���� is the offset polarization. ������� is | | | | | | | **Case I: 10 nm FE without** | | | | **(b)** | **(c)** | | | | |
| **interface charge.** | | | |
| calculated from������� � � � � ���������� where E(t) is the applied electric  field and �� is the a material dependent time constant which accounts for  the time-dependent switching behavior of domains in FE. The non-zero  value of ���(10-5 s in our simulations) is essential to physically emulate | | | | | | | Metal | | | | | **NC effect** | | | | |
| 10 nm FE | | | | |
| 0.8 SiO2 | | | | |
| Si | | | | |
| the transient switching behavior of FE and is responsible for origin of the | | | | | | |

snap-back NC effect in MFIS stack.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **���������������������������������������** | | | **Fig. 10:** (a) | VFE | | Ti/Al | VG | **Case II: 10 nm FE with** | **NC effect** | **(e)** |
| **������������������������������������** | | | Schematic of | **interface charge (1013cm-2)** |
| **(a)**   VG Ti/Al FE | Ti/Al | **Fig. 9:** (a) | simulated MFIS SiO2  stack. (b, d, f) VS  Simulated P vs VFE | | FE | | | Metal |
| 10 nm FE |
| Schematic | n+ | | |
| **± 4 V** | | of simulated | Si p-type | | | 0.8 SiO2 | **(d)** |
| for standalone FE | |
| MFM stack. |
| and FE in MFIS | | 5x1015cm-3 | | | **NC effect** | **(g)** |
| Si |
| (b) |
| **± 2 V** | | stack at 1 KHz.  (c,e,g)Corresponding | **(a)** | VS | | |
| Polarization |
| **Case III: 3 nm FE** |
| **± 1 V** | | (P) vs VFE |
| surface potential gain | |
| at 1 KHz. | **without interface charge.** |
| **(b)** | | (dψS/dVGS) vs VGS | |
| **(f)** |
| for various gate stacks. | | | | | | | | Metal |
| **References**: [1] S. Salahuddin *et al.* Nano Lett., vol.8, no. 2, 405, 2008 [2] J. | | | | | | | | 3 nm FE |
| Müller *et al*. Nano Lett.,vol. 12, 4318, 2012 [3] M.H. Lee *et al. pp. 616* IEDM 2015 [4] M.H. Lee *et al.* IEDM 2016. [5] Y. K. S. Chatterjee *et al.* J. Nano- Electron. Phys 2011. [6] Dragosits, K. Modeling and simulation of | | | | | | | | 0.8 SiO2  Si | **NC effect** |

ferroelectric devices (2000). [7] Sentaurus™ Device User Guide 2015.

2017 Symposium on VLSI Technology Digest of Technical Papers T155