Energy-Efficient Versatile Memories With Ferroelectric Negative Capacitance by Gate-Strain Enhancement

Yu-Chien Chiu, Chun-Hu Cheng, *Member, IEEE*, Guan-Lin Liou, and Chun-Yen Chang, *Life Fellow, IEEE*

***Abstract*— In this brief, we reported a ferroelectric versatile memory with strained-gate engineering. The versatile memory with high-strain-gate showed a >40% improvement on ferroelectric hysteresis window, compared to low-strain case. The high compressive stress induced from high nitrogen-content TaN enhances monoclinic-to-orthorhombic phase transition to reach stronger ferrolectric polarization and lower depolarization field. The versatile memory featuring ferroelectric negative capacitance exhibited excellent transfer characteristics of the sub-60-mVdec subthreshold swing, ultralow off-state leakage of <1fA/μm and >10^8 on/off current ratio. Furthermore, the ferroelectric versatile memory can be switched by ±5 V under 20-ns speed for a long endurance cycling (~10^{12} cycles). The low-power operation can be ascribed to the amplification of the surface potential to reach the strong inversion and fast domain polarization at the correspondingly low program/erase voltages.**

***Index Terms*— Charge trpapping, ferroelectric, multilevel, nonvolatile memory.**

I. Introduction

THE ferroelectric memory combining the switching speed of dynamic random access memory (DRAM) and one-transistor memory structure of flash nonvolatile memory has widely been investigated [1]–[5]. However, the real hot topic attracting more attention is the negative capacitance effect through ferroelectric and antiferroelectric switching [6]–[11]. The ferroelectric negative capacitance effect can be well defined and described by the Landau theory [12]–[15] and also expected to be applied for CMOS technology beyond sub-10-nm node. Another research topic worthy of academic study is energy-efficient ferroelectric memory. In this brief, our versatile memory with the introduction of charge trapping storage based on a gate injection mechanism had been demonstrated. Our one-transistor ferroelectric versatile memory reached the steep sub-60-mV/dec switching and fast program/erase speeds (20 ns) that were more favorable to reduce the dynamic power consumption. To clarify the negative capacitance effect on the switching speed and repeated cycling stability of memory, the flicker noise measurement and long endurance tests were performed here.

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II. Experiments

In this brief, the ferroelectric versatile memory was implemented by using a *p*-channel MOSFET with a combined storage scheme employing ferroelectric HfZrO (HZO) and charge-trapped ZrSiO (ZSO) layers. Then, fabrication procedure of *p*-channel ferroelectric MOSFET was described below. First, a 3.5-nm SiO_2 was grown by vertical furnace as a buffer oxide on *n*-type silicon substrate. Then, the 23-nm-thick HZO ferroelectric layer and 5-nm-thick ZSO trapping layer were deposited by evaporation and sputter systems. The stacked dielectric was then annealed at 400 °C. Subsequently, the 3-nm SiO_2 was deposited as a top tunnel oxide to form final gate-stack structure. The TaN metals with various nitrogen contents were then patterned as gate electrodes. The source and drain regions are followed by a self-aligned BF^{2+} implantation and activated by an RTA. Finally, Al metals were evaporated as source/drain contacts. The fabricated ferroelectric versatile memory has a gate length and width of 10 and 100 μm, respectively. To make a performance comparison, the control ferroelectric memories using a single-layer ferroelectric HfZrO with the same dielectric thickness, thermal annealing, and gate-strain process were simultaneously fabricated.

III. Results and Discussion

Our previous studies reported that the strain-gate effect on ferroelectric HfZrO dielectric can be simulated by the first-principle calculation (FPC) approach [16]. The atomic structures of monoclinic and orthorhombic crystallinities are shown in Fig. 1(a). The formation of orthorhombic phase is very important for the ferroelectricity in HfZrO dielectric. The schematic of strain-induced phase transition is shown

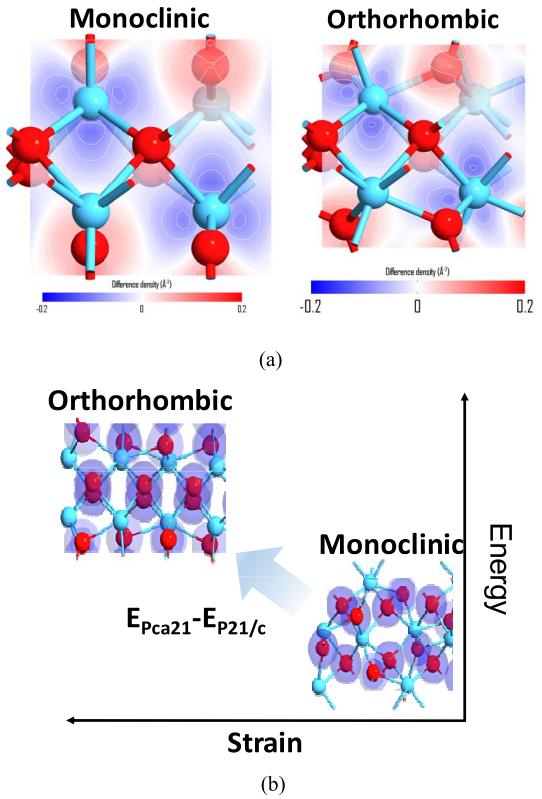

Fig. 1. (a) Atomic structure of monoclinic and orthorhombic crystallinities. (b) Schematic of strain-induced phase transition from monoclinic-to-orthorhombic phase.

in Fig. 1(b). Our FPC simulation has demonstrated that the increased gate strain can enhance the phase transition from low-strain energy monoclinic to high-strain energy the metal gate strain with a locally compressive stress can assist and accelerate the low-energy $P2_1/c$ monoclinic polar phase to overcome the energy barrier ($E_{Pca21}-E_{P21/c}$) of monoclinic-to-orthorhombic phase transition. In this brief, the strain-gate engineering was further applied on ferroelectric versatile memory with a combined storage scheme. The electric characteristic, the ferroelectric negative capacitance effect, and related physical mechanism are described below.

To further improve memory characteristics, we proposed a new storage mechanism of combining the charge trapping and ferroelectric domain. The top thin ZrSiO trapping layer creating an aligned dipoles at ZrSiO/HfZrO interface can effectively reduce the migration effect of charged oxygen vacancies [17], [18]. According to our new experimental result of Fig. 2(a), the TaN gate with high-nitrogen content of 10% shows a larger ferroelectric hysteresis than that of low nitrogen content. This suggests that the high compressive stress induced from high-nitrogen-content TaN enhances monoclinic-to-orthorhombic phase transition to reach a large ferroelectric memory window of 3 V. In addition, the transfer characteristics of ferroelectric versatile memory were also improved owing to the advantage of ferroelectric negative capacitance. Under the influence of negative capacitance supported by the Landau model [12]–[15], the measured OFF-state current (I_{OFF}) can be significantly reduced to below 1fA/μm, which is mainly

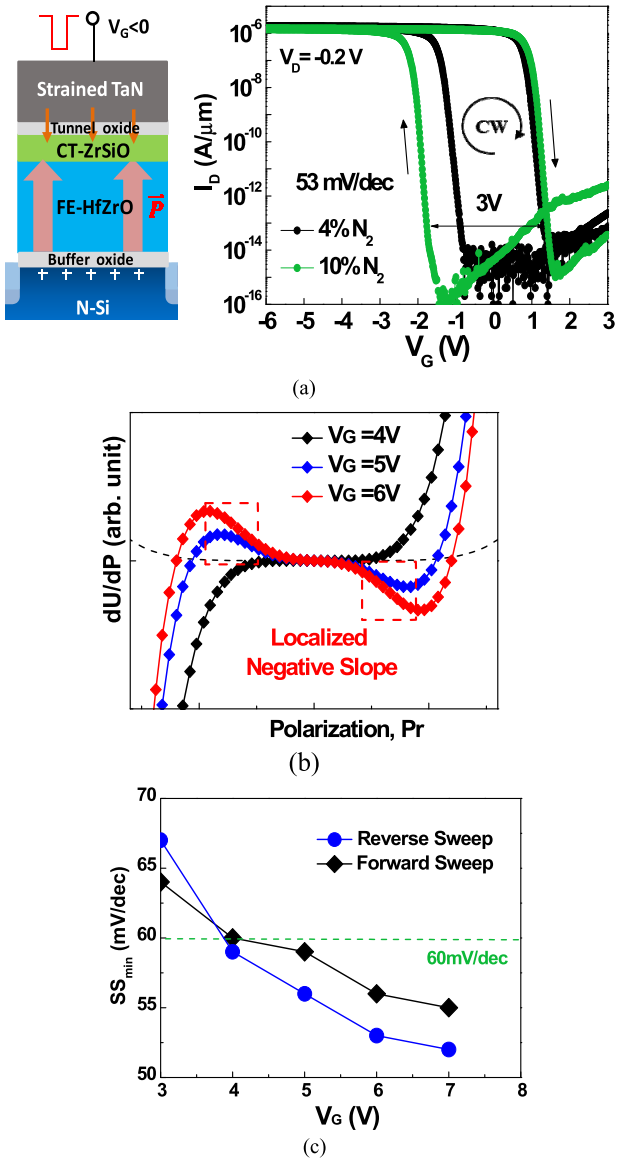

Fig. 2. (a) Transistor characteristics. (b) Derivate *dU/dP* under various gate votalges. (c) SS_{min} as a function of gate voltage of ferroelectric versatile memory with strain gate.

ascribed to steep subthreshold swing (SS) characteristic with the lowest 53 mV/dec under ±6 V dc sweep.

The Gibb's free energy with double well energy landscape was simulated, as shown in Fig. 2(b). The derivate *dU/dP* exhibits a negative slope in a bi-stable well potential, confirming the existence of negative capacitance effect during gate voltage sweep. Fig. 2(c) shows that the SS_{min} of sub-60-mV/dec becomes smaller with the increase of gate voltages. It implies that the negative capacitance effect is significantly affected by the polarization and depolarization of ferroelectric switching along the direction of vertical electric field.

To further investigate the negative capacitance effect in gate dielectric stack, gate bias dependence of flicker noise characteristics was applied for examining the difference of conventional HZO FeRAM and ferroelectric versatile memory with an additional introduction of top ZSO trapping layer.

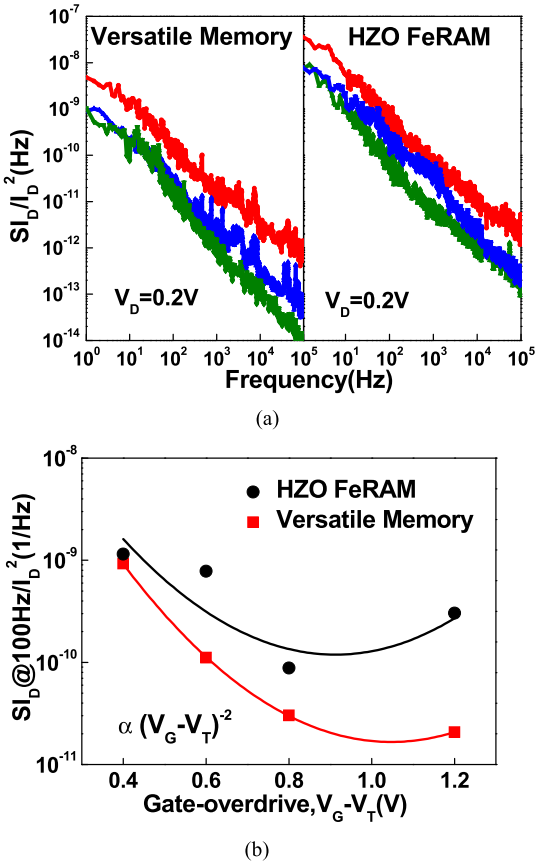

Fig. 3. (a) Normalized current power spectral densities (SI_D/I_D^2). (b) Normalized SI_d for control HfZrO FeRAM and ferroelectric versatile memory.

The measured flicker noise is shown in Fig. 3(a) and the relation between normalized $1/f$ noise (SI_D/I_D^2) and gate overdrive ($V_G - V_T$) is shown in Fig. 3(b). The normalized $1/f$ noise of ferroelectric versatile memory with significant sub-60mV/dec swing is lower than that of control HZO FeRAM. The flicker noise results reveal that the subthreshold characteristics of versatile memory are less influenced by gate-stack traps. Thus, the gate dielectric stack dominated by ferroelectric negative capacitance is more favorable for enhancing the stability of ferroelectric switching.

The high-speed endurance test was also tested for ferroelectric versatile memories with low- and high-nitrogen-content TaN gates. A read scheme using I_{ON}/I_{OFF} ratio is adopted to define sense margin and monitor ON/OFF switching states. As shown in Fig. 4(a), the "0" state and "1" state can be identified by OFF-state and ON-state currents of transistor transfer characteristic. In Fig. 4(b), the fast drain-current response reveals that the speed of ferroelectric–antiferroelectric transition can be reached at 20 ns for both program and erase operation. The fast ferroelectric domain switching like static random access memory and DRAM can be used for cache and main memory.

For one-transistor memory device, the read and write scheme has been proposed [19]. The sense margin is defined by I_{OFF}/I_{ON} ratio under program and erase states. Fig. 4(c) depicts the I_{OFF}/I_{ON} and SS dependence of endurance characteristics under the program/erase voltages of ±5 V. For high-strain-gate with 10% N_2, the much lower I_{OFF}/I_{ON} ratio

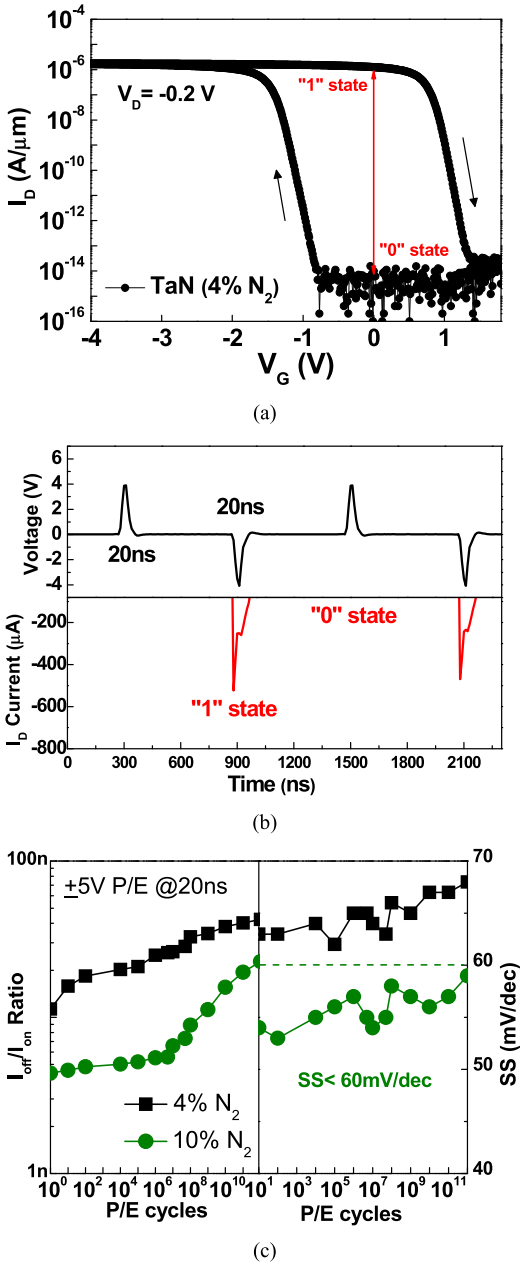

Fig. 4. (a) Transistor transfer characteristic curve. (b) 20-ns I_D response current waveforms. (c) I_{OFF}/I_{ON} and SS dependence of P/E cycling of ferroelectric versatile memory with strain gate.

than low strain one can obtain an energy-efficient ferroelectric switching, according to simplified energy model: $E \propto V_{DD}^2(\xi + I_{OFF}/I_{ON})$ [20]. The I_{OFF}/I_{ON} must be as low as possible in order to obtain small V_{DD} for power saving. It is worth noting that both I_{OFF} and I_{OFF}/I_{ON} keep stable without significant degradation before 10^6 cycles, indicating the gate-stack suffer small damage during program/erase cycling. Furthermore, the high-strain-gate case with a steeper sub-60 mV/dec SS exhibits a better fatigue endurance over 10^{12} cycles than that of low-strain-gate case. This is because the high-strain-gate case is accompanied with stronger ferroelectric polarization and lower depolarization field. Thus, the sub-60 mV/dec SS characteristics originated from the negative capacitance effect

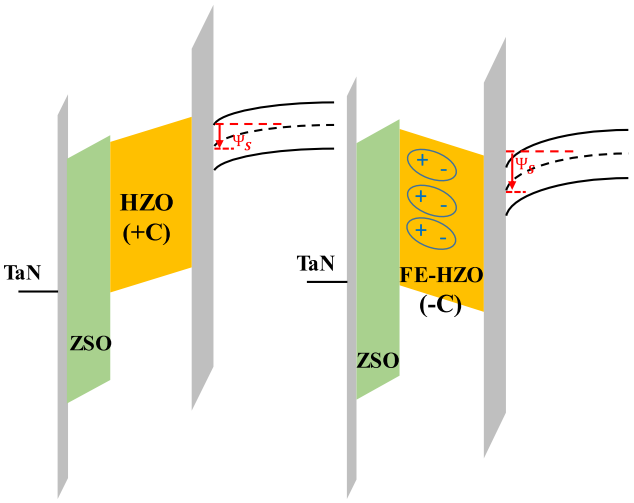

Fig. 5. Schematic band diagrams of gate-stack using control HZO dielectric (positive capacitance) and ferroelectric HZO dielectric (negative capacitance).

can effectively suppress the I_{OFF} ($I_{OFF} \propto 10^{-VT/SS}$) and thus stabilize the I_{OFF}/I_{ON} ratio.

To explain the energy-efficient ferroelectric switching behavior in versatile memory, the schematic band diagram illustrating the operation mechanism is shown in Fig. 5. Compared to traditional HZO dielectric with positive capacitance, the ferroelectric negative capacitance of orthorhombic-phase HZO dielectric can amplify the surface potential (ψ_s) to reach the strong inversion and fast domain polarization at a correspondingly low driving voltage. Thus, the program and erase voltages can be prominently reduced to lower memory switching energy. Besides, the fast ferroelectric negative capacitance switching also enhances the electron tunneling efficiency through gate injection mechanism under negative gate voltage. This part has been verified by fast pulse endurance test with a 20-ns speed in Fig. 4. Therefore, this versatile memory achieves not only the ferroelectric polarization enhancement by strain-gate technique, but also the energy-efficient switching through a negative capacitance effect.

IV. Conclusion

The negative capacitance effect is critical for improving program/erase efficiency and lowering switching energy in strain-gate versatile memory. Based on our best results, we believed that the strain-gate versatile memory with fast speed of 20 ns and long endurance of 10^{12} cycles can be functionalized as one-transistor capacitorless DRAM and have the potential for next-generation memory applications.

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