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Critical Role of Interlayer in Hf0.5Zr0.5O2 Ferroelectric FET Nonvolatile   
Memory Performance

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***Abstract— We fabricate, characterize, and establish the critical design criteria of Hf0.5Zr0.5O2 (HZO)-based ferro-electric field effect transistor (FeFET) for nonvolatile mem-ory application. We quantify VTH shift from electron (hole) trapping in the vicinity of ferroelectric (FE)/interlayer (IL) interface, induced by erase (program) pulse, and VTH shift from polarization switching to determine true memory win-dow (MW). The devices exhibit extrapolated retention up to 10 years at 85 °C and endurance up to 5* × *106cycles initiated by the IL breakdown. Endurance up to 1012cycles of partial polarization switching is shown in metal–FE–metal capacitor, in the absence of IL. A comprehensive metal–FE–insulator–semiconductor FeFET model is developed to quantify the electric field distribution in the gate-stack, and an IL design guideline is established to markedly enhance MW, retention characteristics, and cycling endurance.***

***Index***  ***Terms— Charge***  ***trapping,***  ***ferroelectric***  ***FET (FeFET), Hf0.5Zr0.5O2 (HZO), interlayer (IL).***

I. INTRODUCTION   
**T** HE discovery of ferroelectricity in doped HfO2 has triggered significant interest in FeFET-based nonvolatile

memory (NVM), due to its scalability and CMOS compatibil-

ity [1]. Compared with the embedded flash technology, HfO2-based FeFET is voltage driven, low power, and high speed,

thus promising for embedded NVM application. Unlike other

dopants, HfO2 doped with Zr [Hf0*.*5Zr0*.*5O2 (HZO)] shows ferroelectricity over a wide range of composition and requires

low thermal budget for processing, and, hence, promising for

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manufacturing [2], [4]. However, HZO-based FeFET for NVM is rarely evaluated.

One serious challenge of HfO2-based FeFET is that the charge trapping in HfO2 during write cycle counteracts polar-ization switching and degrades memory window (MW) [5]. Due to relatively large density of defects in HfO2, significant amount of charge trapping is induced by the write pulse. In addition, the charge release process after charge trapping affects read-after-write operation and limits the operation speed. Therefore, it is important to quantify the extent of charge trapping and detrapping.

Finally, the theoretical MW in FeFET is approximately 2*EC* × *t*FE (*EC* is the coercive field and *t*FE is the FE thickness) [6], but most reported HfO2-based FeFETs exhibit≈ 10 nm, about half of the MW around 1 V for *t*FE maximum MW. We show that MOSFET load line reduces

the voltage across FE, forcing it to work on a nonsaturated polarization loop, which reduces the MW. Based on a com-prehensive FeFET model, we demonstrate that MW can be improved by optimizing the electric field distribution in the gate-stack through the utilization of high-*κ* interlayer (IL) dielectric.

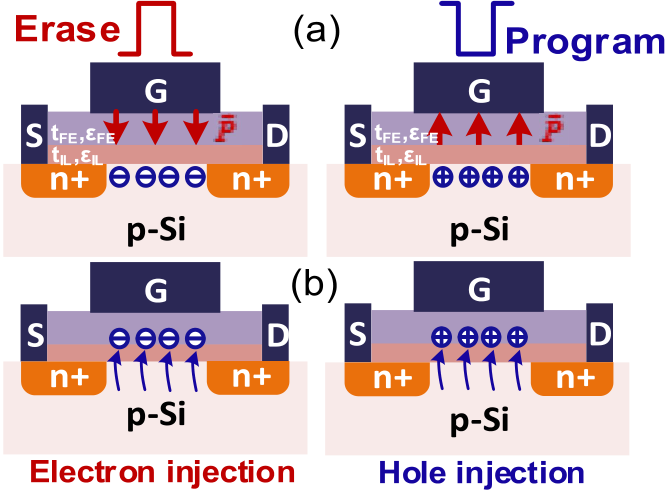
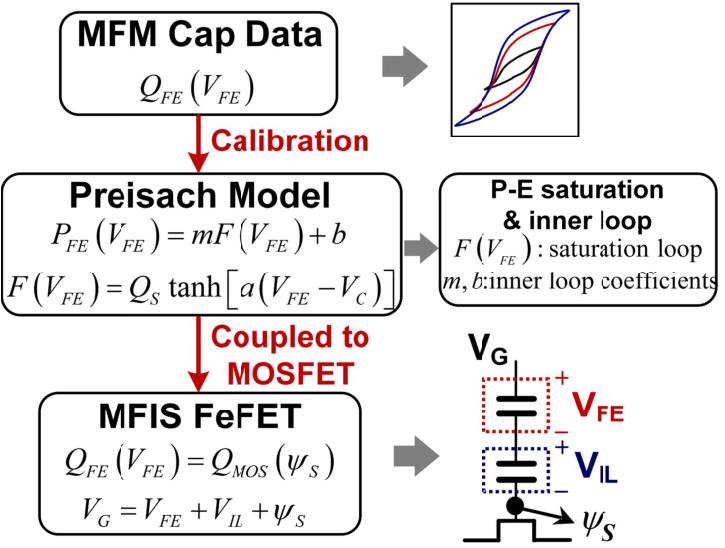
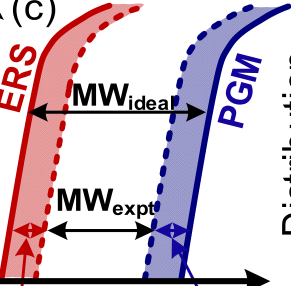
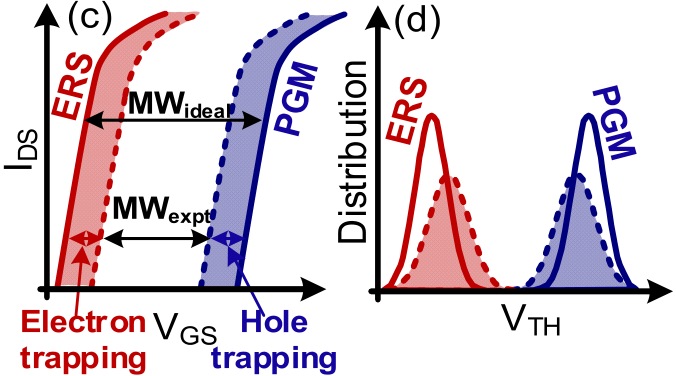
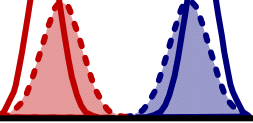
In this paper, a gate-last HZO-based FeFET memory is presented. Charge trapping is separated from polarization switching, and charge release dynamic is investigated. Detailed memory performance and reliability characterization are also performed. In the end, design optimization of the gate-stack to improve MW is demonstrated.

II. EXPERIMENTAL DETAILS

The HZO-based FeFETs were fabricated using a gate-last process. For the gate-stack, 10-nm HZO film and 5-nm TiN capping layer were deposited by ALD, and subsequently annealed in N2 ambient at 600 °C for 30 s to crystallize HZO. Detailed process information can be found in [4]. Fig. 1 shows the top view SEM of FeFET and cross-sectional TEM image of the gate-stack, which is composed of TiN/HZO(10 nm)/SiO2(0.8 nm)/Si.

All the device (including metal–FE–metal (MFM) capac-itor and FeFET) characterizations were performed using

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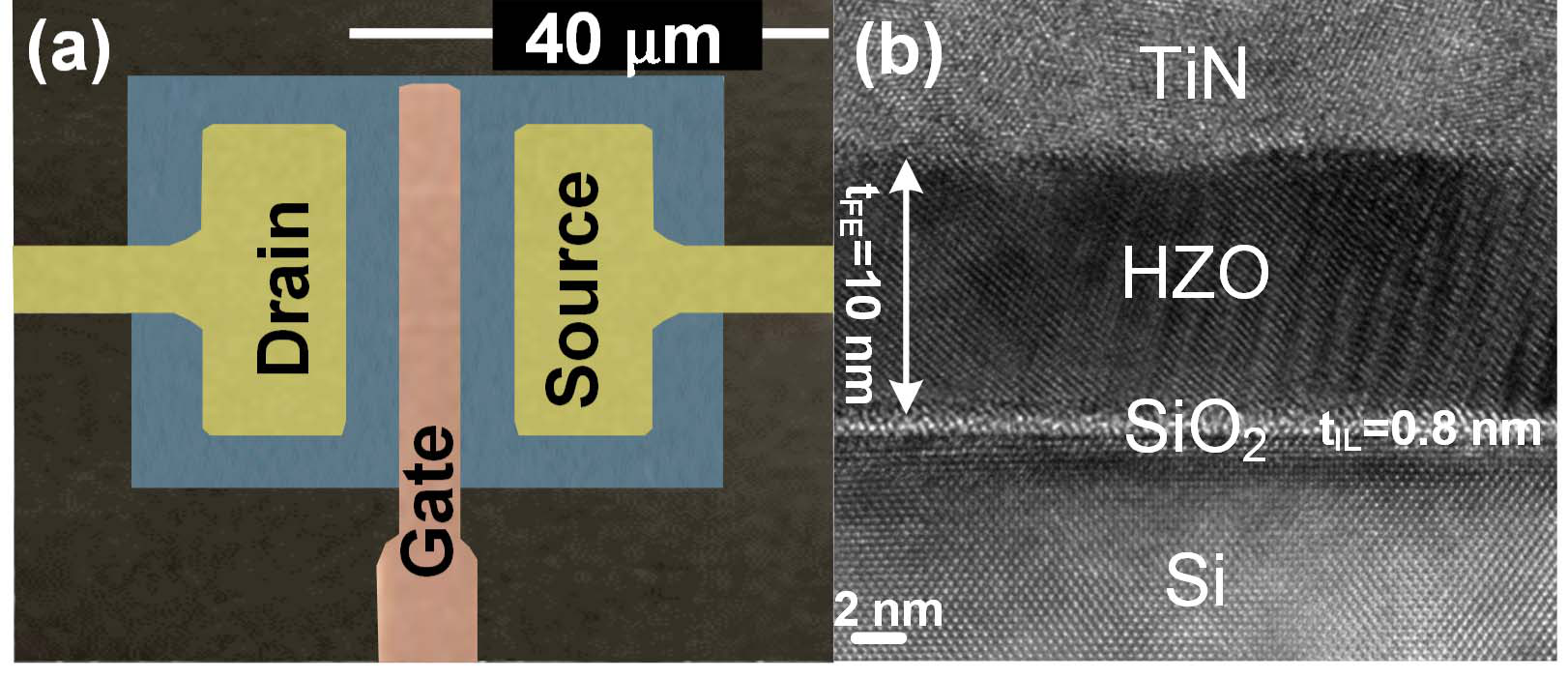
 

Fig. 1. (a) Top view false color SEM of FeFET and (b) TEM cross section   
of metal–FE–insulator–semiconductor (MFIS) gate-stack.



Fig. 3. Modeling framework for MFIS FeFET.

voltages, we use the experimental *Q*FE–*V*FE data obtained   
from MFM capacitors to fit an analytic function (**tanh**) to   
determine the saturated hysteresis loop   
 *F(V*FE*)* = *QS* tanh[*a(V*FE ± *VC)*] (1)   
where *QS* is the maximum charge contribution from polar-  
ization switching, *a* determines the slope of the *Q*FE–*V*FE   
loop, and +*VC*/−*VC* descending/ascending *Q*FE–*V*FE loop, respectively. A linear are the coercive voltages for the

scaling approach is used to describe the nonsaturated inner   
loops   
 *P*FE*(V*FE*)* = *mF(V*FE*)* + *b*  (2)   
where *m* and *b* are the scaling constants. Then, the MFM

Fig. 2. (a) FeFET NVM operation. (b) Electron/hole trapping within

gate-stack during erase/program pulse, respectively. (c) Charge trapping

narrows MW. (d) VTH distribution without (solid line) and with (dashed

line) charge trapping. Charge trapping broadens and shifts distribution.

Keithley 4200 pulse measurement units. Triangular pulses

were applied to characterize the MFM capacitor *Q*FE–*V*FE

loops. For FeFET, different waveform sequences were applied

to study different device properties, which are shown along

with the results in Section IV. *V*TH is extracted using a constant

drain current criterion of *ID* = 10−7A · W/L.

capacitor *Q*FE–*V*FE relationship can be obtained by com-bining the polarization contribution and the linear dielectric

contribution

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| *Q*FE*(V*FE*)* = *P*FE +*ε*FE | *V*FE | (3) |

where *ε*FE is the FE linear dielectric constant and *t*FE is the FE thickness. Since this paper studies the electrostatics of FeFET,

the FE switching dynamics are not included in the model [8].

The MFM capacitor is connected with a baseline MOSFET

in series to form an FeFET. Charge conservation across the

series connected FE, IL, and silicon substrate is imposed

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| III. OPERATION AND MODELING OF FEFET | | | | | | | *Q*FE*(V*FE*)* = *Q*MOS*(ψS)*   *VG* = *V*FE + *VI L* + *ψS* | (4) |
| Fig. 2(a) and (b) illustrates the operation of FeFET memory. | | | | | | |
| Erase/program pulse sets the FE polarization dipole pointing | | | | | | | (5) |
| where the MOSFET charge is given by [9] |
| toward channel/gate, respectively. Therefore, erase/program | | | | | | |
| *Q*MOS*(ψS)* = −√    2*εskBT/q*  *L D*  *f*�  *kBT/q*  *ψS*  �  *L D* =�*kBT εs*    *q*2*NA*  *f (u)* = ±�[*e*−*u*+ *u* − 1]+*n*2 *N*2 *A* [*eu*− *u* − 1]*.* |
| sets the device in low/high *V*TH state, following the same | | | | | | |
| terminologies as flash memory. During the erase/program | | | | | | |
| operation, | the | electron/hole | trapping | in | the | gate-stack |
| decreases the MW, as illustrated in Fig. 2(c). In addition, | | | | | | |
| charge trapping broadens and shifts the *V*TH distribution in | | | | | | |
| an array, as shown in Fig. 2(d), compared with no trapping | | | | | | |
| case. Thus, the emerging FeFET memory technology needs an | | | | | | |
| empirically validated reliable model to quantify intrinsic MW | | | | | | |

for arbitrary write voltages in the presence of charge trapping.

Fig. 3 shows the modeling framework based on the FE interpretation of the static Preisach theory of hysteresis [7]. Since the Preisach theory assumes a distribution of coercive

Here *ψS* is the semiconductor surface potential, *εS* is the semi-conductor dielectric constant, and *NA* is the substrate doping. Equations (1)–(5) are solved self-consistently for each *VG* to obtain the theoretical MW.

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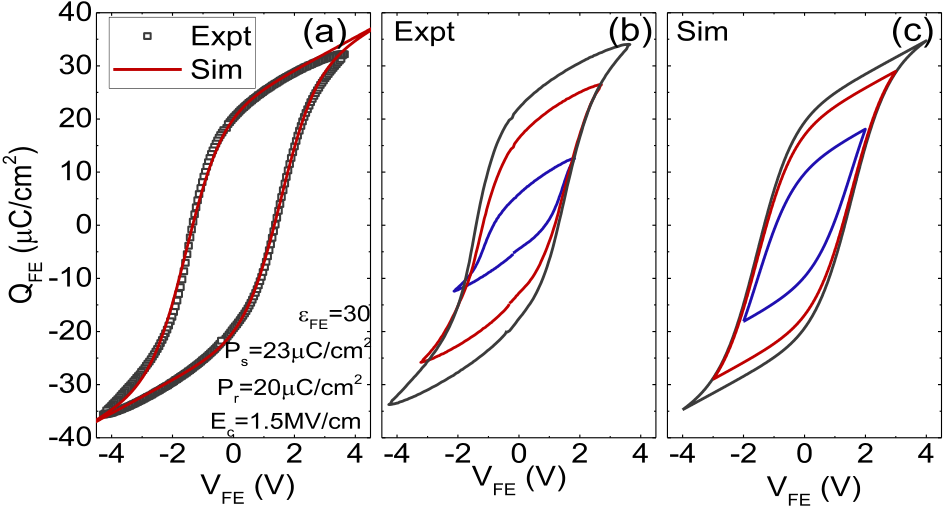


Fig. 4. (a) Calibration of the Presaich model with experimental QFE–VFE saturation loop. (b) Experimental and (c) simulated QFE–VFE loops, including nonsaturated inner loops.

The Preisach model calibration for MFM capacitor is shown in Fig. 4. *Q*FE–*V*FE loops measured and simulated for different *V*FE ranges are independent of each other. Therefore, they are all centered at (*Q*FE = 0 and *V*FE = 0) point. It shows that the analytic function could well capture the saturation loop and give an approximate description of the nonsaturated inner loops. Note that the overestimation of the inner loop polarization charge is because the model is a static one, which does not consider the polarization switching delay at low *V*FE.

IV. RESULTS AND DISCUSSION

A. Theoretical Memory Window

The theoretical MW is modeled using the approach outlined in Fig. 3. Fig. 5(a) shows the *ψS*–*VG* curves, which capture the hysteresis as *VG* is swept forward and backward, due to polar-ization switching. The *VG* separation between the intersection points at *ψS* = 2*φB* denotes the MW. Fig. 5(b) shows the field effect transistor load lines at threshold voltages during forward and backward *VG* sweep. When *VG* sweeps from −4 to 4 V,

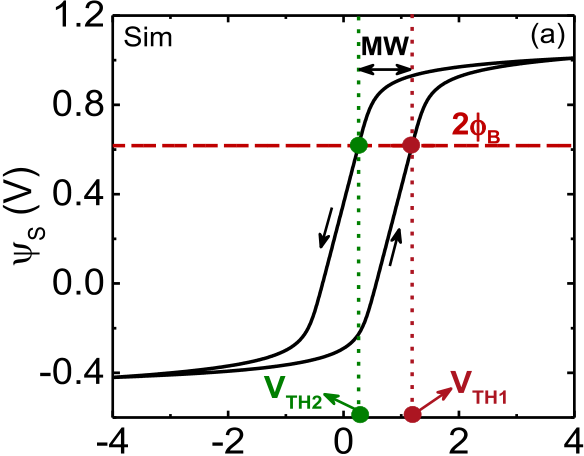
drops across the SiO2 IL and Si channel, the FE operates on *V*FE is only from −1 V to 1 V. Since most of the gate voltage

a nonsaturated inner loop with lower polarization, resulting in reduced MW.

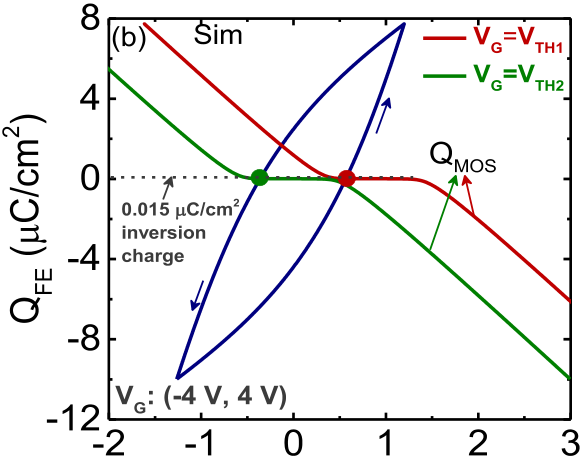
The inner loop FE operates on strongly depends on the *VG* sweep range and saturation remnant polarization (*Pr)*, as shown in Fig. 5(c). The larger the *VG* range and the larger the *Pr*, the closer MWideal is to 2*EC* × *t*FE limit. Measured MW tracks the simulation result very well.

B. Charge Trapping and Detrapping

The measurement of MW is conducted by applying pulse sequence shown in Fig. 6. Program/erase pulses are applied and then each followed by measurement pulses. The measure-ment range is chosen such that it does not disturb the FE polarization state. By tuning the time delay (*T*1/*T*2*)* between program/erase pulse and measurement, the amount of trapped charge sensed can be varied. Measured FeFET *ID*–*VG* charac-teristics after program and erase for time delay of 1 *μ*s and 1 s are shown in Fig. 6. With 1 *μ*s of sense delay, trapped charge narrows the MW, consistent with Fig. 1(c).









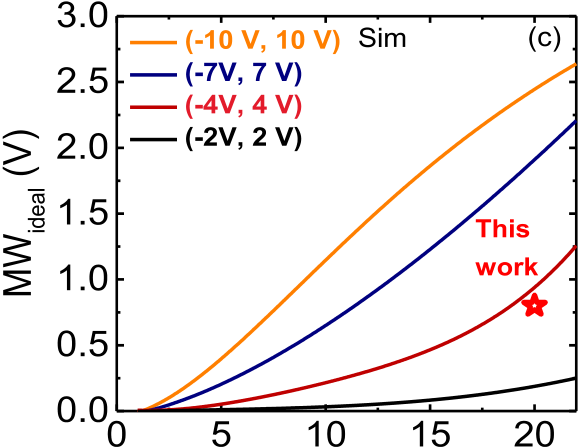




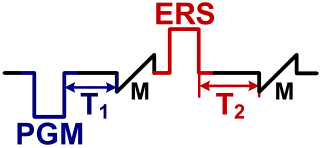
Fig. 5. (a) Surface potential (*ψ*S) versus VG (−4 V, +4 V). (b) MOSFET load lines intersect the QFE–VFE inner loop (dark blue loop) for VTH1 (red curve) and VTH2 (green curve) configuration states (c) MWideal versus remnant polarization (Pr) for different VG ranges. MW widens with larger VG sweep range and larger Pr.

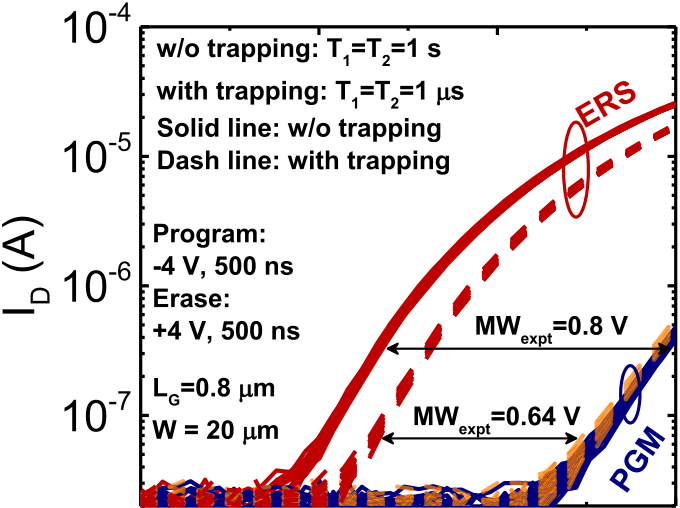
On the other hand, the *V*TH shift solely arising from charge trapping contribution is ascertained by monitoring the electron/ hole release dynamics after erase/program, as shown in Fig. 7. An initial program/erase pulse is applied to set the device to a reference state, and (*V*TH*)*ref is extracted from subsequent *ID*–*VG* measurement. The release dynamics is monitored by probing drain current at certain time intervals after erase/program pulse. This type of one spot measurement has been widely applied to study the charge release for negative bias temperature instability study [10]. *V*TH shift during release could be obtained from the probing current.

The results show that with an erase voltage of 2.5 V, the polarization does not switch; hence, electron release causes *V*TH relax back to initial (*V*TH*)*ref. However, with 4 V erase, *V*TH relaxes to a low *V*TH state, due to polarization switching. Electron trapping dominates over polarization switching at *T*2 = 1 *μ*s, and the release process lasts for approximately 10 ms, which sets the minimum delay of

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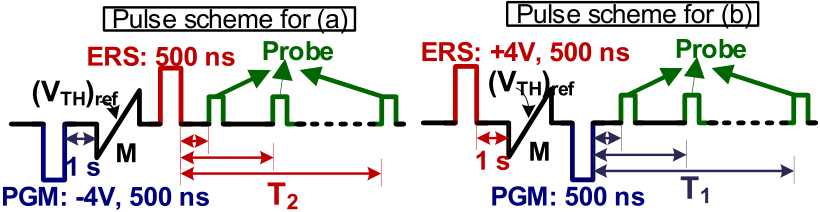


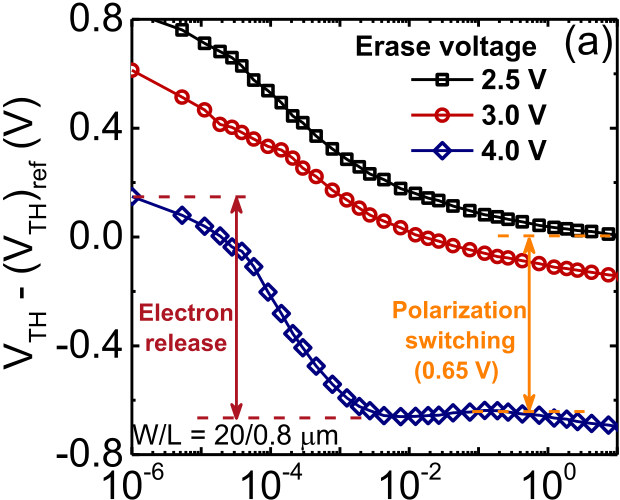


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Fig. 6. ID–VG characteristics after program and erase pulses. A read delay of T1 that MWexpt approaches MWideal. MWexpt narrows for a read delay of = T2 = 1 s allows trapped charge to release such T1 = T2 = 1 *μ*s.







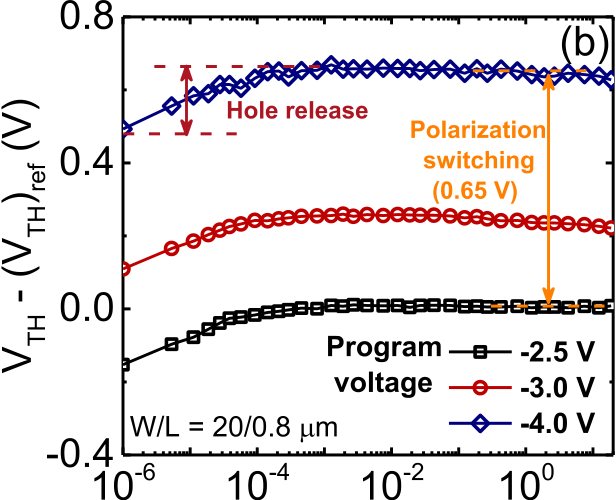
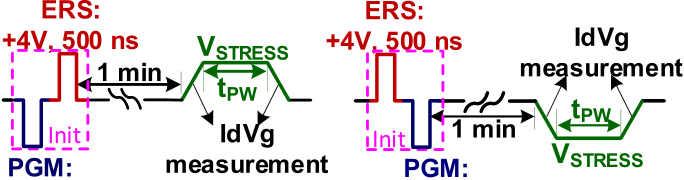




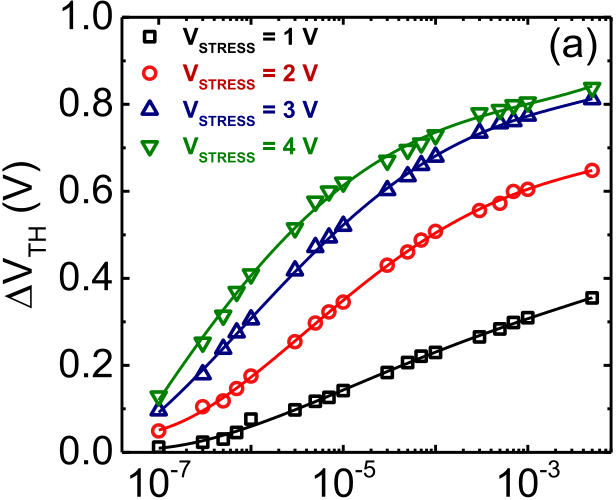
Fig. 7. Dynamics of (a) trapped electron release after erase and (b) trapped hole release after program, as a function of pulse ampli-tude. Holes detrap faster than electrons. For ±2.5-V write, polarization switching is suppressed and thus VTH relaxes back to (VTH)ref.

read-after-write. On the other hand, the hole release is com-pleted within 100 *μ*s, faster than electron detrapping, as previ-ously observed in high-*κ* dielectric [11], [12].*V*TH induced

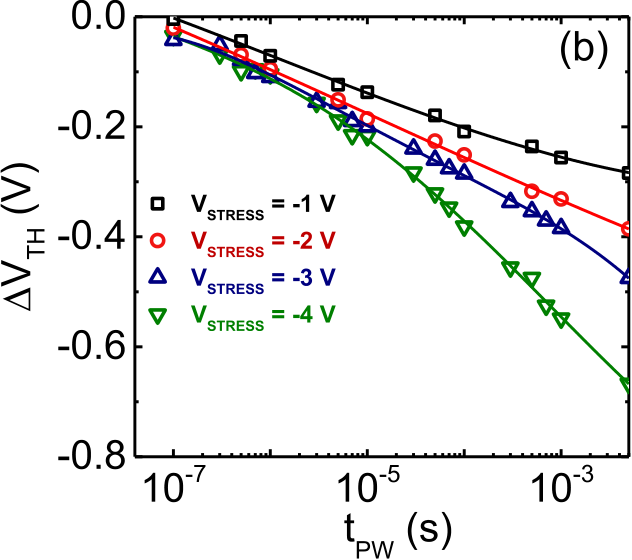
 









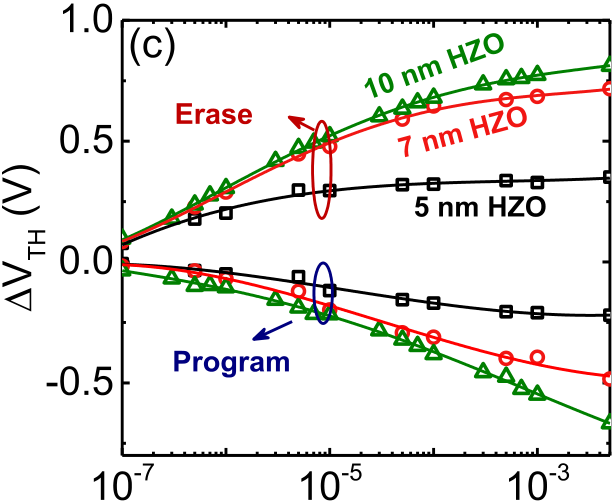


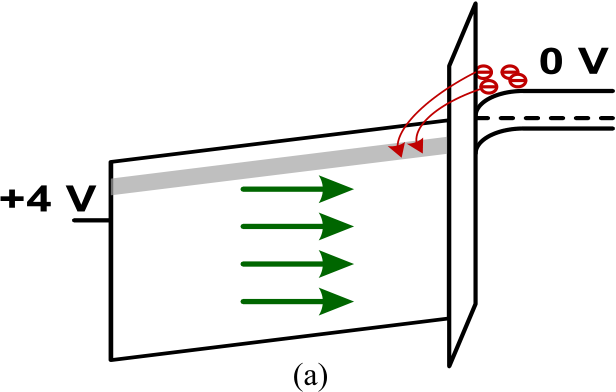


Fig. 8. (a) Electron and (b) hole trapping during positive and negative voltage stresses, respectively. Electron trapping is more efficient than hole trapping. (c) Charge trapping increases approximately linearly with HZO thickness, suggesting trapping close to the FE/IL interface. *Δ*VTH is the shift between ID–VG curves measured at rising/falling edges, which last for 1 *μ*s. W/L = 20/0.8 *μ*m.

by electron and hole release is 0.8 and 0.15 V, respectively, corresponding to 2*.*1 × 1019cm−3/1*.*9 × 1018cm−3trapped electron/hole during erase/program, assuming a uniform trap distribution in the FE [*VT H* = *ρ*FE*t*2 (*V*TH*)*IL represents threshold voltage shift induced by the FE*/*2*ε*FE + *(VT H)I L*, IL charge trapping and is estimated from Fig. 8(c)]. This is consistent with the estimated defect densities in HfO2 [5] Fig. 8(a) and (b) shows the electron/hole trapping as a function of applied stress pulse duration and amplitude.

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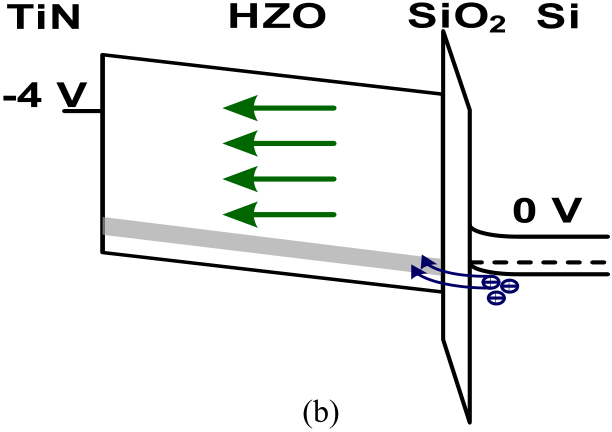
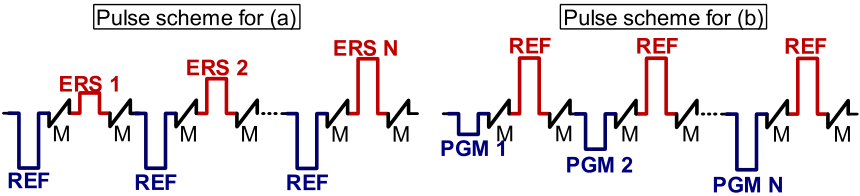
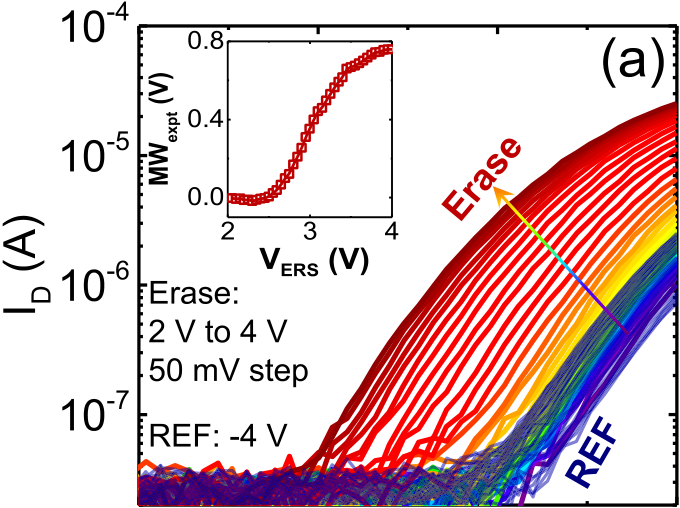


Fig. 9. Energy band diagram during (a) erase and (b) program pulses. Corresponding polarization is shown in green arrow. Charge trapping is also indicated.

The device is initialized in such a way that no polarization switching occurs during stress. The rising/falling edges of the stress pulse are used to measure the *ID*–*VG* transfer characteristics before and after stress, whose *V*TH difference represents charge trapping during stress. Charge trapping increases with stress amplitude and saturates with duration, suggesting trapping at preexisting traps, instead of defect generation, with electron trapping more efficient than hole trapping. Note that the extracted*V*TH underestimates the actual amount of charge trapping, because the charge trapping during the rising edge reduces the amount of available defects for trapping during stress. This amount of significant charge trapping is partially due to polarization, which enhances the IL electric field, assisting charge injection from channel [5]. The effect of HZO thickness on charge trapping is also studied, as shown in Fig. 8(c). An approximate linear increase of*V*TH with HZO thickness at small pulse widths (*<*1 *μ*s) suggests that the charge trapping is in IL. At long pulse widths,*V*TH shows a saturating dependence on HZO thickness. It is likely that at small pulse widths, the charge trapping happens only in the IL due to limited available time for trapping. At longer pulse widths, charge trapping will happen in the FE, beyond the IL. This saturation dependence on the FE thickness and the short time scale (*<*10 ms) suggests that charge trapping mainly happens adjacent to the FE/IL interface, not in the





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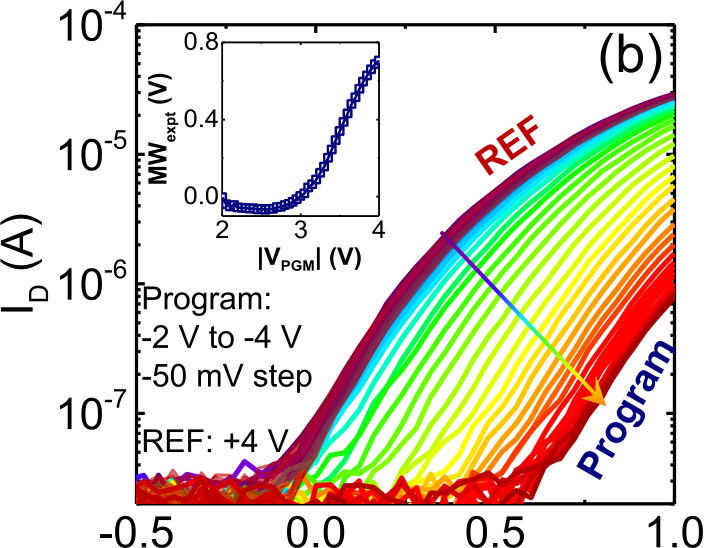




Fig. 10. ID–VG characteristics with increasing (a) erase and (b) program voltage amplitudes. Inset: MWexpt as a function of the write amplitude. MWexpt monotonically increases with amplitude. Pulsewidth of 500 ns is applied. W/L = 20/0.8 *μ*m.

C. Variation, Retention, and Endurance

The effect of erase/program pulse amplitude on polariza-tion switching is shown in Fig. 10. Erase/program pulses with incremental amplitudes and fixed reference pulses are applied. The *ID*–*VG* curve continuously shifts negatively/ positively when erase/program amplitude increases, as shown in Fig. 10(a) and (b). The measured MW could be monoton-ically tuned with pulse amplitude, corresponding to partial switching of FE domains, offering a tantalizing possibility for multilevel cell memory or even analog memory for neuromor-

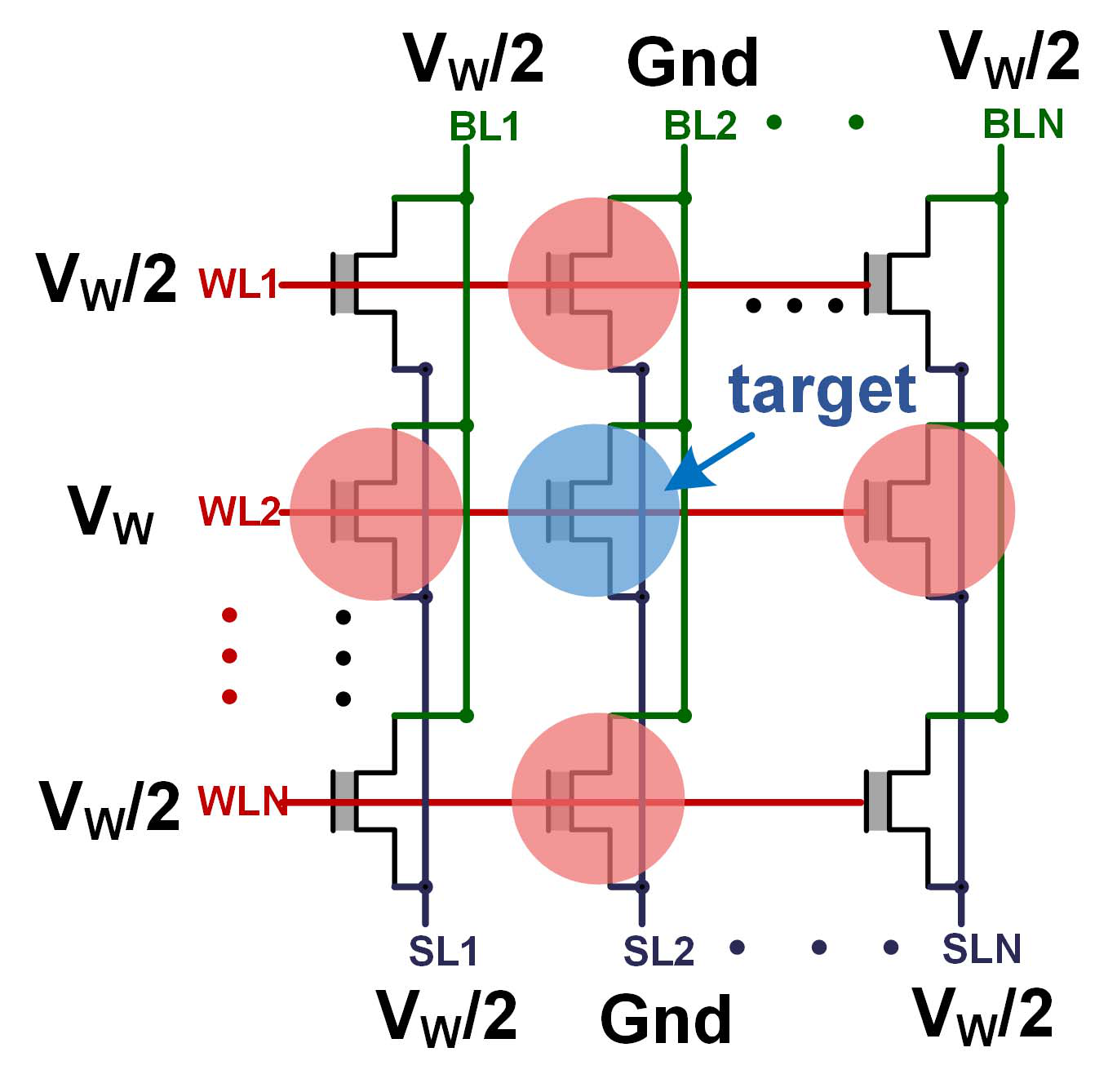
bulk of HZO. Pinpointing the exact charge trapping location phic computing.

needs further investigation in the future.

Fig. 9 shows the energy band diagram during +4 V erase/−4 V program. The electric field distribution in each layer is based on simulation results shown in Fig. 5. Electron/ hole trapping is also included. It is likely that oxygen vacancy acts as a shallow electron trap (∼1 eV below HZO conduction band), while oxygen interstitial acts as hole trap (∼1 eV above HZO valence band) [13], [14]. Process optimization of FE dielectric without compromising FE property is critical for high-speed FeFET memory application.

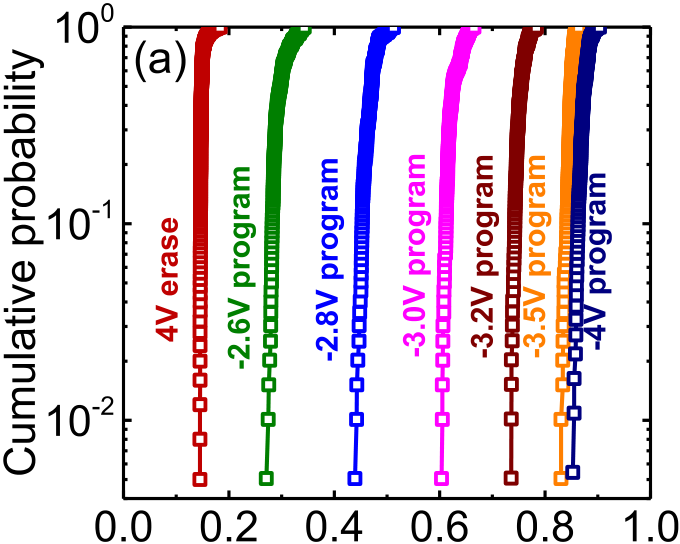
The cycle-to-cycle variations are shown in Fig. 11(a). The erase amplitude is kept at 4 V, and program amplitude is varied. A well-tempered distribution is obtained, indicating excellent cycle-to-cycle variation in HZO FeFET. Fig. 11(b) shows the charge trapping effect on *V*TH distribution by vary-ing erase/program-to-measurement delay, as defined in Fig. 6. With charge trapping, the distribution shifts, narrowing MW.

When FeFETs are configured into an AND array, we expect write disturbs affecting the cells that share the same word line or bitline as the accessed cell, as illustrated in Fig. 12(a).



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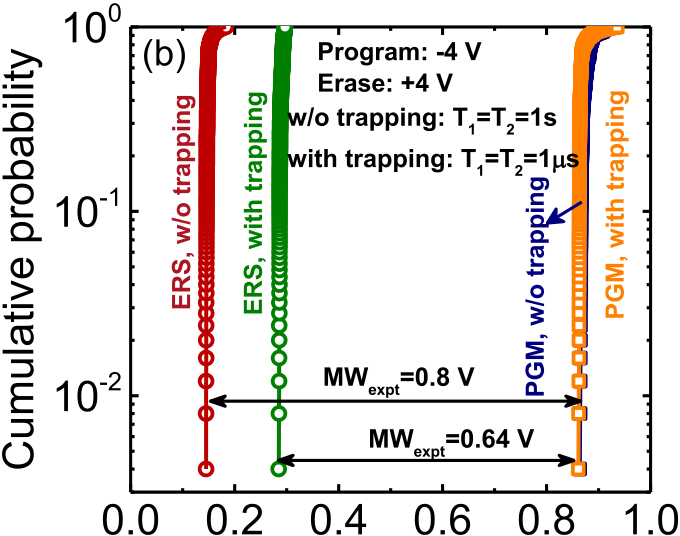




Fig. 11. (a) Cycle-to-cycle VTH variation for different program ampli-tudes. (b) VTH distributions with and without trapping. Charge trapping narrows the MW. W/L = 20/0.8 *μ*m.

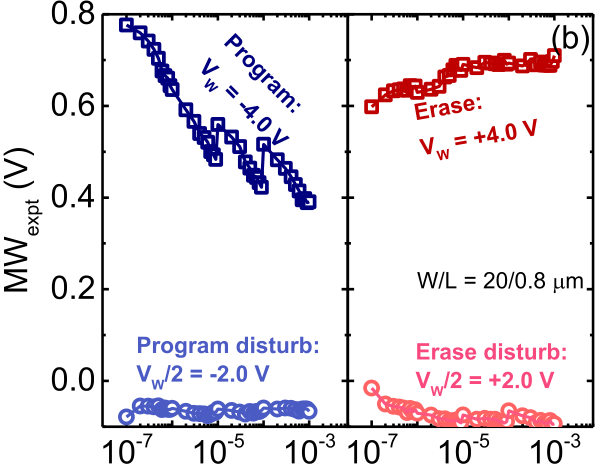
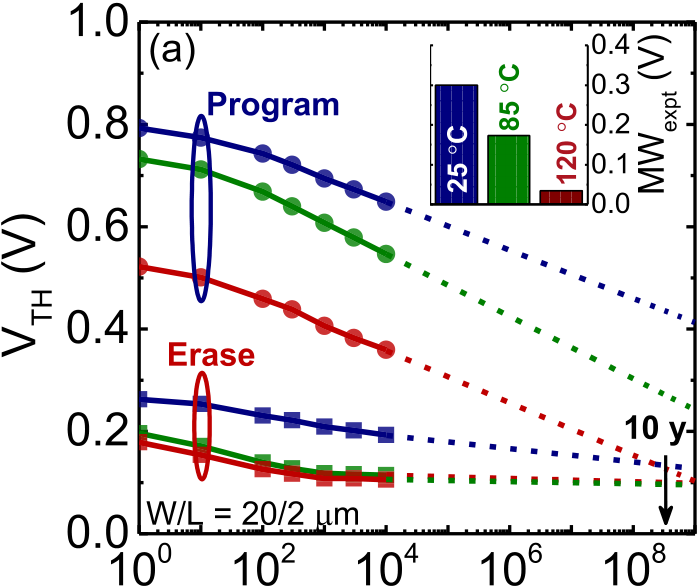


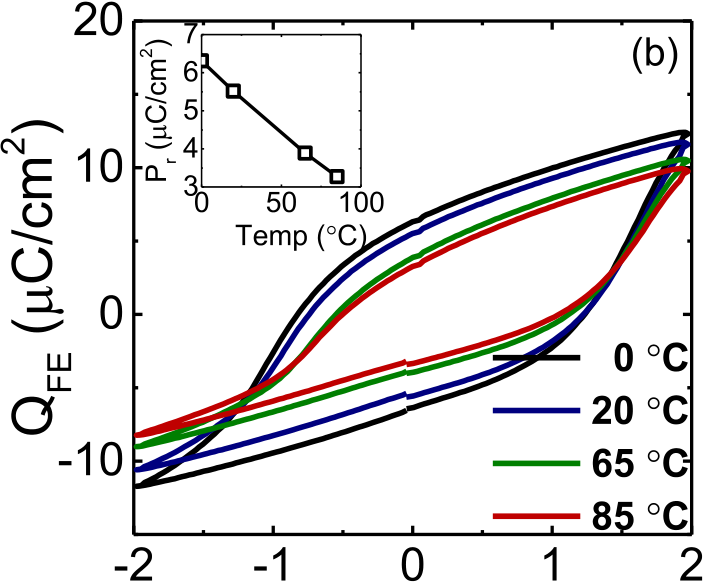
 

Fig. 12. (a) VW/2 write scheme in an and array to reduce write disturb for half-selected cells, which only experience ±VW*/*2. (b) MWexpt as a function of pulsewidth. FeFET is free from disturb for VW/2. The abrupt MW jump at certain PW is caused by single-domain switching.

Half-select (*VW*/2) is a popular write scheme to reduce disturb to those half-selected cells [15]. By applying this scheme, half-selected cells only experience ±*VW*/2, well below that







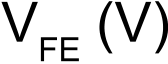


Fig. 13. (a) VTH during retention after program/erase at different temperatures. Low VTH state remains almost unchanged, but high VTH state degrades during retention. (b) Polarization decreases with increase of temperature, which reduces the MW at high temperature.

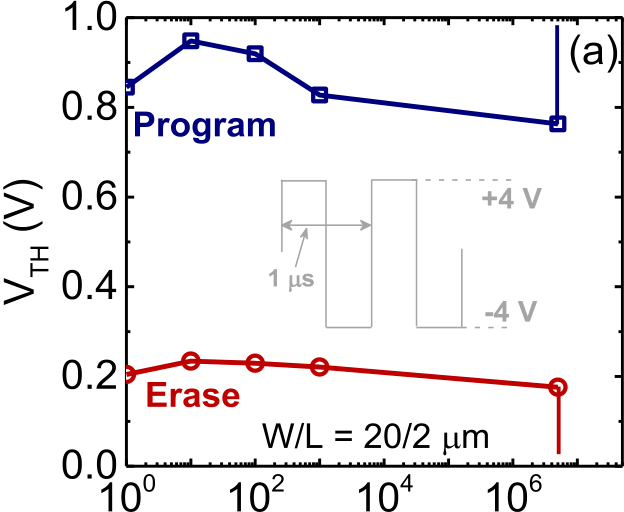
for polarization flip. To verify this, Fig. 12(b) shows the MW as a function of program/erase pulse width. As the program pulse width increases, MW decreases due to accumulation of hole trapping. Interestingly, an abrupt jump in MW, which is caused by *V*TH jump after program, is also observed [16]. The missing of abrupt jump after erase is likely related with the electric field asymmetry in the FE or the nucleation site difference during program and erase [17], and needs further investigation. For both erase/program, no disturb is observed for *V*W/2, suggesting write disturb-free FeFET NVM array.

Fig. 13(a) shows the retention performance of HZO FeFET at different temperatures. MW decreases when the temperature increases, due to decrease in polarization with temperature, as shown in Fig. 13(b) [18]. When extrapolated to 10 years, the device can retain its state at 85 °C. The relatively low and thin IL (0.8 nm) reduces the depolarization field within permittivity of HZO (*ε*FE = 30) compared with perovskite FE, the FE and enhances the retention [19]. Two factors affect MW degradation, depolarization field, and charge trapping, enhanced by the IL field [19]. Note that the low *V*TH state remains unchanged, whereas the high *V*TH state degrades during retention, similar to Si-doped HfO2 FeFET [18]. This suggests that depolarization field may play a minor role since, otherwise, it affects both the high *V*TH state and low *V*TH state. It is likely that charge trapping during retention makes



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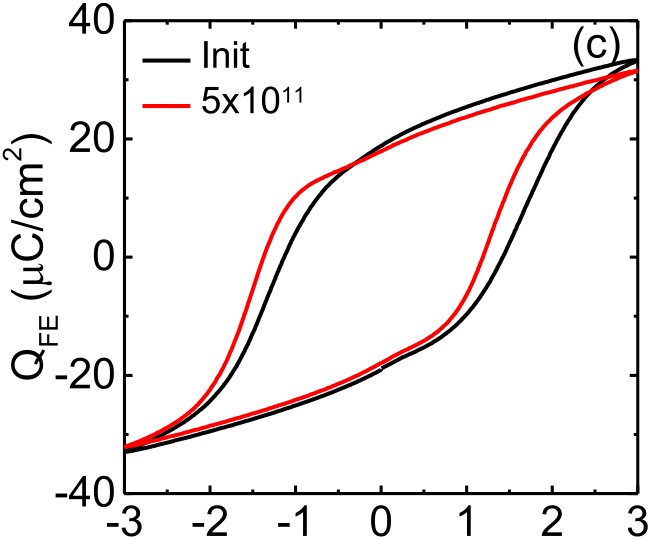
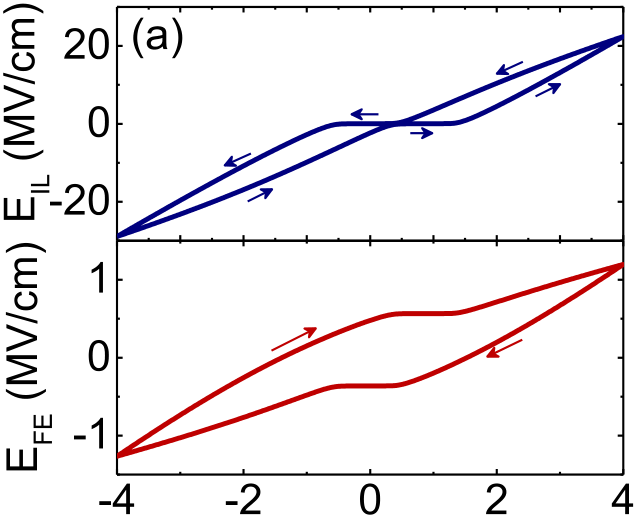




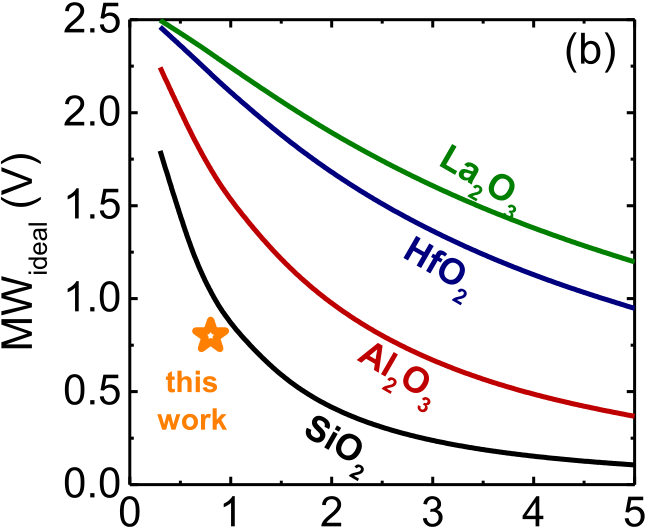
Fig. 14. (a) FeFET endurance is limited to 5×106erase/program cycles, followed by gate dielectric breakdown. (b) Endurance of MFM capacitor up to 1012cycles. (c) MFM QFE–VFE loop shifts negatively with cycles, showing imprint after cycling.

the most contribution to retention loss. This is because during retention after program, the device is in accumulation, which leads to hole trapping in high *V*TH state due to high IL electric field as shown in Fig. 15(a). But during retention after erase, it operates in depletion and causes negligible electron trapping in low *V*TH state. If the low *V*TH state is normally ON, the device is in inversion during retention, which would lead to electron trapping, and thus the degradation in low *V*TH state, as observed in [18]. Therefore, the device *V*TH could affect the retention performance.

The endurance performance is shown in Fig. 14(a), where the MW is 0.6 V after 5 × 106cycles, followed by abrupt dielectric breakdown. The FeFET was partially waked up with a −4 V,1-ms program pulse followed by a +4 V, 1-ms erase









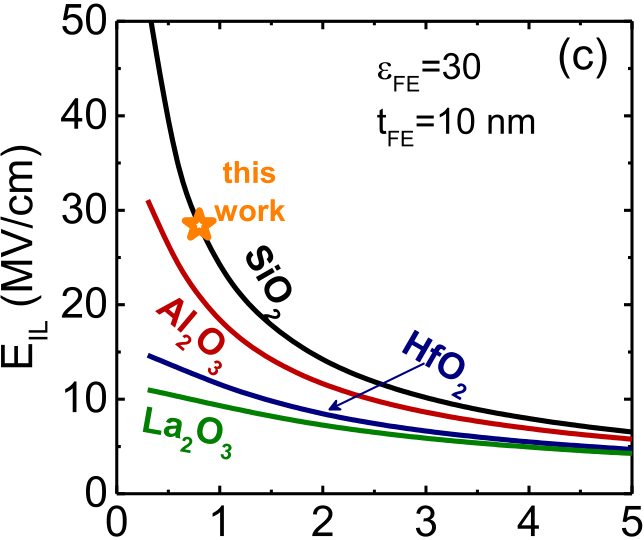




Fig. 15. (a) Electric field distribution for 1-nm FE/0.8-nm SiO2 IL stack, EIL *>* 25 MV/cm (degrades reliability), while EFE ∼ 1 MV/cm (reduces MW). (b) Simulated MW and (c) maximum EIL as a function of IL composition/thickness.

pulse prior to the endurance test. The high *V*TH state increases initially due to further FE wake up and then degrades gradually due to hole trapping. To understand the intrinsic endurance property, further endurance tests on MFM capacitors were conducted. The capacitors were fully waked up before the endurance tests with 1000 cycles, 3-MV/cm pulses. Tests with 2.5-MV/cm pulse show that polarization remains unchanged up to 1012cycles, as shown in Fig. 14(b). Note that during the cycling, only partial polarization is switched, due to the high-frequency pulses applied. However, it has a great implication for the intrinsic endurance property of FeFET, since only par-tial polarization is switched in FeFET, not the full polarization. The *Q*FE–*V*FE loop shifts negatively, showing imprint after cycling. Since the FE electric field is only around 1 MV/cm

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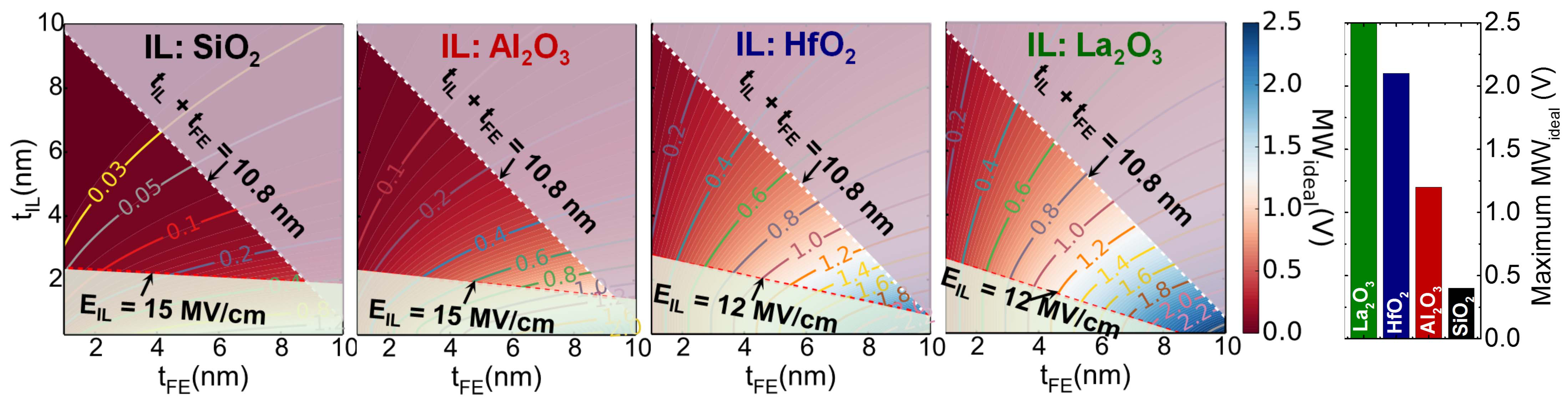


Fig. 16.

La2O3 and HfO2 and EIL ≤ 15 MV/cm for Al2O3 and SiO2. (b) Maximum MW satisfying all the constraints for four different IL dielectrics. *ε*FE kept at 30 is used for all thicknesses of HZO. (a) Design space exploration for four different IL dielectrics, bounded by constraints: 1) tIL + tFE ≤ 10.8 nm and 2) EIL ≤ 12 MV/cm for

for FeFET with *V*G range of −4 V to 4 V, as shown in Fig. 5(b), the FeFET endurance could be improved. Currently, FeFET endurance is limited by dielectric breakdown, which can be improved by optimizing the electric field in the gate-stack [20], [21].

and 2) increased *E*-field in the IL that not only causes charge trapping reducing MW, but also causes early dielectric breakdown. A pragmatic FE/IL stack design is proposed which would significantly enhance MW, retention characteristics, and cycling endurance in the future FeFET NVMs.

D. IL Design Criteria REFERENCES

Fig. 15(a) shows that the limitation in the measured MW (∼1/3 of the maximum MW) and in the retention and endurance performance (due to dielectric breakdown) funda-mentally arises from uneven electric field distribution in the stack (which is small in the FE and high in the IL). The small electric field in FE causes it to operate on an inner loop, which decreases the MW. The high electric field in IL enhances charge injection from channel and accelerates IL breakdown. We present a holistic design study of gate-stack for future FeFET memory, where the field distribution is re-engineered. Fig. 15(b) and (c) shows the calculated MW and IL electric field for different IL candidates. Increase of IL dielectric constant improves the MW and decreases the IL electric field at the same time.

Fig. 16 shows the MW design space exploration for different IL thicknesses, FE thicknesses, and IL compositions. Two design constraints are imposed: 1) *t*IL + *t*FE ≤ 10*.*8 nm and 2) maximum IL electric field ≤15 MV/cm for SiO2 and Al2O3, and ≤12 MV/cm for HfO2 and La2O3. The first constraint arises from process integration requirement in advanced nodes. The second limit is imposed by the maximum field across IL. The results show that the MW widens with thicker FE and thinner IL with higher permittivity.

V. CONCLUSION

In summary, HZO FeFET NVM is fabricated and char-acterized, and critical role of IL in determining memory performance is elucidated. We show both the thickness and permittivity gap between the HZO FE (*t*FE = 10 nm and *ε*FE = 30) and SiO2 IL (*t*IL = 0*.*8 nm and *ε*IL = 3*.*9); the electric field is nonuniformly distributed across the stack leading to: 1) lower voltage across FE causing polarization switching along nonsaturated hysteresis loops that reduce MW

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Authors’ photographs and biographies not available at the time of publication.