FeFET: A versatile CMOS compatible device with game-changing potential

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***Abstract* — With the discovery of ferroelectricity in HfO2 based thin films and the co-integration of ferroelectric field effect transistors (FeFET) into standard high-k metal gate (HKMG) CMOS platforms, the FeFET has emerged from a theoretical dream to an applicable reality. This paper summarizes the status of GLOBALFOUNDRIES FeFET technology and some of its potential applications. We show excellent 0.12µm2 SRAM yields of our mature 28nm CMOS platform, with co-integrated FeFETs, exhibiting a solid memory window of 1.4V. In contrast to conventional embedded memory cells, the FeFET can be integrated like a regular 26Å EOT transistor, exhibiting two reversibly programmable VT states, while offering full design flexibility. We show state of the art across wafer VT variability of the programmed and erased states of the FeFETs and discuss its**

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| **layout-dependence.** | **Embedded** | **size-competitive** | **FeFETs** |

**already allow solid separation of the memory states, approaching a mature 6Sigma distribution. Reasonable endurance and stable data retention are demonstrated. Moreover, an outlook of this technology beyond the von Neumann computing will be discussed, considering some of the various applications of this new, versatile device.**

***Keywords—* FeFET, eNVM, HKMG, neuromorphic**

comparable to standard FETs. The field-effect driven, reversible switching of VT states only requires pulses in the nanosecond-, sub |5V|-range with no large currents. Sub-critical pulses offer an additional horizon for accumulative switching [8], making this technology especially interesting for spiking neural network design applications.

II.FEFETMODULE IMPLEMENTATION

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| The | FeFETs | are | incorporated | into |

GLOBALFOUNDRIES 28nm gate first HKMG CMOS platform (28SLP) using a simple dual mask patterning module, as shown in Fig. 1. Two optional implant masks can be used for independent device tuning.

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|  | Fig.1. Schematics of the FeFET technology process | | | |
| flow. | Two | to | four |
| additional masks are used on top of the CMOS baseline. | | | |

I.INTRODUCTION The FeFETs comprise a 0.8nm thick SiO2 interfacial

The discovery of ferroelectricity in doped hafnium oxide (e.g. Si:HfO2) in 2007 and first report in 2011 [1] paved the way for the co-integration of hafnium oxide based ferroelectric field effect transistors (FeFETs) within 28nm HKMG bulk CMOS [2] and 22nm HKMG FDSOI CMOS [3] platforms. The vision of an ultralow-power nonvolatile memory offering, fast read/write access and high cost effectiveness has come closer to the long envisioned [4] manufacturing reality. AND architecture FeFET-based arrays are on their way to offer cost competitive and low power alternatives to classical embedded NOR-Flash (eFLASH) in the established MCU markets. Moreover, the FeFETs are also increasingly drawing the attention of the emerging neuromorphic and analog-in-memory computing sectors. In contrast to classical eFLASH cells, FeFETs are not bound to stringent array structure and do not require complicated strap cells. Like CMOS devices, FeFETs can be dimensioned in transistor width, gate length and can be flexibly intermixed with standard CMOS FETs offering a true in memory computing solution. Whereas BEoL embedded, memristor-based eNVM cells often only offer small resistance changes, which require sophisticated, area and power consuming sensing schemes, FeFETs exhibit a current swing

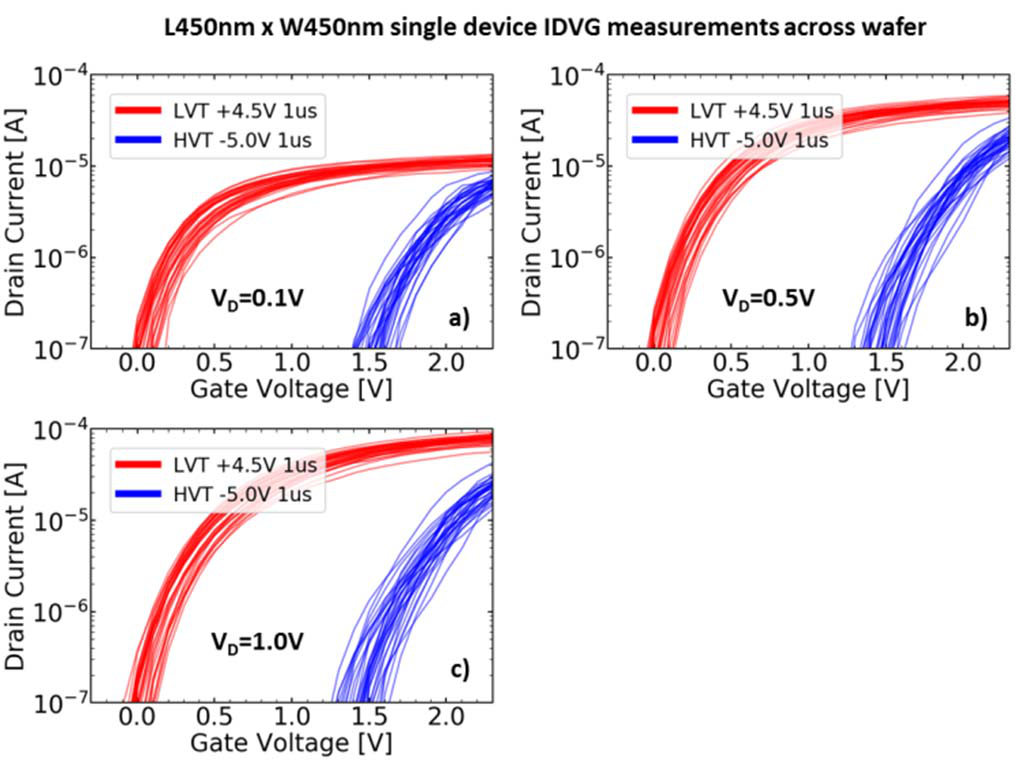
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oxide followed by an 8 to 10nm thick, ferroelectric doped HfO2, capped with a TiN metal cap and silicided poly

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| silicon, shown in Fig. 2.  Fig.2. TEM cross-section of an embedded FeFET, comprising a ferroelectric 9nm thick doped HfO2. |  |

The integration of the FeFET module is done minimal invasive such that the standard CMOS devices are already close to platform specifications. Accordingly universal curves for the standard core devices are shown in Fig. 3. The BEoL properties are completely independent of the FeFET module insertion. As we continuously improve the properties of the embedded FeFETs, also the CMOS D0 of the 28SLP-FeFET technology and the CMOS device matching to 28SLP platform specifications is subject of ongoing improvement.

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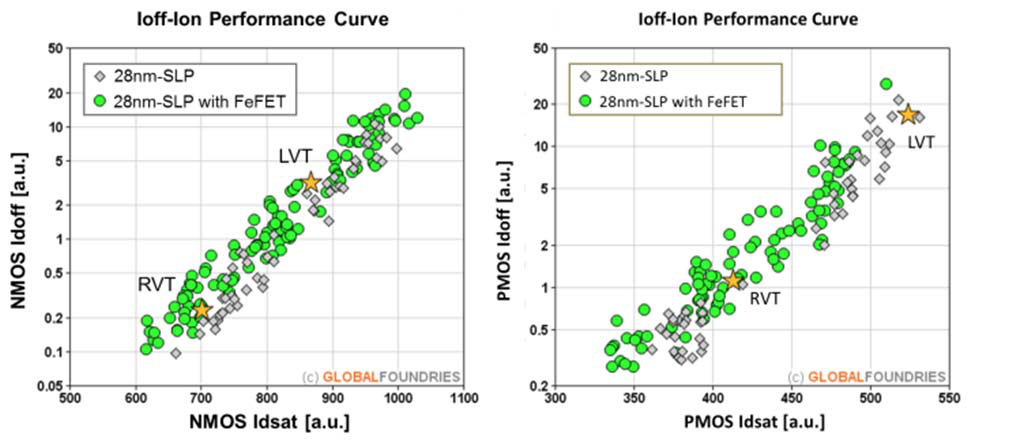


Fig.3. Standard thin gate oxide (SG GOX) 28SLP CMOS transistor performance of the 28SLP-FeFET technology, respective to 28SLP platform specifications.

Our 24Mb 0.12µm2 6T SRAM yield is at a stable >90%, close to mature D0 values on the 28SLP-FeFET technology (Fig. 4). Random logic test macros do confirm the D0 numbers extracted from the SRAM.

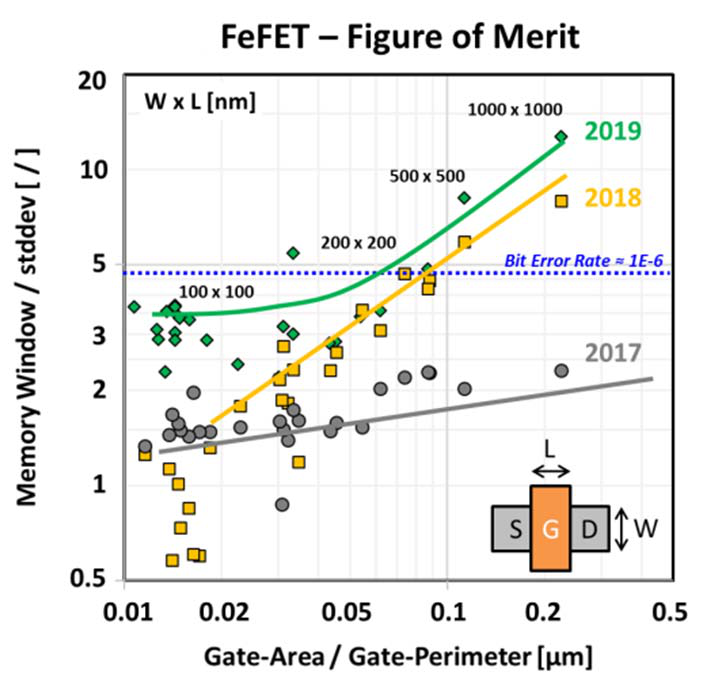
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|  | Fig.4. | 24Mb | | 28SLP | | standard | |
| 0.120µm2 6T SRAM yield map with co-integrated FeFETs. Bin1 reflects 24Mb fully functional at nominal | | | | | | |
| voltage, | without | | | repair. | | The |
| example shows 92.5% bin1 yield that are very close to the mature D0 | | | | | | |
| levels | of | the | 28SLP | | CMOS | |
| platform. | | | | | | |

III.FEFETDATA

The embedded FeFETs exceed the capabilities of classical eNVM-cells. It rather resembles a new type of transistor with ~26Å equivalent oxide thickness (EOT), exhibiting two stable, but reversible VT states. Using <|5V|, <10µs rectangular pulses, a FeFET can be switched from “low-VT” (LVT) to “high-VT” (HVT) state. The optimal pulsing conditions, for maximum separation of the two states, i.e. memory window (MW) and the variability of the VT is dependent on the gate length and width. The GLOBALFOUNDRIES FeFET technology in the 28SLP platform has FeFET devices with MW up to 1.7V [5], close to the theoretically maximum MW. Fig. 5 shows 1280 stacked single device IDVGs with extracted VTs at 1µA with

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|  | Fig.6. Across wafer stacked IDVG curves | | | |
| of | stripe | | patterns |
| programmed | | | into |
| 63bit | | L=450nm, | |
| W=450nm of FeFET passive mini arrays, | | | |
| co-integrated | | | in |
| 28SLP. | | | |

Without CMOS co-integration, memory windows up to 2.9V have been demonstrated for FeFETs possessing a 20nm ferroelectric film [6]. For co-integrated FeFETs we are continuously reducing FeFET-device variability over the last years, as demonstrated in Fig. 7 by plotting the memory window normalized to its standard deviation as a figure of merit for memory state separation.

strongly depends on the FeFETs Gate size and geometry. The overall variability control is under improvement. FeFET

continuous   
 VT   
Fig.7. The memory   
window of 128 single   
devices x-wafer,   
divided by   
 the standard deviation,   
shown as figure of   
merit. The FeFET   
NVM capability

As shown in Fig. 8, staying within the 1.2V VGS and 1.0V VDS regime, FeFETs behave like ordinary transistors in its LVT and respective HVT state, exhibiting normal ID scaling with VDS.

across wafer statistics for the CMOS co-integrated FeFETs   
(L = 450nm x W = 450nm)., where in Fig. 6 a global wafer   
view of same IDVGs are plotted.

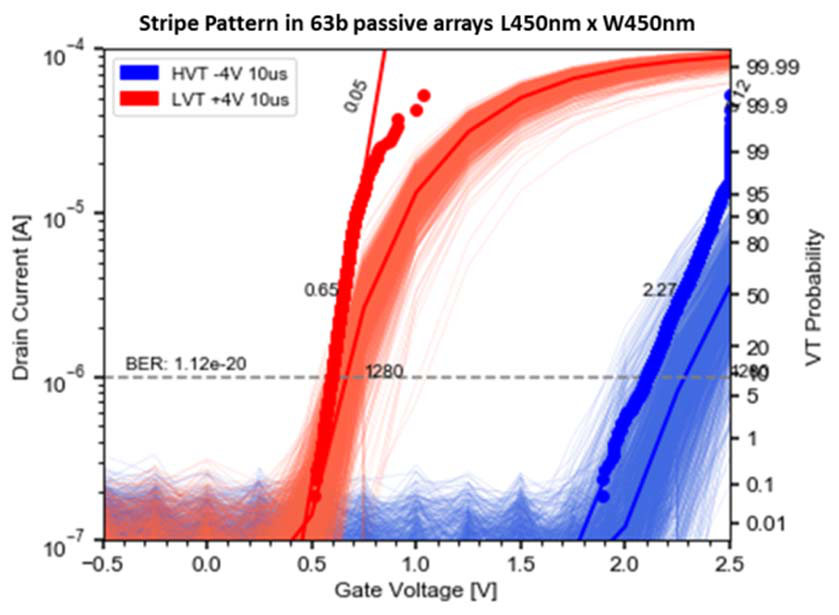


Fig.5. IDVG curves and cumulative probability plot of extracted VT from stripe patterns programmed into 63bit passive mini arrays, exhibiting across wafer variability of 1280 stacked FeFET-CMOS co-integrated devices (L =450nm, W=450nm).

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| Fig.8. IDVG | curves for |
| different VDS in 28SLP | |
| embedded | FeFETs |
| (L=450nm x W=450nm),  programmed/erased with  +4.5V/-5V 1µs voltage  pulses. | |

Dependent on process conditions we can tune the energy barrier in this asymmetric device. Neglecting charge trapping related imprint effects, we can measure an effective energy barrier for the HVT to LVT and LVT to HVT transition as described in [7], using voltage accelerated retention. A programmed FeFET state using optimal write

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conditions is followed by a square pulse of variable amplitude of opposite polarity and variable duration. When 50% of the MW (opposite state VT shift) is reached, the device is considered as switched (see Fig 9a.). Fig. 9b shows an example of this so called ‘Halid-plot’ for two different split groups, where Fig. 10 displays the corresponding classical data-retention through temperature.

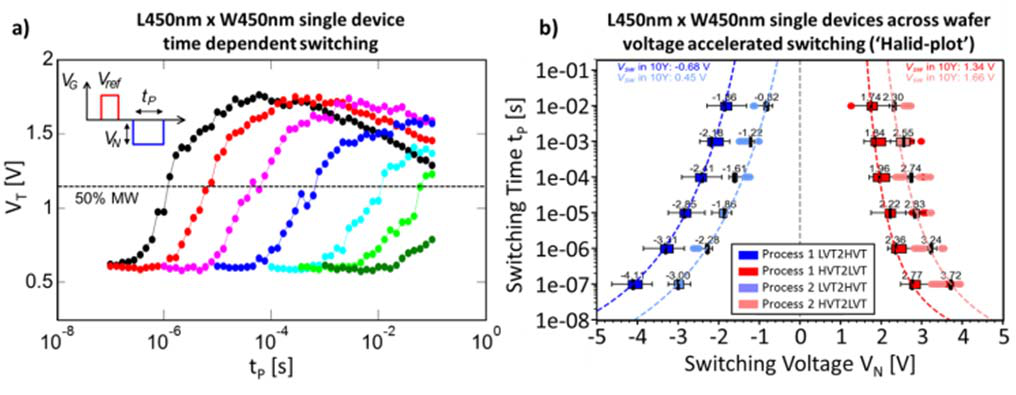


Fig.9. The inset in a) illustrates the pulsing scheme used to characterize the voltage accelerated switching, exhibited in the ‚Halid-plot‘ shown in b). For the LVT to HVT transition, after a solid pulse for setting the LVT state, a subsequent pulse with opposite polarity and varying voltage VN and duration tP is applied. A subsequent read determines if the VT of a FeFET surpasses 50% of the expected VT shift to the HVT state – if so, it is considered as ‘switched’. b) shows a ‘Halid-plot’ of L=450nm x W=450nm FeFETs for 2 different process conditions in the FeFET module. The blue data reflects the LVT to HVT and the red data is the HVT to LVT transition.

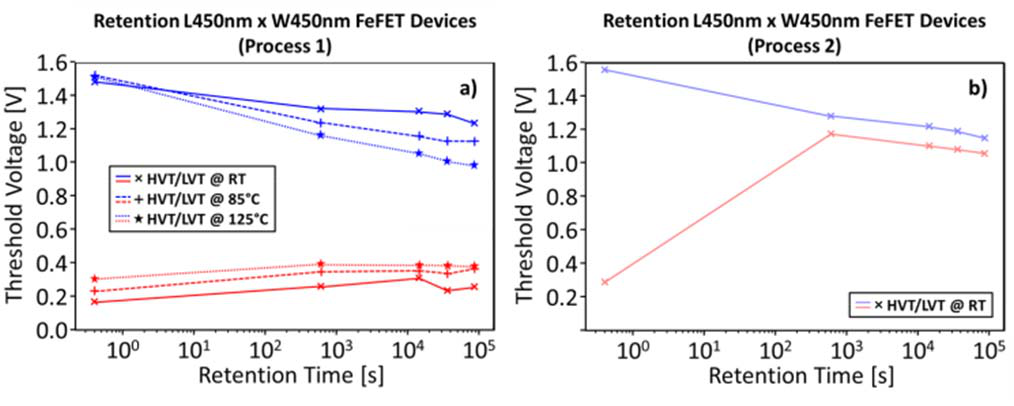


Fig.10. The FeFET retention of process 1 and 2 with mean program/erase VT evolution over time at different temperatures (25°C-125°C) of x-wafer L=450nm x W=450nm single device measurements. Retention properties correlate with the Halid-plot in Fig. 9, where a stable FeFET retention is illustrated for process 1.

The endurance of the FeFETs strongly depends on the pulsing conditions. With un-optimized symmetrical +/-4.0V for 10µs without a relaxation delay between opposite polarity pulses, the MW drifts over time, but endures at least ~104 cycles, as displayed in Figure 11. Using an on chip clock, allowing controlled pulses in the 10ns range, endurance >105 cycles have been demonstrated [2]. Theoretical material fatigue is not expected until at least 1011 cycles of endurance [11].

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|  | Fig.11. VT of 140 single device FeFETs across wafer (L=450nm x  W=450nm) through  cycling, using crude  symmetric -4.0/+4.0V 10µs back to back  pulses, without delays, or application of target programming schemes. |

Using large array test-chips, complex patterns can be written, using very short pulse-lengths <10ns [2]. Figure 12 and 13 show the latest status of a product like eNVM macro, running on the 28SLP-FeFET technology.

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|  | Fig.12. Digital fail bit- | | | |
| count | vs. | reference | |
| current | | of | 1Mb |
| measured on a large array eNVM macro, featuring L=450nm x | | | |
| W=450nm | | FeFETs., | |
| erased with -4.5V 10µs and programmed with +5.0V 10µs (external supply). | | | |

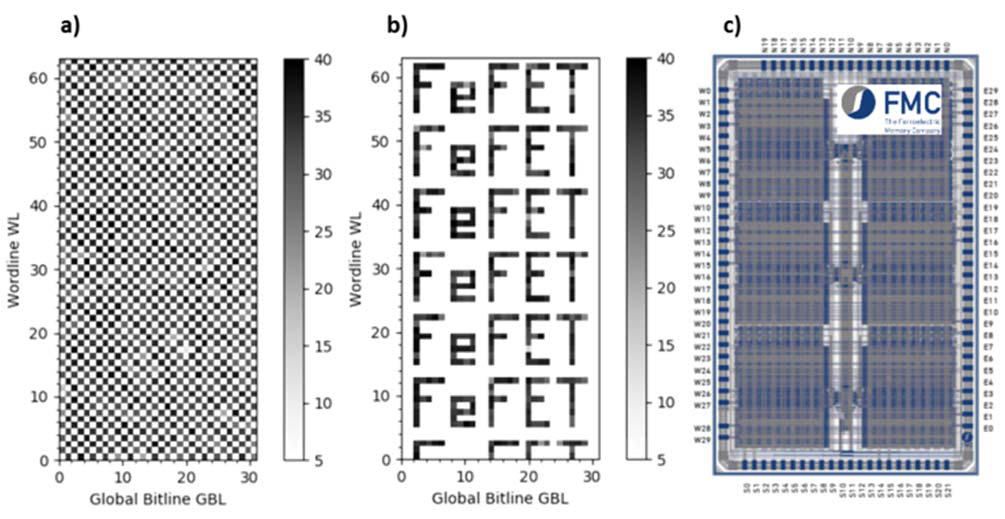


Fig.13. VTs (Currents) extracted in DMA mode of a) physical checkerboard and b) complex pattern. These patterns have been written into a test-chip, comprising various cells summing up to a total of 10Mb as c) processed on our 28SLP-FeFET technology.

In contrast to classical eFlash based eNVM cells, FeFETs can be flexibly co-located with standard logic gates as shown in Figure 14.

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| Fig.14. a) STEM cross section of a 2T NOR structure, comprising a mix of SG FETs and FeFETs.  b) top view close-up of the passive 2T-NOR | |  |
| array | design |
| dimension. All values | |
| are | physical |
| dimensions. | |

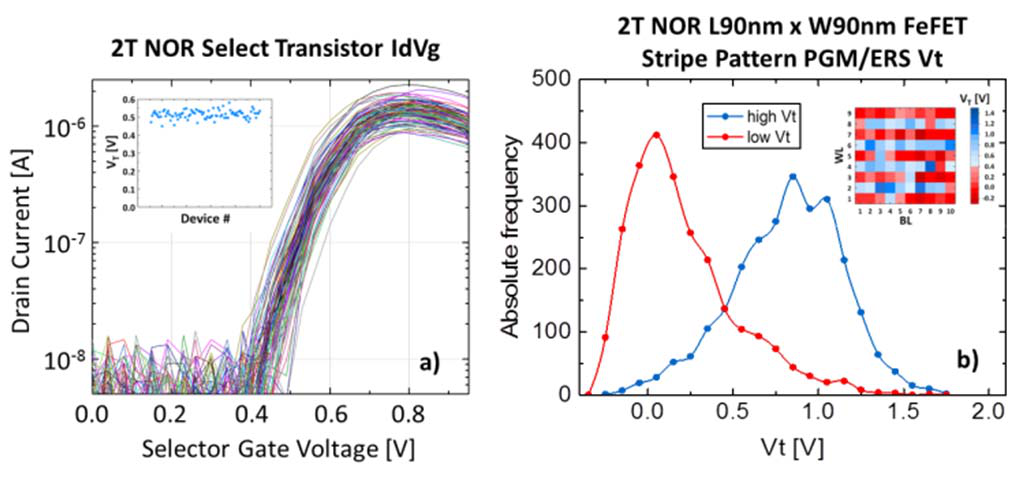


Fig.15. a) shows the IDVG set of the regular SG logic FETs, for one selected 2T NOR array, with the L = 90nm x W = 90nm FeFETs in series in programmed state. The inset shows the VTs extracted at 100nA of these logic devices.b) Extracted VTs at 100nA IRef of the L = 90nm x W = 90nm FeFETs of 29 stacked 2T NOR arrays, erased with -4.5V 1µs and programmed with +5.0V 1µs, using 1V inhibit voltage.

Figure 15 illustrates the cell performance under close proximity placements of FeFETs and regular logic gates. Even at overcritical design dimensions, the co-integration doesn’t have any significant impact on the general FeFET and logic device properties.

The VT of large, multi-domain devices can be tuned

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| through | choice | of | sub-loop | PRG/ERS | ferroelectric |

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switching pulses, as shown in Figure 16 [5]. On the contrary, the small, single-domain FeFETs exhibit the phenomenon of accumulative switching [8] as demonstrated in Figure 17.



Fig.16. Examplatory PRG and ERS VT transitions of an L = 450nm x W = 450nm single device FeFET. The VTs of these large multi-domain FeFETs can be fine-tuned by adaptive write conditions.

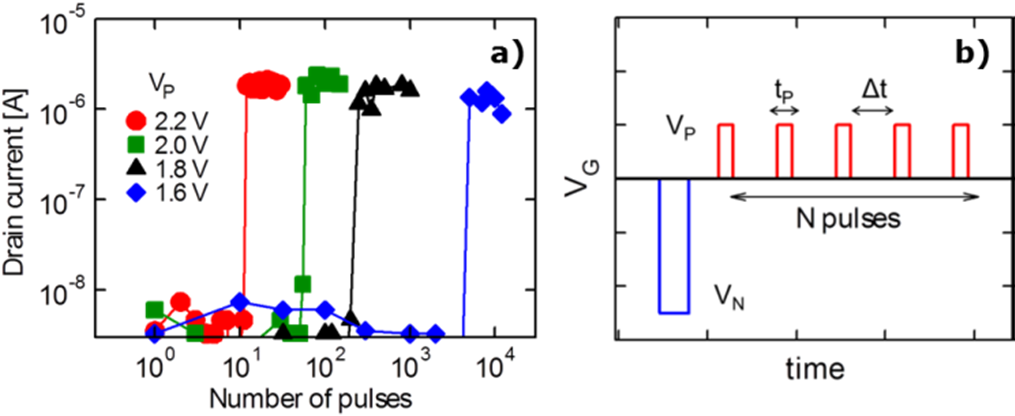


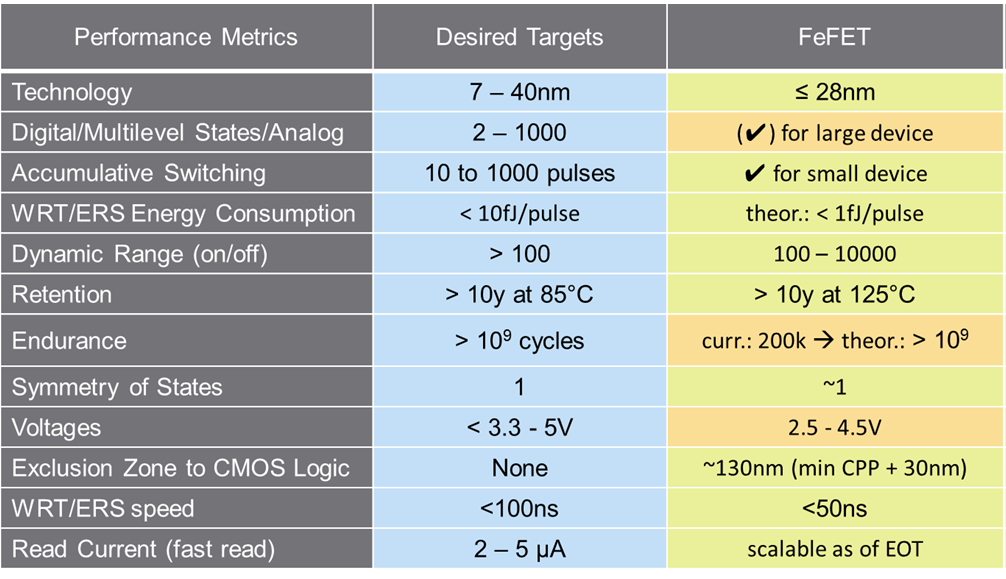
Fig.17. a) shows the ID of an L = 30nm x W = 72nm FeFET after solid ERS and subsequent a series of sub-loop switching PRG pulses with amplitude Vp and duration tP as illustrated in b). The behavior is highly repeatable and independent of Δt up to at least 1sec.

IV.FEFETAPPLICATION

Especially with respect to beyond conventional memory

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| --- | --- | --- | --- | --- | --- |
| applications | the | emerging | FeFET | concept | clearly |

outperforms other transistors based memory concepts, such as eFLASH. Besides the classical usage as cost effective, low power eNVM [2,3], the FeFET can be used for TCAM designs [9], as neuromorphic synapse [10], or capacitor-less “integrate and fire” neurons [8]. Especially for the promising new market of neural networks, the FeFET proves to be extremely attractive as shown in Table 1.



Tabale1. A benchmarking summary of FeFETs for neuromorphic architectures.

V.SUMMARY

We have introduced the GLOBALFOUNDRIES FeFET technology, embedded into the 28nm gate first HKMG low power CMOS platform 28SLP. We have shown close to mature 0.120µm2 SRAM yields and CMOS model matching,

with co-integrated FeFET process module. On the same silicon we have demonstrated the eNVM capability of larger FeFETs. Besides cost benefits the FeFETs open a range of applications far beyond classical eFLASH cells, due to its design flexibility, ultra-low power, low switching voltages, and fast switching speed. In addition, the phenomenon of accumulative switching makes it in particular interesting for the field of advanced neural networks. Despite the already convincing status, the technology is in continuous improvement, trying to approach the theoretical capability, scalability roadmap, and application specific metrics.

VI.ACKNOWLEDGEMENT

This work has been supported by funding from the Free State of Saxony, the European Regional Development Fund and the Federal Ministry of Economic Affairs and Energy.

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