**Re-examination of Vth Window and Reliability in HfO2 FeFET Based on the Direct Extraction of Spontaneous Polarization and Trap Charge during Memory Operation**

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***Abstract*—**We re-examine the dominant factors of the memory window (MW) and reliability of HfO2 FeFET using a new technique to extract both spontaneous polarization (Ps) and interface trap charges (Qt) by one-time current measurement of an FeFET during the memory operation. FeFET characteristics are strongly affected by unstable Qt (unrelated to ferroelectric) which causes Vth instability just after programming, and stable Qt which compensates most of electric(E)-field generated by Ps. Stable Qt is coupled to Ps with constant ratio (~90%), and reduce MW to the value much lower than the coercive voltage (Vc) limitation. Unlike the conventional model, Ps increase and stabilization are still effective to improve MW and retention, respectively. During cycling, MW is degraded by ∆Ps reduction as well as the increase of the compensation ratio (∆Qt/∆Ps) which can be mitigated by suppressing charge injection/ejection via interfacialSiO2.

**Introduction:** HfO2 FeFET has attracted much attention as a promising emerging memory because of its high speed/low voltage operation and CMOS compatibility. Recently, a huge amount of Qt at the interface close to 1014 cm-2 in FeFET has been reported [1, 2]. Although it has been suggested that the charge trapping affects Vth instability after programing (prog.) [2, 3], retention [3, 4], and the limited endurance [3, 5], the accurate amount of ∆Ps as well as ∆Qt during memory operation and their impact on the MW and reliability have not been understood yet. In this study, we extract both ∆Ps and ∆Qt directly from FeFET under various operating conditions. As shown in Fig. 1, we re-examine the dominant factors of the memory characteristics and reconstruct the improvement guideline.

**Results and discussions:** We measured poly-Si channel thin-film transistor with Si-doped ferroelectric (FE)-HfO2 of 10nm. Cross sectional TEMis shown in Fig. 1. The thickness of interfacial SiO2 is around 1.5nm. We newly developed a convenient analysis scheme that can extract both ∆Ps and ∆Qt during prog., retention and cycling from *one-time current measurement of a single FeFET* (no need for Hall measurement unlike [1]). Fig. 2 shows the concept of the analysis and the measurement sequence.

Vth shift after erase (Vg<0) /prog. (Vg>0) operation is shown in Fig. 3. Vth just after prog. shifts to the positive direction which is opposite to the expected direction, then Vth decreases drastically in about 10sec. After 1000sec, Vth increases again. The change of Ps and Qt caused by prog. and the subsequent time evolution derived from (1)-(4) (Fig. 2a) are shown in Fig. 4a. Qt larger than Ps is generated temporarily, but a part of Qt disappears within 10sec (I). After that, the state is stable until 1000sec, then Ps and Qt start to decrease together (II). From these characteristics, the charges produced by prog. can be divided into the unstable component which disappears in 10sec and the stable component which does not change until 1000sec as shown in Fig. 4b. These components are also clearly separated in the erase operation (Fig. 4c).

*Unstable charge trapping*:As shown in Fig. 4b, the unstable component is dominated by Qt. The positive Vth shift caused by prog. and the following Vth reduction with time are also observed in FETs with paraelectric-HfO2/SiO2 as shown in Fig. 5. So, the unstable Qt (electron trapping: e--trapping) originates in the defects unrelated to FE. In an FeFET, the E-field modulation due to the excessive e--trapping induces a small amount of the unstable Ps.

*Stable charge compensation of Ps at the interface*: In the stable component, Qt is quite large and close to Ps as shown in Fig. 4b. The correlation of Qt with Ps extracted by changing the prog. condition (Fig. 6a) is shown in Fig. 6b. ∆Qt is almost 90% of ∆Ps regardless of the prog. condition. This proves that the stable Qt completely follows the Ps and inevitably compensates the most of

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Ps. As illustrated in Fig. 6b, the following feedback would occur: Ps increases the E-field across SiO2 and causes e--injection, and consequently charge compensation at the interface decreases the E-field across SiO2, then high E-field across HfO2 is maintained even at large Ps. Fig. 7 shows the dependence of MW on Ps. Although the large Ps (> 10uC/cm2) is realized, only 10% of Ps contributes to MW because of the charge compensation. As a result, MW is proportional to Ps for a wide range. So, Ps increase still directly contributes to MW enlargement. This is significantly different from the conventional FeFET model (ideal situation) where Vc is the indicator of MW for such a large Ps.

*Impact of each component on Reliability*: Correlation of Qt and Ps is maintained even in the long-term retention (Fig. 8). Despite the E-field across SiO2 should accelerate e--injection via SiO2, Qt decreases with Ps reduction which is possibly caused by the depolarization field of FE-HfO2 as shown in Fig. 9. This means that the Vth shift in long-term domain is triggered by Ps change, not by charge injection. This is also different from the conventional model. To improve the retention, Ps stabilization is essential.

Fig. 10 shows the cycling characteristics. MW starts to reduce after 1k cycles (Fig. 10a). One of the origins for MW reduction is ∆Ps decrease (Fig. 10b). ∆Qt also decreases with ∆Ps but the ∆Qt/∆Ps ratio increases with cycling then reaches almost unity (Fig. 10b). ∆Qt/∆Ps ratio increase is critical, because ∆Qt/∆Ps ratio of unity vanishes MW even if the decrease of ∆Ps can be suppressed. To verify the possibility that the increase of ∆Qt/∆Ps originates in the stabilization of e--trapping unrelated to FE, Ig-Vg during erase at each cycle are compared in Fig. 11a. The peaks belonging to the e--trapping unrelated to FE disappear within 100sec even after the cycling. So, the larger ∆Qt/∆Ps ratio after cycling is not caused by the stabilization of the e--trapping unrelated to FE. As shown in Fig. 11b, ∆Qt is also proportional to ∆Ps even after 100k cycles. From these results, it is suggested that the trap sites which can compensate Ps stably increase with cycling as shown in Fig. 11c.

The excessive prog. stress which causes a larger amount of the unstable e--trapping (Fig. 12a) accelerates ∆Qt/∆Ps ratio increase, while the unipolar stress does not cause the degradation as shown in Fig. 12b. This means that the repetition of e--trapping/de-trapping via SiO2 caused by the unstable components induces the additional trap sites at the interface which can compensate Ps and indirectly affects ∆Qt/∆Ps ratio of the stable component. The charge trapping/de-trapping caused by the stable component itself presumably has more impact on ∆Qt/∆Ps ratio increase by cycling, because ∆Qt of the stable component is much larger than the unstable component as shown in Fig. 4b.

**Revised model and guideline:** Dominant factors of the memory characteristics are summarized in Fig. 13a. Compared to the conventional model assuming the ideal situation and additional charge trapping, a huge amount of Qt completely coupled to Ps strongly dominate the whole memory operation in the revised model as shown in Fig. 13b. Based on this model, we developed the improvement guideline: Ps increase/stabilization, and suppression of charge injection/ejection via SiO2, all of which are supported by the experiment data shown in Fig. 13c-e.

**Conclusions:** Behaviors of both Ps and Qt during FeFET memory operation were quantitatively revealed by the newly developed analysis. A huge amount of stable interface trap charges coupled to Ps significantly alters the operating model of FeFET memory. Ps increase and stabilization are still effective for MW and retention improvement, respectively. Suppression of charge injection and ejection via SiO2 is a key to higher endurance.

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| Fig. 1. Concept of this work. | | Fig. 2 (a) Concept of the analysis. ∆Ps and ∆Qt can be described by the measurable  parameters : ∆Vth, Qm and ∆QSi (equation (1)-(4)). (b) Measurement sequence to extract ∆Ps and ∆Qt during prog., retention and cycling. Triangle wave of Vg is applied twice to remove the leakage current. The ramp rate of Vg is 5000V/s. | | |
|  | Fig. 4. (a) ∆Ps and ∆Qt caused by prog. and the subsequent time evolution (b) Stable and unstable components of Ps and Qt generated by prog. (c) Ig-Vg during erase just after prog. and 100sec after prog. | | |  |
| Fig. 3. Time evolution of Vth | Fig. 5. Time evolution of Vth after prog. in FET with paraele-ctric HfO2/SiO2 gate dielectric. |
| after erase and prog. |
| Fig.6. (a) Measurement scheme to analyze prog. with Fig. 7. Dependence of  square wave. (b) ∆Qt-∆Ps for various prog. condition. MW on ∆Ps | | | Fig. 8. ∆Qt-∆Ps during retention process. (time domain II in Fig. 4a) |  |
| Fig. 9. Schematic of the Qt and Ps behavior during long-term retention process. |
| Fig. 10. Cycling characteristics Fig. 11. (a) Ig-Vg during erase just after prog. and 100sec after prog. at each cycle. (b) The relationship  (a) Vth (b) ∆Ps, ∆Qt and ∆Qt/∆Ps ratio. between ∆Qt and ∆Ps of the stable component after 100k cycles. (c) Schematic of degradation by cycling.      Fig. 12. (a) Impact of the excessive Fig. 13. (a) Comparison between the conventional model and the revised model. (b) Schematic  prog. stress on ∆Vth (Vth-Vth(before prog.)) of the dominant factors of memory performance and the guideline for the improvement. (c) MW  just after prog. and 100sec after prog. of the devices with different Ps and almost the same compensation ratio. (d) Dependence of Qt  (b) Dependence of ∆Qt/∆Ps ratio on and Vth on Ps during long-term retention. (e) Influence of the total amount of charge trapping/de-  cycles with various cycling conditions. trapping on the endurance. The data are obtained by the experiment shown in Fig. 12. | | | | |
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