

A FeFET based ultra-low-power ultra-fast embedded NVM technology for 22nm FDSOI and beyond

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***Abstract*—**We show the implementation of a ferroelectric field effect transistor (FeFET) based eNVM solution into a leading edge 22nm FDSOI CMOS technology. Memory windows of 1.5 V are demonstrated in aggressively scaled FeFET cells with an area as small as 0.025 µm². At this point program/erase endurance cycles up to 105 are supported. Complex pattern are written into 32 MBit arrays using ultra-fast program/erase pulses in a 10 ns range at 4.2 V. High temperature retention up to 300 °C is achieved. It makes FeFET based eNVM a viable choice for overall low-cost and low-power IoT applications in 22nm and beyond technology nodes.

**I.**  **INTRODUCTION**

Ferroelectric HfO2 [1] enables a scalable and CMOS compatible embedded non-volatile memory (eNVM), keeping pace with the scaling demands of leading-edge logic technologies (Fig. 1). We have developed an innovative and non-invasive eNVM process [2] applicable for HKMG technologies. The corresponding memory module is directly transferable into our 22nm planar FDSOI platform [3] where it proves scalability down to the 12nm technology node, while keeping the manufacturing costs very low since only two additional masks are required. Back-bias as a unique fully-depleted SOI (FDSOI) feature offers further opportunities for the FeFET operation and application. In a 28nm bulk technology, a 32 MBit memory array using 0.036 µm2 cells was tested to show robust pattern write and read capability. We demonstrate technology temperature data retention up to 300 °C.

**II.RESULTS AND DISCUSSION**

*A. 22nm and 12nm FDSOI platform*

Switching the polarization of the FeFET by applying a positive (*program*) or negative (*erase*) gate voltage pulse induces a stable but reversible threshold voltage shift depending on the orientation of the dipoles (low-*VT* and high-*VT*, respectively). These two distinguishable states of the device (Fig. 2), separated by the so-called memory window (*MW*), can be sensed with a short readout of the transistor's drain current.

A ferroelectric HfO2-based FeFET has been integrated into a 22nm FDSOI CMOS platform. Physical gate lengths are

24 nm and 20 nm which are required for 22nm and 12nm generations, respectively. Fig. 3 shows TEM cross sections of the FeFET implemented into the FDSOI process. Beside the memory device, cross sections of the logic devices are shown to illustrate the successful patterning of this SoC embedded technology. The 22nm baseline performance remains unchanged (Fig. 4).

Fig. 5 shows the *ID*-*VG* transfer characteristics of a *W*x*L*=80x20 nm FDSOI FeFET after applying positive and negative voltage pulses of 3.8 V for 10 µs. A clear counter-clockwise *VT* shift indicates ferroelectric switching in this highly scaled device (cell size is 0.025 µm²) and therewith proves the feasibility of a fully depleted FeFET technology as well as its scalability to the 22nm and 12nm FDSOI nodes. Besides the remarkably large memory window of up to 1.5 V, exceeding the state of the art 28SLP technology [2], the back-bias option available in FDSOI technologies offers further *VT* optimization (Fig. 6). Advanced trimming and targeting possibilities for this new memory concept during read can be used (Fig. 7). The coupling factor |d*VT*/d*VB*| of 75 mV/V of the back-biased FeFET is comparable to a standard logic device [3] and can be used for both positive and negative voltages.

Pulse duration and pulse amplitude can be traded depending on the aimed application field. For example, a low-voltage programming scheme with longer pulse durations can be used for non-speed critical but high density circuits. On the other hand ultra-fast high-performance tasks can be realized with rapid and high voltage pulses. Program/erase pulse times in the nanosecond range furthermore minimize the parasitic charge trapping, avoiding the artificial lowering of memory window [4] and enable immediate readout after write.

According to TCAD simulations a strong confinement of the electrical field in the interfacial/ferroelectric layer is expected from this fully depleted technology (Fig. 8). For ferroelectric switching a high field in the ferroelectric layer at low gate voltage is highly beneficial, since it reduces electrical field stress with improved endurance and enables denser low-voltage periphery circuits.

Endurance cycling (using +/−3.5 V, 10 µs) of the most aggressively scaled 20 nm devices shows a residual memory window of 0.4 V after cycling to 2x104 (Fig. 9). The result is comparable to previous data [2,4,5] obtained for the 28SLP platform and further optimization is expected from interface treatments [6].

*B.32 MBit Test Vehicle*

In order to analyze and optimize performance and yield of the FeFET cells a flexible 28SLP test chip is designed, which can be adapted to changes in the FeFET integration process. The chip comes with a competitive target cell size of 0.036 µm² and a memory size of 32 MBit per cell type. As shown in Fig. 10, the chip layout is composed of twelve instances of memory macros with different cell geometries. The internal control logic and the parallel 32 Bit bus allows a fast and robust read/write performance. A JTAG interface gives access to various timing, voltage and configuration settings. Three different types of sense amplifiers are implemented depending on speed and accuracy requirements. In addition each cell in the memory array can be directly accessed (direct memory access, DMA) in order to record transfer functions and verify program/erase operations.

*C.32 MBit Array Performance*

This basic device functionality was tested utilizing a 30 µs pulse 2 MBit sector erase and a 20 ns 2 kBit word program, including the 10 ns 4.2 V actual program pulse. The readout was done using a 50 ns drain-current sensing. Fig. 11 shows the sense amplifier readout of a complex and non-monotonic pattern written into the 0.036 µm2 cell 32 MBit array. The analog drain current readouts via DMA are illustrated in Fig. 12. From the comparison with the sense amplifier results from Fig. 11, it can be concluded that the peripheral logic works within the expected noise margin. The remaining bit error rate is affected mainly by defects as indicated in the wafer map in Fig. 13 rather than by ferroelectric instabilities of the memory cell itself.

The threshold voltage distribution of *W*x*L*=240x34 nm and *W*x*L*=500x500 nm single cells, measured with voltage sweeps in the millisecond range, is shown in Fig. 14. In contrast to on-chip-clock-controlled array operation, charge trapping cannot be suppressed in these measurements by using ultra short pulses. In general device geometries are not the smallest cell size possible on 28nm but were chosen to enable most robust memory operation, using up to 5 V program and erase voltage pulses. Data from three wafers with a die checkerboard measurement were used. A clear separation is visible for the larger FeFET dimension, whereas the smaller cell is currently still affected by charge trapping and needs further process optimizations. Tab. I summarizes the memory window and its variation for various device lengths and widths.

*D.Data Retention*

Retention reliability was studied by monitoring the stability of the two stored states as a function of bake time. Initially, a 64 kBit *W*x*L*=500x500 nm cell array was programmed in stripe pattern, so that half of the bits were in the low-*VT* and the other half in the high-*VT* states. Transfer characteristics (*ID-VG*) of all the devices were measured and a subsequent bake at different temperatures was performed.

Fig. 15 shows the time evolution of the two states after a cumulative bake at 250 °C up to 7 days. The high-*VT* state was taken as a reference. Only a decay of the low-*VT* state is visible. It can be observed that the major margin loss occurs within the first few minutes. Afterwards the separation of the states remains almost stable. Fig. 16 shows the transfer curve of the two states at room temperature and after a bake at 300 °C for 1 hour. Each readout corresponds to the mean value of a 32 kBit collected data points relative to one state whereas the error bars indicate the standard deviation stretch. Two main effects are visible: shift of both curves towards lower *VG* values and a closure of the memory window. The shift of both, the low-*VT* as well as the high-*VT* state could be readily explained by electron-trapping from energetic deep states that were populated during program/erase cycling. Nevertheless, this test still proves the stability of the two states at severe temperature stress.

**III.SUMMARY**

Our low-cost and ultra-low power FeFET based bulk HKMG technology eNVM module has been transferred into a 22nm fully depleted SOI technology keeping all unique features of FDSOI fully functional. The scalability from 28nm to sub-22nm is proven using just two additional masks over the 22FDSOI baseline. It is also shown that the electrical properties like memory window benefit from the improved electrostatics of the FDSOI technology. In addition, the unique feature of back-bias can be used in order to further tune the FeFET properties. Programming of complex patterns into a 32 MBit array with nanosecond range program/erase times, data retention up to 300 °C for 1 h and endurance up to at least 2x104 cycles has been successfully shown.

ACKNOWLEDGMENT

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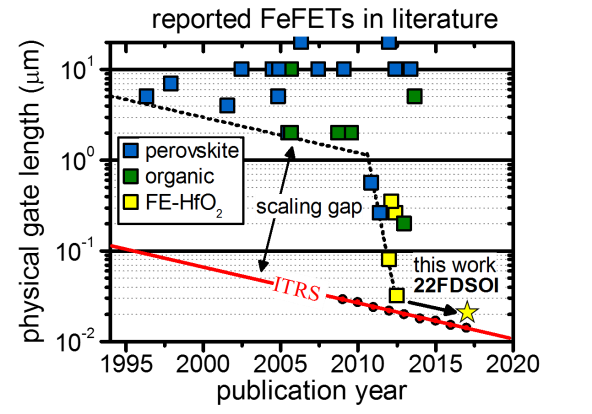
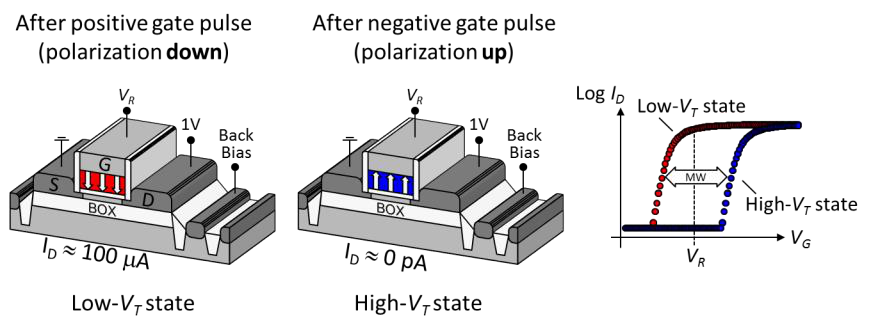
 

Fig. 2. The two non-volatile states of a FDSOI FeFET are realized by two stable

polarization states of the ferroelectric layer in the transistor. A positive or negative

Fig. 1. Physical gate length scaling of FeFET compared to voltage pulse at the gate can switch the polarization and hence the binary

the eNVM logic platforms. information. Readout is sensing the shift in the *ID-VG* curve.

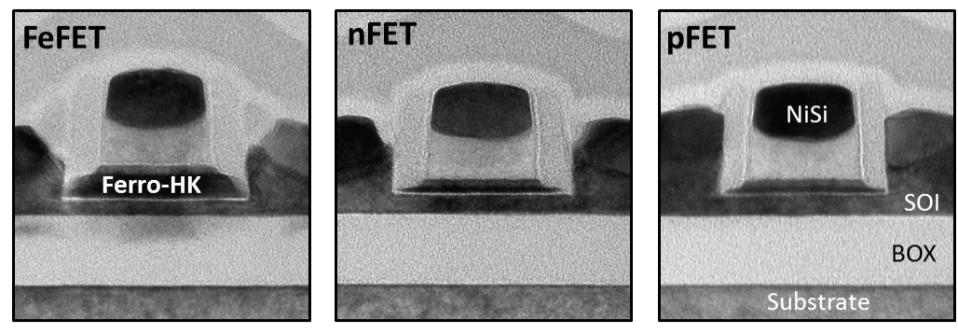
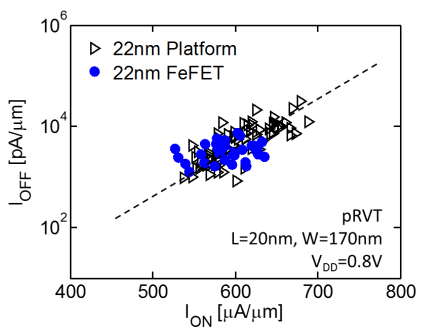
 

Fig. 3. TEM cross sections of embedded FeFET memory devices and logic n- and pFET Fig. 4. Logic pFET *Ion*-*Ioff* performance of the

integrated into the 22FDSOI Platform. 22nm eNVM technology is matched [3].

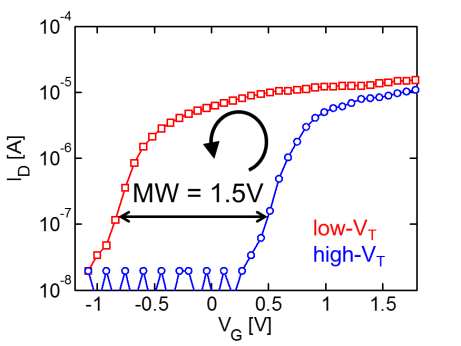
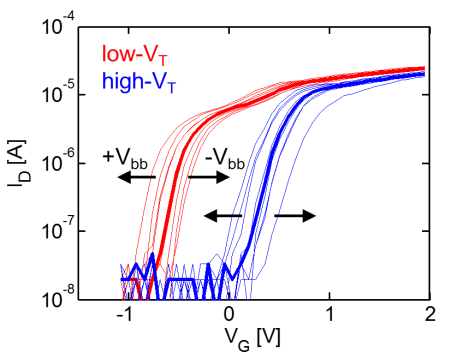
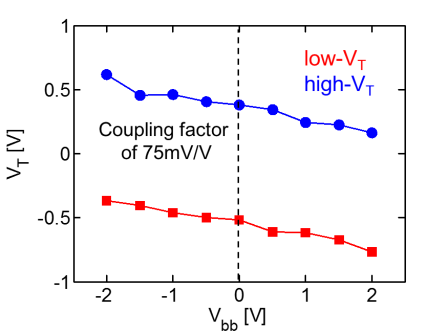
  

Fig. 5. Low- and high-*VT* (+/−3.8 V, 10 µs) *ID-* Fig. 6. Impact of back-bias on the *ID-VG*  Fig. 7. Impact of forward and reverse back-bias

*VG* curves of a subnominal *W*x*L*=80x20 nm curves of a standard *W*x*L*=170x24 nm on the *MW* readout of a *W*x*L*=170x24 nm FDSOI

FDSOI FeFET device. FDSOI FeFET device. FeFET device.

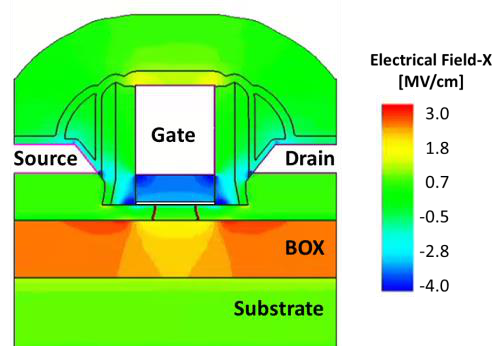
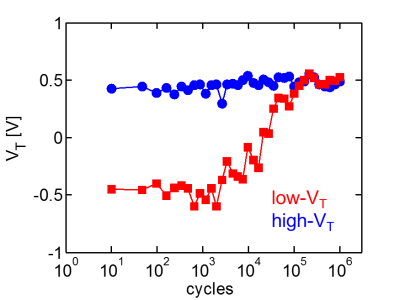
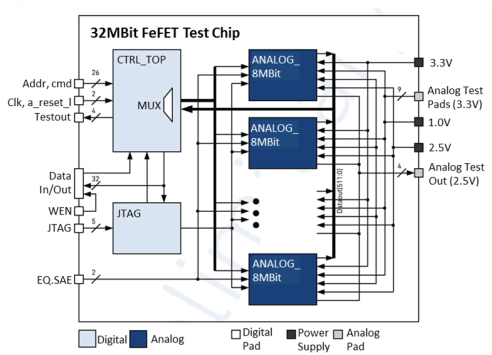
  

Fig. 8. TCAD electrical field distribution Fig. 9. Bipolar endurance cycling (+/−3.5 V, Fig. 10. 32 MBit test macro includes direct

within a ferroelectric FDSOI transistor 10 µs) of a *W*x*L*=170x24 nm FDSOIFeFET memory (DMA) & JTAG for direct cell readout,

(*VD*=*VS*=0 V, *VG*=−5 V, *VB*=floating). device. design verification and test debugging.

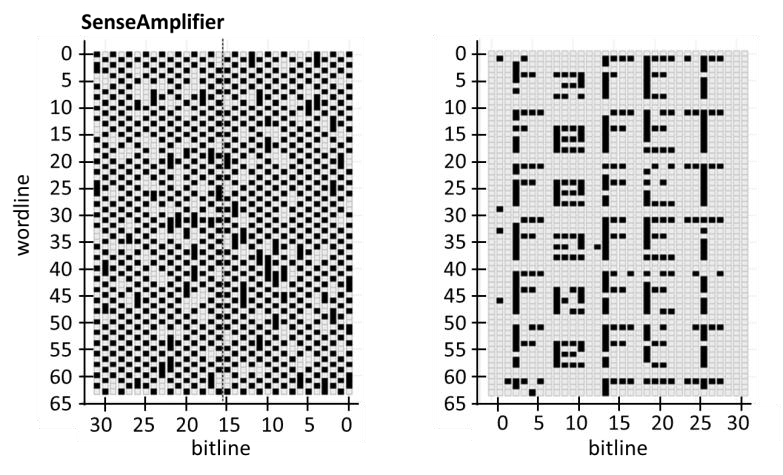


Fig. 11. Checkerboard (left) and complex pattern (right) are written into the 0.036 µm2 cell 32 MBit arrays Readout was done using a 50 ns current sensing.

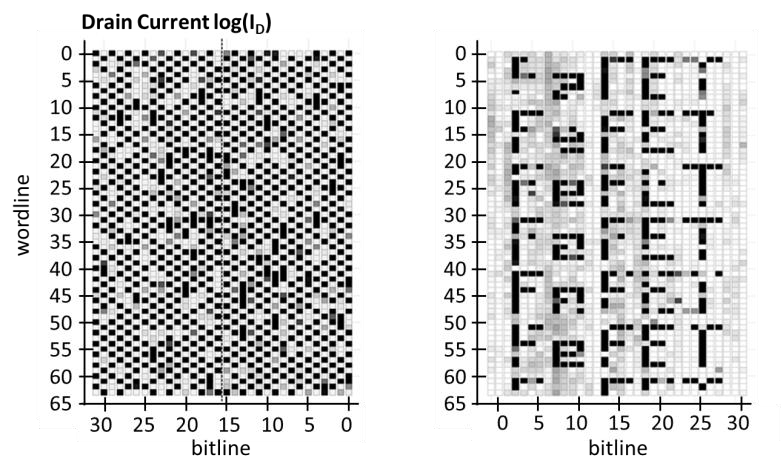


Fig. 12. DMA current readouts are matching the sense amplifier patterns from Fig. 11 within expected noise level of the used measurement equipment (grey scale representing log-current).

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Fig. 13. FeFET yield including logic yield is defect

limited and the focus of further process

optimizations.

Fig. 14. Threshold voltage *VT* distribution of the low- and high-*VT* state for a (a) *W*x*L*=500x500 nm and (b) 240x34 nm device. Stacked data is from three wafers checkerboard measurement (see inset) using millisecond voltage sweeps & 10 µs program/erase pulses, displaying a worst case trapping situation.

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|  | Fig. 15. Retention measurement of 0.28 µm2 cell 64 kBit array @ 250 **°**C. Degradation occurs within the first few minutes and remains stable for longer bake periods. | Fig. 16. Retention measurement of  0.28 µm2 cell 64 kBit array @ 300 **°**C after  1 h. A similar shift to lower *VT* is observed  for both low- and high-*VT* state. |
| Tab. I. Memory window and variation for FeFETs with different device dimensions. |