138 IEEE ELECTRON DEVICE LETTERS, VOL. 35, NO. 1, JANUARY 2014

Low-Leakage-Current DRAM-Like Memory Using a One-Transistor Ferroelectric MOSFET   
With a Hf-Based Gate Dielectric

Chun-Hu Cheng and Albert Chin, *Fellow, IEEE*

***Abstract*—The power consumption of capacitor leakage cur-rent, increase of the capacitor aspect ratio, and lack of higher dielectric constant (*κ*) material are the difficult challenges to downscaling dynamic random access memory (DRAM). This letter reports a new one-transistor ferroelectric-MOSFET (1T FeMOS) device that displays DRAM functions of a 5 ns switching time, 1012on/off endurance cycles, and 30 times on/off retention windows at 5 s and 85 °C. A simple 1T process and a considerably low OFF-state leakage of 3 × 10−12A/*μ*m were achieved. This novel device was achieved by applying ferroelectric ZrHfO gate dielectric to a p-MOSFET, which is fully compatible with existing high-*κ* CMOS processing.**

***Index Terms*—Ferroelectric, ZrHfO, 1T, DRAM, FeMOS, MOSFET, memory.**

I. INTRODUCTION   
**T** is the difficult challenge for dynamic random access HE search for higher dielectric constant (*κ)* material

memory (DRAM) [1]–[5]. Although SrTiO3 is promising because it contains a *κ >* 100, the dielectric thickness of the low metal/insulator barrier height (*ϕb)* must be increased to lower the leakage current [2]. This is the fundamental material-

related problem of high-*κ* dielectric materials, of which the *ϕb* decreases as the *κ* value increases. Nevertheless, the relatively

large thickness is difficult to fill into the smaller footprint

of the DRAM capacitor. Therefore, increasing the capacitor

height is one solution to continuous downscaling of the planar

size of DRAM cell, but the increased aspect ratio increases

the difficulty of fabricating the DRAM capacitor. Furthermore,

the power consumption from the capacitor’s leakage current

is a crucial concern of multi-Gb DRAM, which account for

a substantial amount of the total power consumption of a

system [6]. Therefore, a novel DRAM-like device with a low

leakage current and improved power consumption must be

invented.

However, this new memory device must satisfy the bench-

marks of a sufficiently large memory window, high endurance,

a long data retention time with an improved refresh cycle,

Manuscript received October 23, 2013; revised November 3, 2013; accepted November 4, 2013. Date of publication December 11, 2013; date of current version December 20, 2013. This work was supported by the National Science Council of Taiwan. The review of this letter was arranged by Editor L. Selmi. C.-H. Cheng is with the Department of Mechatronic Technology, National Taiwan Normal University, Taipei 10610, Taiwan.

A. Chin is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan (e-mail: albert\_achin@hotmail.com). Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2013.2290117

a fast switching speed, and a simple, inexpensive process for both commodity and embedded applications, to compete with existing DRAM.

In this letter, we present a DRAM-like one-transistor ferro-electric MOSFET (1T FeMOS) device with superior DRAM functions using a simpler capacitor-less 1T structure and a very lower off-current (3 × 10−12A/*μ*m) than those of existing DRAM devices, in addition to a 5 ns switch-ing time and 1012on/off endurance cycles. This low-power green device with DRAM functions was achieved using a p-MOSFET by applying a ferroelectric effect [7]–[10] to a thin high-*κ* ZrHfO gate dielectric. This Hf-based ferroelectric FeMOS has the extra merit of full process compatibility with a sub-32nm high-*κ* CMOS [11]–[14], which is distinct from conventional non-Hf-based ferroelectric gate dielectric MOSFETs using Pb(Zr,Ti)O3 (PZT), SrBi2Ta2O9 (SBT), and Bi3*.*75La0*.*25Ti3O12 (BLT) [7]–[9]. The process compatibility using Hf-based ferroelectric dielectric is the enabling technol-ogy to realize the 1T FeMOS proposed as early as 1999 [15].

II. EXPERIMENTS

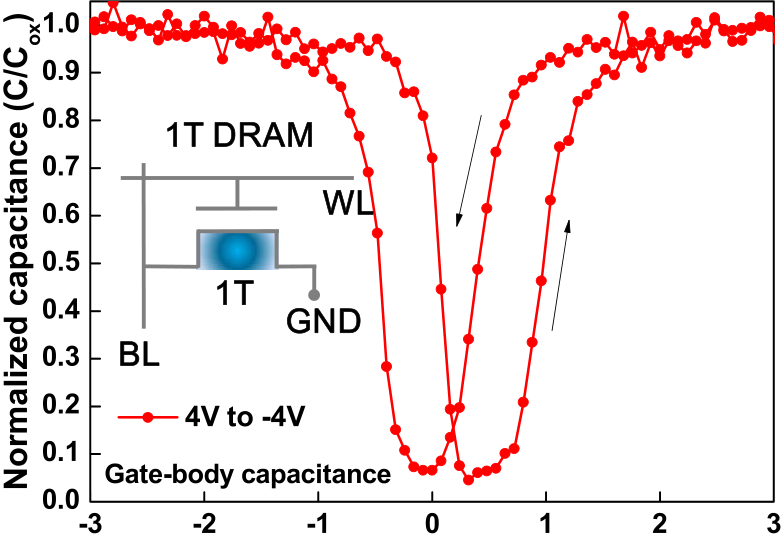
were fabricated on standard n-type Si substrates. A thin 3-nm The self-aligned, gate-first TaN/ZrHfO/SiO2 p−MOSFETs

SiO2 was grown on n-type Si substrate. Then ∼30-nm high-*κ* ZrHfO was deposited by physical vapor deposition (PVD), and followed by 400 °C post-deposition annealing. A Zr/Hf ratio of ∼1 was used to reach the largest polarization and hystere-sis [10]. The TaN metal-gate was then deposited by PVD and patterned. The self-aligned B+ions were then implanted and activated by rapid thermal annealing (RTA) at 950 °C. After opening the contact window at source-drain region, the contact was formed by Al metal deposition, patterning, and annealing at 350 °C. The fabricated p-MOSFETs have a gate length and width of 10-*μ*m and 100-*μ*m, respectively. Therefore, this p-MOSFET has full process compatibility with Hf-based high-*κ* CMOS. The material properties of high-*κ* ZrHfO gate dielectric were examined by grazing incidence x-ray diffraction diffractogram (GI-XRD). The fabricated devices were characterized by capacitance-voltage (*C*-*V)*, current-voltage (*I*-*V )*, and pulsed switching endurance measurements.

III. RESULTS AND DISCUSSION

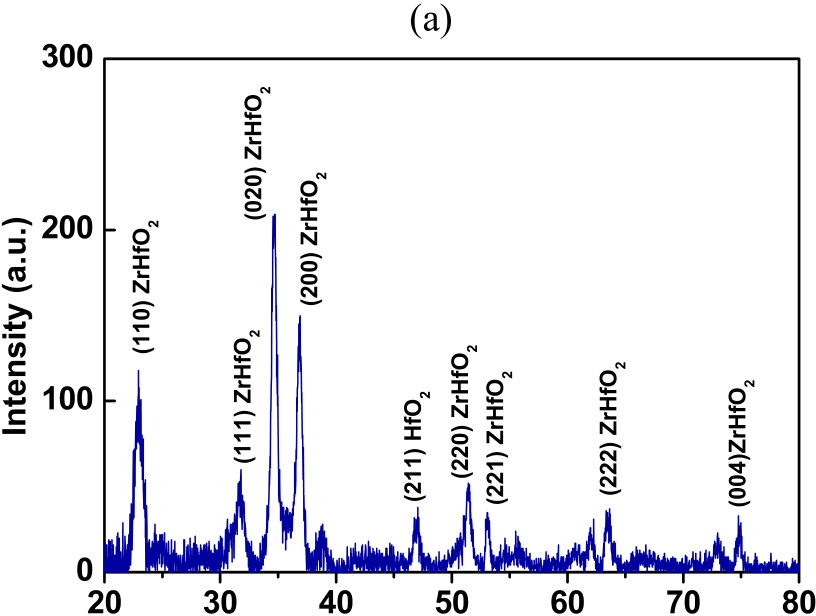
Fig. 1(a) shows the measured *C*-*V* characteristics of the high-*κ* ZrHfO p-MOSFET, in which the schematic 1T FeMOS was inserted. Similar to conventional 1T1C DRAM, the word

0741-3106 © 2013 IEEE



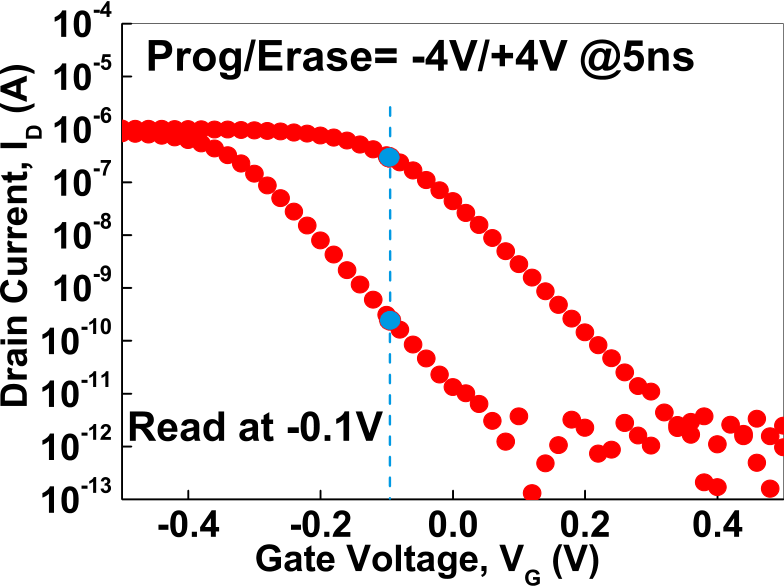
CHENG AND CHIN: LOW-LEAKAGE-CURRENT DRAM-LIKE MEMORY 139



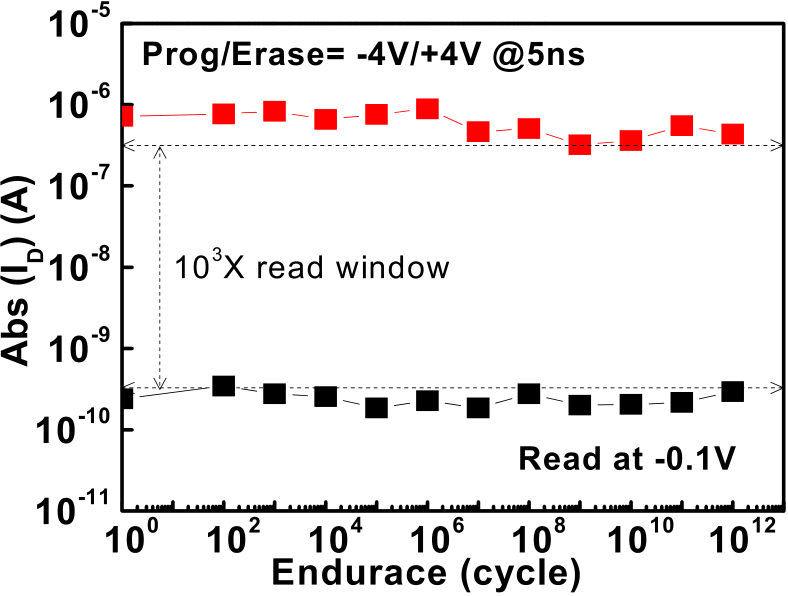












|  |  |  |
| --- | --- | --- |
| Fig. 1. | (a) Measured *C*-*V* characteristics and (b) GI-XRD diffractograms of |  |

high-*κ* ZrHfO *p*-MOSFET. The inserted figure in Fig. 1(a) is the schematic plot of 1T FeMOS.

Fig. 2. (a) *ID*-*VG* after write at −4V/+4V 5 ns P/E pulses and (b) endurance characteristics of ferroelectric ZrHfO *p*-MOSFET.

and bit lines are connected to respective gate and drain to

write/read the stored data. The ferroelectric hysteresis loop and flat band voltage shift were discovered at a 4 V to −4 V sweep. The ferroelectricity is related to the crystalline structure of the ZrHfO gate dielectric observed using GI-XRD diffractograms, as shown in Fig. 1(b), in which various crystalline phases were shown. It is crucial to notice that the ferroelectric gate dielectric thickness in 1T FeMOS was thinner for ZrHfO than for PZT, SBT and BLT [8]. Such a thin thickness is necessary to integrate ferroelectric gate dielectric into a highly scaled deep 1× nm MOSFET, in addition to the Hf-based dielectric compatibility with high-*κ* CMOS [11]–[14].

The FeMOS [7]–[8], in which the ferroelectric material was incorporated into the gate dielectric of the MOSFET, was previously used to perform nonvolatile memory func-tions. However, the FeMOS was subjected to read disturbance and degraded data retention caused by the depolarization effect [16]. To address the read disturbance problem, a novel read scheme was used here to measure the current at a small

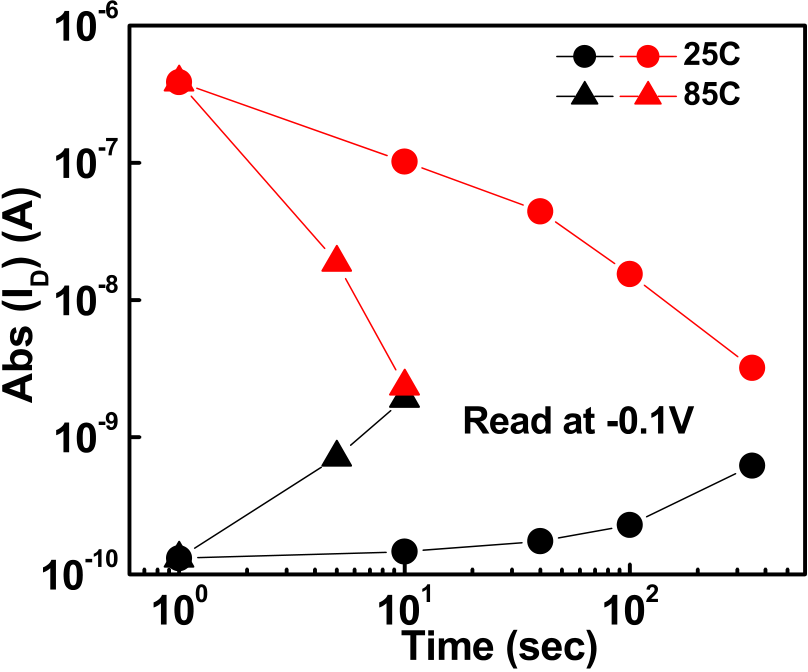
changes by using conventional methods at a high voltage. Such *VG* = −0.1 V, which is different from measuring the *VT*

a low voltage reading has been used in resistive RAM (RRAM) [17]–[19] that can lower the read disturbance effectively in this FeMOS. Fig. 2(a) shows the measured *ID*-*VG* characteristics of the ferroelectric ZrHfO p−MOSFETs, after being written at 5 ns −4 V/+4 V program/erase (P/E) and read at a low *VG* = −0.1 V.

The endurance characteristics are plotted in Fig. 2(b). Stable on-state current (Ion*)* and off-state current (Ioff*)* were maintained for up to 1012P/E cycles, and 5 ns P/E was the fastest pulse time in our system. A considerably large Ion/Ioff read window of 1000 times and a considerably low DC off-state leakage current of 3 × 10−12A/*μ*m were measured, which are critical for energy saving. Although this device has substantially improved DC leakage power, the AC switching power (*CV*2*f/2*) [20] was 1.1 times higher than that of the 32-nm 1T1C DRAM listed in the *ITRS* [1], assuming that was operated at the same frequency ( *f )*. Here *C* is the gate capacitor and/or MIM capacitor; *V* is the drain voltage and/or MIM capacitor voltage. Further reducing the device voltage is necessary for reducing the AC power. Considerably longer endurance is expected at a faster P/E speed with less stress to gate dielectric, because a sub-100 ps polarization switching time was reported in a ferroelectric capacitor.

The retention characteristics of Ion and Ioff are shown in Fig. 3. Although the Ion and Ioff degraded over time because of the depolarization effect, three orders of magnitude Ion/Ioff read windows were still achieved after 10 s of retention at 25 °C. It is important to notice that the endurance and retention performances of this 1T FeMOS are already comparable with or superior to another type of 1T DRAM [21]. Further endurance to 1016cycles using faster pulse generator equip-ment is necessary to explore the full potential for 1T1C DRAM

140 IEEE ELECTRON DEVICE LETTERS, VOL. 35, NO. 1, JANUARY 2014



[4] C. Y. Tsai, K. C. Chiang, S. H. Lin, *et al.*, “Improved capacitance density and reliability of high-*κ* Ni/ZrO2/TiN MIM capacitors using laser annealing technique,” *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 749–752, Jul. 2010.

[5] S. H. Lin, K. C. Chiang, F. S. Yeh, *et al.*, “Improved stress reli-ability of analog metal–insulator–metal capacitors using TiO2/ZrO2 dielectrics,” *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1287–1289, Dec. 2009.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| [6] I. | Hur | and | K. | Lin, | “A | comprehensive | approach | to | DRAM |

power management,” in *Proc. IEEE Intl. Symp. HPCA*, Jun. 2008, pp. 305–316.

[7] Y. Arimoto and H. Ishiwara, “Current status of ferroelectric random- access memory,” *MRS Bull.*, vol. 29, no. 11, pp. 823–828, Nov. 2004. [8] M. Y. Yang, S. B. Chen, A. Chin, *et al.*, “One-transistor PZT/Al2O3, SBT/Al2O3, and BLT/Al2O3 stacked gate memory,” in *Proc. IEDM*, 2001, pp. 795–798.

[9] Z. Wen, C. Li, D. Wu, *et al.*, “Ferroelectric-field-effect-enhanced electroresistance in metal/ferroelectric/semiconductor tunnel junctions,”*Nature Mater.*, vol. 12, pp. 617–621, May 2013.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Fig. 3. | Retention characteristics | of the ferroelectric high-*κ* | ZrHfO | [10] J. Muller, T. S. Boscke, U. Schroder, *et al.*, “Ferroelectricity in simple |
| binary ZrO2 and HfO2,” *Nano Lett.*, vol. 12, pp. 4318–4323, Jul. 2012. [11] K. Mistry, *et al.*, “A 45 nm logic technology with high-k+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm |
| *p*-MOSFET. |

replacement. Further retention improvement may be expected using a thinner SiO2 [22] or high-*κ* interfacial layer [8], for which more than ten years retention was reported [22]. This new DRAM offers a considerably low DC off-state leakage of 3 × 10−12A/*μ*m, a simple capacitor-less 1T process, and a potentially sub-ns switching speed, all of which are impossible for existing 1T1C DRAM devices.

IV. CONCLUSION

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| This | device | offers | superior | DRAM | functions | with |

considerably low DC off-state leakage, a much simpler capacitor-less 1T structure, and a potentially faster speed, all of which far exceed those of existing DRAM devices. These excellent device characteristics were achieved using a ferroelectric high-*κ* ZrHfO gate dielectric in a p-MOSFET that is fully compatible with the existing high-*κ* MOSFET process used in current ICs.

REFERENCES

[1] (2011). *International Technology Roadmap for Semiconductors (ITRS)*  [Online]. Available: http://www.itrs.net/   
[2] K. C. Chiang, C. C. Huang, G. L. Chen, *et al.*, “High performance SrTiO3 metal-insulator-metal capacitors for analog applications,” *IEEE*  *Trans. Electron Device*, vol. 53, no. 9, pp. 2312–2319, Sep. 2006.

[3] K. C. Chiang, C. H. Cheng, K. Y. Jhou, *et al.*, “Use of a high work-function Ni electrode to improved the stress reliability of analog SrTiO3 metal–insulator–metal capacitors,” *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 694–696, Aug. 2007.

dry patterning, and 100% Pb-free packaging,” in *Proc. IEEE IEDM*, Dec. 2007, pp. 247–250.

[12] M. Chudzik, *et al.*, “High-performance high-*κ*/metal gates for 45 nm CMOS and beyond with gate-first processing,” in *Proc. Symp. VLSI Technol.*, Jun. 2007, pp. 194–195.

[13] D. A. Buchanan, *et al.*, “80 nm polysilicon gated n-FETs with ultra-thin Al2O3 gate dielectric for ULSI applications,” in *IEDM Tech. Dig.*, 2002, pp. 223–226.

[14] A. Chin, Y. H. Wu, S. B. Chen, *et al.*, “High quality La2O3 and Al2O3 gate dielectrics with equivalent oxide thickness 5–10 Å,” in *Proc. Symp. VLSI Technol.*, 2000, pp. 16–17.

[15] J.-P. Han and T. P. Ma, “Ferroelectric-gate transistor as a capacitor-less DRAM cell,” *Integr. Ferroelect.*, vol. 27, nos. 1–4, pp. 1053–1062, 1999. [16] T. P. Ma and J.-P. Han, “Why is nonvolatile ferroelectric memory field-effect transistor still elusive?” *IEEE Electron Device Lett.*, vol. 23, no. 7, pp. 386–388, Jul. 2002.

[17] C. H. Cheng, A. Chin, and F. S. Yeh, “High performance ultra-low energy RRAM with good retention and endurance,” in *Proc. IEEE IEDM*, Dec. 2010, pp. 448–451.

[18] C. H. Cheng, F. S. Yeh, and A. Chin, “Low-power high-performance non-volatile memory on a flexible substrate with excellent endurance,”*Adv. Mater.*, vol. 23, no. 7, pp. 902–905, Feb. 2011.

[19] C. H. Cheng, P. C. Chen, Y. H. Wu, *et al.*, “Long endurance nano-crystal TiO2 resistive memory using TaON buffer layer,” *IEEE Electron Device Lett.*, vol. 32, no. 12, pp. 1749–1751, Dec. 2011.

[20] D. S. Yu, A. Chin, C. C. Laio, *et al.*, “3D GOI CMOSFETs with novel IrO2(Hf) dual gates and high-*κ* dielectric on 1P6M-0.18 *μ*m-CMOS,”in *Proc. IEEE IEDM*, Dec. 2004, pp. 181–184.

[21] N. Collaert, M. Aoulaiche, B. De Wachter, *et al.*, “A low-voltage biasing scheme for aggressively scaled bulk FinFET 1T-DRAM featuring 10s retention at 85 °C,” in *Proc. Symp. VLSI Technol.*, Jun. 2010, pp. 161–162.

[22] J. Müller, T. S. Böscke, U. Schröder, *et al.*, “Nanosecond polarization switching and long retention in a novel MFIS-FET based on ferroelectric HfO2,” *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 185–187, Feb. 2012.