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**High *V*th Enhancement Mode GaN Power Devices with High *I*D,max**   
 **Using Hybrid Ferroelectric Charge Trap Gate Stack**   
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**Abstract**  GaN HEMT structure after 400 oC anneal for 30 seconds. The

In this work, we demonstrate a new concept for realizing high threshold voltage (*V*th) E-mode GaN power devices with high maximum drain current (*I*D,max). A gate stack ferroelectric blocking film with charge trap layer, achieved a large positive shift of *V*th. The E-mode GaN MIS-HEMTs with high *V*th of 6 V shows *I*D,max 720 mA/mm. The breakdown voltage is above

intensity of the three peaks attributed to orthorhombic phase HfZrO2 reveals that amorphous HfZrO2 film transformed to polycrystalline orthorhombic phase structure. The P-E hysteresis curves of the metal-insulator-metal capacitor are shown in Fig. 6. Thehigh polarization value of ~30 μC/cm2 was observed, indicating that the amorphous HfZrO2 film had

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| 1100 V. | **Introduction** | transformed to orthorhombic phase after annealing, while the |
| HfO2 sample showed very low polarization. These results |

Gallium Nitride (GaN) HEMT is a promising device for future high power switching device applications. However, due to the fail-safe and fault turn-on issues of high power switching devices, the normally-off GaN HEMTs with high *V*th are needed. However, several techniques such as the gate recess result in the degradation in *I*D,max and thus, the *V*th of the E-mode GaN HEMTs are not high enough to avoid fault turn-on [1, 2]. In this work, a new concept to solve the problem, by the combination of ferroelectric and charge trapped layers [3]is

correspond to the published data as shown in Fig. 7.

The comparison of the device with different blocking oxide is shown in Fig. 8. A higher *V*th was observed for the device with HfZrO2 blocking oxide, indicating a higher density of electrons was stored in the charge trapping layer (CTL). The basic *I-V* characteristics are shown in Figs. 9-12. An E-mode GaN MIS-HEMT operation with a *I*D,max 720 mA/mm, a *g*m,max of 142 mS/mm, a *I*ON/*I*OFF ratio of 3 × 109, and a *V*th of 6 V was achieved. A breakdown voltage of 1138 V at a drain leakage

demonstrated. current of 10 μA/mm was confirmed. Fig. 13 shows the Δ*V*th

**Device Fabrication**   
 The AlGaN/GaN HEMT heterostructure was grown by MOCVD on Si substrate. The ferroelectric HfZrO2 (blocking layer) and HfO2(charge trap layer) films were deposited by ALD as shown in the process flow (Fig. 1). Non ferroelectric samples replacing HfZrO2 by HfO2 or Al2O3 were also fabricated as reference. The blocking oxides (HfZrO2, HfO2, Al2O3) were deposited with the same EOT. The schematic cross section of the device is shown in Fig. 2. The gate-to-drain spacing *L*GD, gate-to-source spacing *L*GS, and gate length *L*G were 15-μm, 3-μm, and 2-μm, respectively.

**Results and Discussion**   
 Fig. 3 illustrates the mechanism of obtaining high *V*th. After the fabrication (Fig. 3(a)), high voltage (16 V) is applied to the gate electrode as the initialization process (Fig. 3(b)). The initialization less than 1 ms, causes strong polarization in HfZrO2 film and electron trapping in HfO2 layer. After the initialization, the gate voltage (*V*g) can be changed to any used voltage, but certain amount of polarization remains because of ferroelectricity of HfZrO2, and trapped electrons remain in the HfO2 layer (Fig. 3(c)). In the case of non-ferroelectric blocked layer (HfO2), electrons are trapped into the trap layer (HfO2), but the amount of the trapped electron is smaller because the non-polarization (Fig. 3(d) and (e)). The larger electron concentration in the trapped layer and remaining polarization in the blocked layer make *V*th higher in HfZrO2 case.

Fig. 4 shows the HRTEM image of the gate dielectric stack. The polycrystalline nature of the HfZrO2 film was confirmed by the fast Fourier transformation (FFT) image (Fig. 4(b)). Fig. 5 shows the GIXRD spectrum of HfZrO2 film deposited on

vs. time with gate stress. A Δ*V*th ~500 mV with *V*DS = 0 V and a Δ*V*th ~300 mV with *V*DS = 10 V were observed after 10,000s stress. The device with HfO2 is burned out earlier in first condition. It might be due to the severe trap assisted tunneling current through the gate.

As shown in Fig. 14, the dynamic *R*ON increased to 1.66 times at the quiescent bias of 500 V. The low current collapse of the device is contributed to the effective passivation with high quality Si3N4/AlGaN interface using nitrogen passivation prior to Si3N4 deposition. Figs. 15 and 16 show the *V*th and *I*D,max with various recess depth for the device with HfZrO2. The recess of AlGaN layer as shown in Fig. 2, is an effective method to increase *V*th. This was confirmed by the experiment shown in Fig. 15. However, the drawback of the recess is the severe degradation in *I*D,max as shown in Fig. 16. In the case of HfZrO2 block layer, the recess depth to obtain the certain *V*th is smaller than that of HfO2. This is the reason why the HfZrO2 blocking layer HEMT shows high *I*D,max than that of HfO2. The benchmark of normally-OFF GaN HEMTs is shown in Fig. 17. The E-mode GaN MIS-HEMTs using ferroelectric gate stack exhibit superior performance (high *V*th and *I*D,max), compared to the other reported E-mode GaN-based devices.

**Conclusion**   
 A new concept to obtain both high *V*th and high *I*D,max by indicating gate stack with ferroelectric and charge trapped layers has been experimentally verified. The results showed the record high *I*D,max of 720 mA/mm with a high *V*th of 6 V. The concept will be a promising candidate for next generation GaN HEMT power device after the device and process optimization for the long term reliability.

**References**   
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| Fig. 1. Process flow of the E-mode GaN MIS-HEMT. |  | Initialization *V*GS = 16 V |
| Fig. 2. The schematic cross section of the GaN MIS-HEMT. | After Initialization (*V*GS = 0 V case) |
| Fig. 3. Schematic band diagram of the polarization gate dielectric stack, illustrating the mechanism of charge storage | |

using high polarity and low polarity materials when *V*GS > 0 V and *V*GS = 0 V.

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|  | | | | | | |  | | | Fig. 6. P-E field hysteresis curves of the metal-insulator-metal capacitor. | | | Fig. 7. Polarization in the HfO2−ZrO2 solid solution with increasing ZrO2 content [6]. | |
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| Fig. 4. (a) HRTEM image of the | | | | | | |
| gate dielectric stack. (b) FFT | | | | | | | Fig. 5. Grazing incidence X-ray | | |
| diffraction spectrum of HfZrO2 | | |
| image of the HfZrO2 film. | | | | | | |
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| Fig. 10. Transfer characteristics in linear scale. The *V*th is extracted to be 6 V from | | | | Fig. 11. OFF-state leakage and breakdown characteristics. |
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| Fig. 9. *I*D-*V*DS characteristics with *V*GS | | |
| Fig. 8. Transfer characteristics of the | | | | | | |
| from 4 to 14 V. | | |
| devices. | | | | | | |
| linear extrapolation. | | | | |
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| Fig. 12. Transfer characteristics in log scale for the devices with HfZrO2 and HfO2 Fig. 13. Changes of *V*th with gate bias stress and gate pulse drain stress. | | | | | | | | | | | | | | |
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| Fig. | 14. | High | | voltage | | switching | | Fig. 15. *V*th versus gate recess depth. | | | Fig. 16. *I*D,max versus gate recess depth. | |
| Fig. 17. Comparison of the performance of | |
| characteristics | | | with | | fast | switching | |
| the E-mode GaN HEMTs. | |
| module. The quiescent drain biases were | | | | | | | |

from 0 V to 500 V.

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