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Integration of Hafnium Oxide on Epitaxial SiGe

for p-type Ferroelectric FET Application

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***Abstract— Increasing demands for new computer archi-tectures may require embedded non-volatile memories as for example in-memory computing. Ferroelectric field-effect transistors (FeFETs) add further advantages besides their outstanding properties due to the availability of both n-type and p-type transistors. The latter favor a different channel materials, like SiGe, due to the low hole mobility in silicon. In this article, we demonstrate the integrationof ferroelectric hafnium oxide on SiGe as well as working p-type FeFETs, possessing a large memory window of about 1.1 V and low variability. Such architectures were co-integrated into a standard high-k metal gate (HKMG) CMOS platform. Fur-thermore, we report on the impact of annealing temperature on the interface and ferroelectric layer, which appears to be universal for SiGe and Si substrates. Here, a growth of the interface layer during annealing at higher temperatures was observed as well as a reduction of the wake-up effect for the ferroelectric layer.***

***Index Terms— Anti-ferroelectrics, ferroelectrics, ferro-electric field-effect transistor (FeFET), hafnium oxide, sili-con germanium.***

I. INTRODUCTION   
**T** ogy, has resulted in an increased interest in embedded HE increasing gap between logic and memory technol-

non-volatile memory (eNVM) solutions, especially with the

increasing interest in new computer architectures like near-/in-

memory computing, reconfigurable logic, and other non-von-

Neumann architectures [1]. Hafnium oxide based ferroelectric

field-effect transistors (FeFETs) have been demonstrated as a

promising solution for the 28 nm [2] and 22 nm [3] technology

node.

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Due to its compatibility to complementary metal-oxide-semiconductor (CMOS) processes, its high coercive field and stable ferroelectricity in ultra-thin films, ferroelectric hafnium offers many advantages as compared to standard ferroelectrics such as lead zirconate titanate (PZT) [4]–[6]. The orthorhom-bic phase, which is attributed to the ferroelectricity in HfO2 [7], is meta-stable. Therefore, other phases, like the mono-clinic, tetragonal and cubic phase, might co-exist inside the thin film [8]. Applying doping, stress, thermal treatment, or an increase of the specific surface area, the composition of the film can be influenced to increase the amount of orthorhombic phase [8]–[11].

So far, most research regarding the integration of FeFETs has considered n-type transistors [2], [3], [6], as silicon exhibits a low hole mobility, thus prohibiting an equally good performing p-type FET [12]. On the other hand, p-FeFETs could offer new circuit possibilities, especially for new emerg-ing architectures like near- and in-memory computing [1] as well as reconfigurable logics [13]. In order to achieve good device performance for p-FeFETs, epitaxial silicon germa-nium (SiGe) can be used as the channel material, analogously to p-type FETs in the CMOS process flow.

In this contribution the integration of silicon doped HfO2 (HSO) on an epitaxially grown SiGe layer is investigated and compared to HSO layers grown on silicon. Here, strong influ-ences of the annealing temperature on the interface layer thick-ness are found for both substrates. Additionally, changes in the crystallographic orientation and accompanying texture as well as the electrical behavior of the HSO layer were observed. Furthermore, the integration of a p-FeFET in an high-k metal gate (HKMG) CMOS process is demonstrated here.

II. INTEGRATING HAFNIUM OXIDE ONTO SIGE

Boron-doped silicon germanium (B:Si0*.*75Ge0*.*25) layers were grown epitaxially to a thickness of 50 nm on a highly p-doped silicon wafer in a chemical vapour deposition (CVD) process. Afterwards, a 10 nm thick HSO layer was deposited by atomic-layer-deposition using HfCl4 and SiCl4 with a 16:1 cycling ratio as precursors. For both the SiGe and Si substrates, a native oxide layer with a thickness of 1 nm was detected by ellipsometry prior to HfO2 deposition. TiN deposited via physical vapor deposition (PVD) was used as top electrode. The crystallization of the HSO layer was induced by a rapid thermal processing (RTP) spike anneal at different

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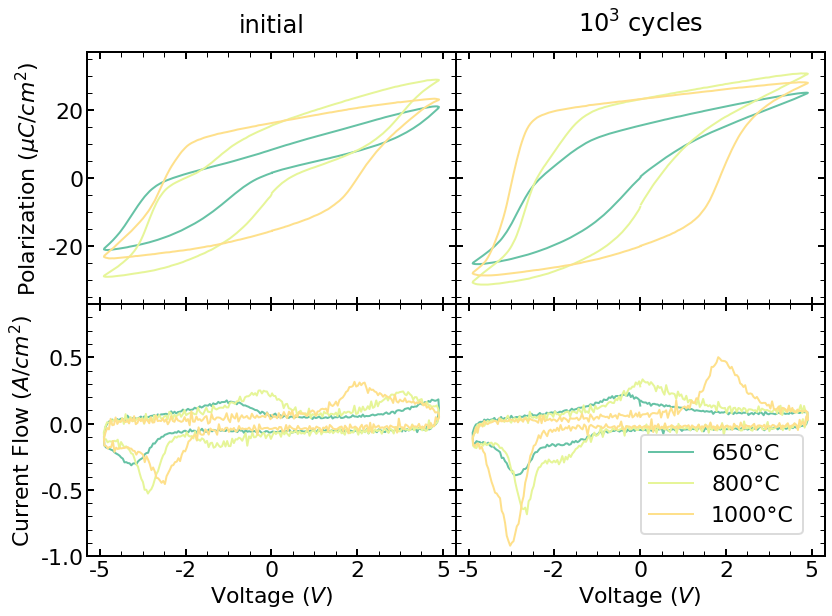


Fig. 1. Polarization-voltage loops as well as the corresponding current-voltage loops for pristine (left) and post-cycled (right) state of the HSO samples grown on SiGe. A strong asymmetric behavior is found for lower annealing temperatures. No pronounced wake-up is observed for the sample annealed at 1000◦.

temperatures. Capacitor structures were formed by sputtering Ti/Pt metal contacts using a shadow mask followed by a SC1 wet etch to remove TiN between individual structures.

Dynamic hysteresis measurements are conducted with a frequency of 1 kHz and 5 V amplitude, same conditions are applied for cycling. The polarization hysteresis of the produced layers (see Figure 1) on SiGe substrates show a high remanent polarization around 20 *µ*C/cm2. The higher voltage required to switch the polarization in these metal-ferroelectric-insulator-semiconductor (MFIS) structures compared to metal-ferroelectric-metal (MFM) samples can be explained by the voltage drop across the insulator layer. Furthermore, strong differences in the polarization-voltage (P-V) loops for different annealing temperatures are apparent. Initial curves of samples annealed at 650◦C and 800◦C show an anti-ferroelectric-like behavior and thus a pronounced wake-up effect, which has been attributed to defect redistribution [14], [15], phase-

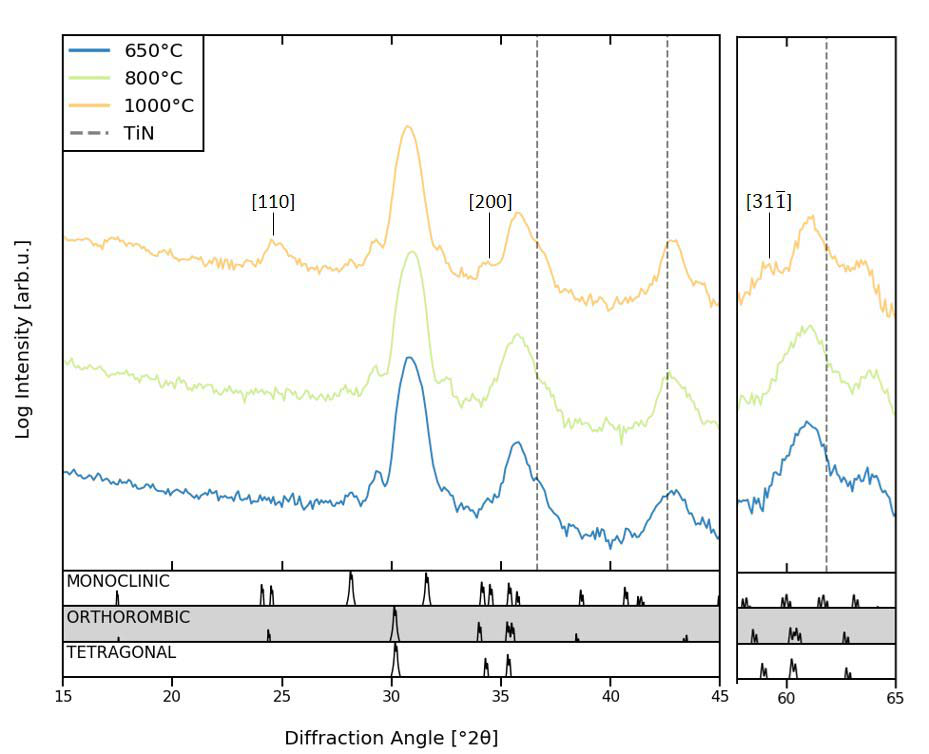


Fig. 2. GIXRD diffraction pattern for HSO layers grown on SiGe substrate. A [110] texture (at 25◦) appears for increased annealing temperature.

of the positive peaks’ coercive field. This corresponds to a destabilization of one certain polarization state. Shifts of the coercive fields in the same direction are due to internal bias fields resulting from band alignment or charged defects as well as depolarization fields, influenced by the capacitance stack [21]. Additionally, this might be superimposed by changes in the coercive field distribution due to textures inside the film. In general, internal bias fields due to band alignment are expected for MFIS stacks. On the contrary, a shift of more than one volt does exceed the expected magnitude, as the difference between all samples is only the annealing temperature. In addition, only a weak internal bias field is observed for the sample annealed at 1000◦(see Figure 1).

To gain further insight into the origin of the deviating behavior of the MFIS stacks, capacitance-voltage (CV) mea-surements were conducted. The appearing hysteresis in the CV curves is a result of the different polarization states. As the

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| transitions [15]–[17], or | ferroelastic switching [18]–[20]. | additional interplay of electrical active defects is currently |

Both samples show strong asymmetry in the switching behav-ior before and after wake-up. On the contrary, annealing at 1000◦C results in a purely ferroelectric and symmetric behavior, revealing only a slight increase in P*r* with cycling.

From grazing incident X-ray diffraction (GIXRD) data, an increase of intensity for the [110] diffraction line of the monoclinic and/or orthorhombic phase for higher anneal-ing temperature is found (see Figure 2). This suggests a preferred in-plane orientation of the [110]-axes. Addition-ally, increased intensity of the [200] and [31¯1] lines are observed. Consequently, an out-of-plane texture of the [001]-axis appears likely. As the texture becomes less dominant with decreasing temperature, more [001]-axes will arrange closer to in-plane directions, enabling ferroelastic switching. Consequently, a much more pronounced wake-up effect is observed.

After wake-up cycling, the samples annealed at lower tem-peratures show a stronger asymmetry of the switching voltages (see Figure 1), originating mainly from a strong reduction

not fully understood, interface defect densities could not be extracted. Nevertheless, for large voltage amplitudes, the hysteresis closes and capacitance values saturate, thus allowing the extraction of the combined oxide capacitance (C*ox*) of the two insulating layers at −5 V. Here, the extracted C*ox* shows a clear trend to lower values with increasing annealing temperature, as shown in Figure 3a. Since the XRD measurements (see Figure 2) shows no apparent differences, a significant change in the relative per-mittivity of this layer, due to amorphous regions and/or higher monoclinic phase, can be excluded. For investigating the SiO2 interface layer, transmission electron microscopy (TEM) measurements were conducted.

As shown in Figure 3b, a strongly increased thickness of the interface layer was found for samples annealed at 1000◦C. This agrees qualitatively with the C-V measurements, as an increase in interface layer thickness will result in a lower C*ox* of the MFIS stack. Quantitatively, on the other hand, the extracted interface layer thickness, with 1.0 nm and 0.3 nm for

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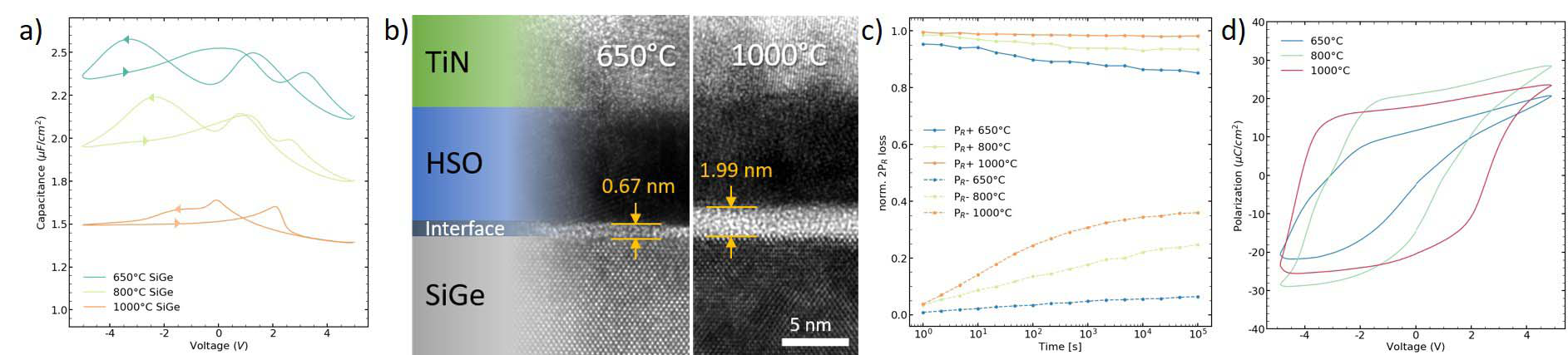


Fig. 3. Capacitance-voltage curves for samples grown on SiGe (a). C-V measurements are dominated by the hysteretic behavior resulting from ferroelectricity, but a overall shift to lower capacitance values can be observed. TEM analysis (b) of cross-sections from samples grown on SiGe show interface growth with higher annealing temperatures. Retention measurements (c) show increased polarization loss with interface thickness. For the P-V loops of samples grown on heavily doped p-type silicon (d) only insignificant differences to HSO on SiGe are observed.

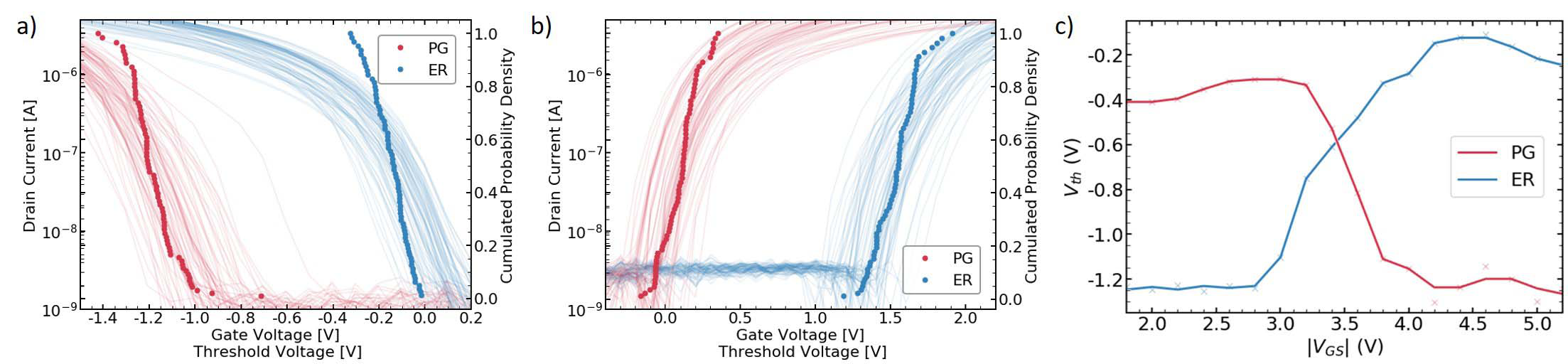


Fig. 4. Switching characteristics (c) of the p-FeFET show clear transitions. Drain voltage was set to 0.1 V for all readouts. Transfer characteristics of a p-type (a) and n-type (b) FeFET with L = 450 nm2, W = 450 nm2for program (red) and erase (blue) state.

1000◦C and 650◦C, respectively, is lower than the thickness measured by TEM, assuming a relative permittivity of 3.9 for SiO2 and 30 for HSO. Consequently, the relative permittivity of the layers may differ due to changes in the composition or crystallographic phase.

Thinner interface layers will result in a lower depolarization field [22], which is contradictory to a stronger destabilization of the negative polarization state for samples annealed at lower temperatures. On the other hand, the relative retention loss is higher for thicker interfaces (see Figure 3c). Remarkably, the measurement shows a shift in the stability of the two states. While thinner interfaces show less retention loss for the negative state, the positive state is more stable in case of thicker interfaces. This highlights that charged defect states in the interface layer or a currently unknown contribution are affecting the stability/behavior of the polarization states. Improved understanding of the C-V hysteresis may help to extract charges and defect densities in the layers.

From Figure 3d which shows a similar behavior of the ferroelectric layer for samples having a Si substrate, it can be further deduced that the aforementioned effects seem to be generally present in CMOS based MFIS stacks.

Like in anti-ferroelectric behavior based devices [23], band engineering allows to superimpose an adapted bias field, thus rendering the I-V loops symmetric. This could enable to build less power consuming non-volatile memory devices due to the decreased switching voltage.

on a SiGe epilayer while the n-FeFETs were structured on silicon on the same wafer. For writing the program and erase state, a square pulse with an amplitude of ±4*.*5 V (±4 V for n-FeFETs) and a pulse duration of 500 ns was applied. For each type a total of 72 devices were measured. The resulting transfer characteristics are displayed in Figure 4a and 4b for p- and n-FeFETs, respectively. The p-FeFET devices could achieve a memory window of 1*.*1 V. This value is quite similar to the n-FeFETs, with a memory window of 1*.*4 V. Additionally, low variability was achieved for both types. Furthermore, by applying pulses with increasing amplitude and erasing/programming each time in between, switching characteristics can be extracted for programming and erasing, respectively (see Figure 4c). Here, switching in the range of about 3*.*5 V is observed for both directions.

IV. CONCLUSION

In conclusion the integration of HfO2 based p-FeFET onto silicon germanium in a CMOS compatible way was demonstrated, opening up new possibilities for circuit design, especially for near-/in-memory computing and reconfigurable logics. Furthermore, structural and electrical characterization showed a strong influence of the annealing temperature on the interface layer as well as the material behavior and crys-tallographic texture of the ferroelectric HfO2 layer. Especially samples annealed at 1000◦C showed an absence of initial anti-ferroelectric behavior.

III. P-FEFET DEVICE PERFORMANCE REFERENCES

The p- and n-FeFETs were integrated in a CMOS-compatible eNVM process [2]. The former were produced

[1] A. Chen, “A review of emerging non-volatile memory (NVM) tech-nologies and applications,” *Solid-State Electron.*, vol. 125, pp. 25–38, Nov. 2016, doi: [10.1016/j.sse.2016.07.006](http://dx.doi.org/10.1016/j.sse.2016.07.006).

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LEDERER et al.: INTEGRATION OF HAFNIUM OXIDE ON EPITAXIAL SiGe FOR p-type FeFET APPLICATION 1765



[2] J. Müller, E. Yurchuk, T. Schlosser, J. Paul, R. Hoffmann, S. Müller, D. Martin, S. Slesazeck, P. Polakowski, J. Sundqvist, M. Czernohorsky, K. Seidel, P. Kucher, R. Boschke, M. Trentzsch, K. Gebauer, U. Schroder, and T. Mikolajick, “Ferroelectricity in HfO2 enables nonvolatile data storage in 28 nm HKMG,” in *Proc. Symp. VLSI Technol.*  *(VLSIT)*, Jun. 2012, pp. 25–26, doi: [10.1109/VLSIT.2012.6242443](http://dx.doi.org/10.1109/VLSIT.2012.6242443).

[3] S. Dunkel, M. Trentzsch, R. Richter, P. Moll, C. Fuchs, O. Gehring, M. Majer, S. Wittek, B. Müller, T. Melde, H. Mulaosmanovic, S. Slesazeck, S. Müller, J. Ocker, M. Noack, D.-A. Lohr, P. Polakowski, J. Müller, T. Mikolajick, J. Hontschel, B. Rice, J. Pellerin, and S. Beyer,“A FeFET based super-low-power ultra-fast embedded NVM technology for 22 nm FDSOI and beyond,” in *IEDM Tech. Dig.*, Dec. 2017, p. 19, doi: [10.1109/IEDM.2017.8268425](http://dx.doi.org/10.1109/IEDM.2017.8268425).

[4] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger,“Ferroelectricity in hafnium oxide thin films,” *Appl. Phys. Lett.*, vol. 99, no. 10, Sep. 2011, Art. no. 102903, doi: [10.1063/1.3634052](http://dx.doi.org/10.1063/1.3634052).

[13] E. T. Breyer, H. Mulaosmanovic, T. Mikolajick, and S. Slesazeck,“Reconfigurable NAND/NOR logic gates in 28 nm HKMG and 22 nm FD-SOI FeFET technology,” in *IEDM Tech. Dig.*, Dec. 2017, p. 28, doi: [10.1109/IEDM.2017.8268471](http://dx.doi.org/10.1109/IEDM.2017.8268471).

[14] D. Zhou, J. Xu, Q. Li, Y. Guan, F. Cao, X. Dong, J. Müller, T. Schenk, and U. Schröder, “Wake-up effects in Si-doped hafnium oxide ferro-electric thin films,” *Appl. Phys. Lett.*, vol. 103, no. 19, Nov. 2013, Art. no. 192904, doi: [10.1063/1.4829064](http://dx.doi.org/10.1063/1.4829064).

[15] M. Peši´c, F. P. G. Fengler, L. Larcher, A. Padovani, T. Schenk, E. D. Grimley, X. Sang, J. M. LeBeau, S. Slesazeck, U. Schroeder, and T. Mikolajick, “Physical mechanisms behind the field-cycling behavior of HfO2 -based ferroelectric capacitor[s,”](http://dx.doi.org/10.1002/adfm.201600590) *Adv. Funct. Mater.*, vol. 26, no. 25, pp. 4601–4612, Jul. 2016, doi: [10.1002/adfm.201600590](http://dx.doi.org/10.1002/adfm.201600590).

[16] S. E. Reyes-Lillo, K. F. Garrity, and K. M. Rabe, “Antiferroelectricity in thin-film ZrO2 from first principles,” *Phys. Rev. B, Condens. Mat-ter*, vol. 90, no. 14, Oct. 2014, Art. no. 140103, doi: 10.1103/Phys-

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| --- | --- | --- | --- | --- | --- | --- |
| [5] J. Müller, T. S. Böscke, U. Schröder, S. Mueller, D. Bräuhaus, | RevB.90.140103. | T. Schenk, | X. Sang, | M. Peši´c, | U. | Schroeder, |
| U. Böttger, L. Frey, and T. Mikolajick, “Ferroelectricity in simple binary | [17] E. D. Grimley, |

ZrO2 [and HfO2](http://dx.doi.org/10.1021/nl302049k),” *Nano Lett.*, vol. 12, no. 8, pp. 4318–4323, Aug. 2012, doi: [10.1021/nl302049k](http://dx.doi.org/10.1021/nl302049k).

[6] T. Ali, P. Polakowski, T. Buttner, T. Kampfe, M. Rudolph, B. Patzold, R. Hoffmann, M. Czernohorsky, K. Kuhnel, P. Steinke, L. M. Eng, and K. Seidel, “Principles and challenges for binary oxide based ferroelectric memory FeFET,” in *Proc. IEEE 11th Int. Memory Workshop (IMW)*, May 2019, pp. 1–4, doi: [10.1109/IMW.2019.8739651](http://dx.doi.org/10.1109/IMW.2019.8739651).

[7] X. Sang, E. D. Grimley, T. Schenk, U. Schroeder, and J. M. LeBeau,“On the structural origins of ferroelectricity in HfO2 thin film[s,”](http://dx.doi.org/10.1063/1.4919135) *Appl.*

*Phys. Lett.*, vol. 106, no. 16, Apr. 2015, Art. no. 162905, doi: [10.1063/ 1.4919135](http://dx.doi.org/10.1063/1.4919135).

[8] R. Materlik, C. Künneth, and A. Kersch, “The origin of ferroelectricity in Hf1−*x*ZrxO2: A computational investigation and a surface energy model,” *J. Appl. Phys.*, vol. 117, no. 13, Apr. 2015, Art. no. 134109, doi: [10.1063/1.4916707](http://dx.doi.org/10.1063/1.4916707).

[9] J. Müller, P. Polakowski, S. Mueller, and T. Mikolajick, “Ferroelectric hafnium oxide based materials and devices: Assessment of current status and future prospects,” *ECS J. Solid State Sci. Technol.*, vol. 4, no. 5, pp. N30–N35, 2015, doi: [10.1149/2.0081505jss](http://dx.doi.org/10.1149/2.0081505jss).

T. Mikolajick, and J. M. LeBeau, “Structural changes underlying field-cycling phenomena in ferroelectric HfO2 thin films,” *Adv. Electron.*

*Mater.*, vol. 2, no. 9, Sep. 2016, Art. no. 1600173, doi: [10.1002/aelm. 201600173](http://dx.doi.org/10.1002/aelm.201600173).

[18] T. Shimizu, T. Mimura, T. Kiguchi, T. Shiraishi, T. Konno, Y. Katsuya, O. Sakata, and H. Funakubo, “Ferroelectricity mediated by ferroelastic domain switching in HfO2-based epitaxial thin films,” *Appl. Phys.*

*Lett.*, vol. 113, no. 21, Nov. 2018, Art. no. 212901, doi: [10.1063/ 1.5055258](http://dx.doi.org/10.1063/1.5055258).

[19] M. Lederer, T. Kämpfe, R. Olivo, D. Lehninger, C. Mart, S. Kirbach, T. Ali, P. Polakowski, L. Roy, and K. Seidel, “Local crystallographic phase detection and texture mapping in ferroelectric Zr doped HfO2 films by transmission-EBSD,” *Appl. Phys. Lett.*, vol. 115, no. 22, Nov. 2019, Art. no. 222902, doi: [10.1063/1.5129318](http://dx.doi.org/10.1063/1.5129318).

[20] M. Lederer, T. Kämpfe, N. Vogel, D. Utess, B. Volkmann, T. Ali, R. Olivo, J. Müller, S. Beyer, M. Trentzsch, K. Seidel, and L. M. Eng,“Structural and electrical comparison of Si and Zr doped hafnium oxide thin films and integrated FeFETs utilizing transmission kikuchi diffrac-tion,” *Nanomaterials*, vol. 10, no. 2, p. 384, Feb. 2020, doi: [10.3390/](http://dx.doi.org/10.3390/nano10020384)

[10] L. Xu, T. Nishimura, S. Shibayama, T. Yajima, S. Migita, and [nano10020384](http://dx.doi.org/10.3390/nano10020384).

A. Toriumi, “Kinetic pathway of the ferroelectric phase formation in doped HfO2 films[,”](http://dx.doi.org/10.1063/1.5003918) *J. Appl. Phys.*, vol. 122, no. 12, Sep. 2017, Art. no. 124104, doi: [10.1063/1.5003918](http://dx.doi.org/10.1063/1.5003918).

[11] E. Yurchuk, J. Müller, S. Knebel, J. Sundqvist, A. P. Graham, T. Melde, U. Schröder, and T. Mikolajick, “Impact of layer thickness on the ferro- electric behaviour of silicon doped hafnium oxide thin films,” *Thin Solid*  *Films*, vol. 533, pp. 88–92, Apr. 2013, doi: [10.1016/j.tsf.2012.11.125](http://dx.doi.org/10.1016/j.tsf.2012.11.125). [12] S. Verdonckt-Vandebroek, E. F. Crabbe, B. S. Meyerson, D. L. Harame, P. J. Restle, J. M. C. Stork, and J. B. Johnson, “SiGe-channel hetero- junction p-MOSFET’s,” *IEEE Trans. Electron Devices*, vol. 41, no. 1, pp. 90–101, Jan. 1994, doi: [10.1109/16.259625](http://dx.doi.org/10.1109/16.259625).

[21] T. Schenk, E. Yurchuk, S. Mueller, U. Schroeder, S. Starschich, U. Böttger, and T. Mikolajick, “About the deformation of ferroelectric hystereses,” *Appl. Phys. Rev.*, vol. 1, no. 4, Dec. 2014, Art. no. 041103, doi: [10.1063/1.4902396](http://dx.doi.org/10.1063/1.4902396).

[22] T. P. Ma and J.-P. Han, “Why is nonvolatile ferroelectric memory field-effect transistor still elusive?” *IEEE Electron Device Lett.*, vol. 23, no. 7, pp. 386–388, Jul. 2002, doi: [10.1109/LED.2002.1015207](http://dx.doi.org/10.1109/LED.2002.1015207).

[23] M. Peši´c, M. Hoffmann, C. Richter, T. Mikolajick, and U. Schroeder,“Nonvolatile random access memory and energy storage based on antiferroelectric like hysteresis in ZrO2,” *Adv. Funct. Mater.*, vol. 26, no. 41, pp. 7486–7494, Nov. 2016, doi: [10.1002/adfm.201603182](http://dx.doi.org/10.1002/adfm.201603182).

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