**Hybrid 1T e-DRAM and e-NVM Realized in One 10 nm node Ferro FinFET**

**device with Charge Trapping and Domain Switching Effects**

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***Abstract****� For the first time, we experimentally demonstrated a 10nm node HfZrO based FE-FinFET device with both Charge Trapping and Domain Switching memory effect.* Extreme high endurance (>1012), high operation speed (<20ns), good data retention (104@85C), low operation voltage (<3V) were identified in charge trapping mode, which is quite promising for e-DRAM application. As the device working in domain switching mode, even more robust retention (>10 years) and read disturbance immunity were achieved, showing great potential for e-NVM application.

**INTRODUCTION**

Due to recent trends of increasing system core-count and memory bandwidth bottleneck, large size on-chip caches are pursued to effectively reduce the performance gap between processor and main memory. Suffering from the large cell size and increasing leakage of SRAM, frustrations with SRAM for majority real estate occupation and unsatisfying scaling performance were encountered by chip designer. To overcome the limitations of SRAM, alternate memory technologies, such as eDRAM and STT-RAM were explored as a substitution of SRAM(**Fig.1**).[1]However, eDRAM suffers from poor data retention and scaling limitation below 1z node. Other alternates with better scaling potential and non-volatility are needed. On the other hand, e-NVM in SOC chip is also suffering from the limitation of e-FLASH integration on the advanced technology node. BEOL based memories, such as STT-RAM and RRAM were proposed as the possible solutions at 40 nm and 22 nm node(**Fig.2**).[2, 3]However, for the e-NVM solution at 10 nm node or beyond, there still is no candidate identified.

In this work, we proposed a Fe-FinFET memory device with HfZrO (HZO) ferro layer as the gate dielectric for both 1T e-DRAM and e-NVM applications. The coexistence of

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| charge | trapping | (CT) | and | domain | switching | (DS) |

phenomenon was observed. As the operation voltage <3V, charge trapping effect was dominant, and as the operation voltage >5V, domain switching of HZO layer occurred. Both of the CT and DS behavior exhibit high operation speed (<20ns). High endurance of more than 1012and good data retention of 104s were achieved in CT mode, which is quite promising for e-DRAM application. The DS mode exhibits even more robust retention (>10 years) and read disturbance immunity, showing good possibility for e-NVM applications.

**EXPERIMENTAL**

The process flow of this Fe-FinFET was shown in **Fig.3**. The Spacer-Image Transfer (SIT) method was implemented to form ultra-small fin structure. The STI oxide provides the basic body isolation between adjacent fins. After the junction isolated process, Punch through Stop Layer (PTSL) implantation in the PTSL flow, there is a low thermal anneal, followed by dummy gate formation and SD formation. The PTSL implantation was skipped in the self-aligned punch through stop pocket (PTSP) process flow. In following steps, the dummy gate, spacers, source/drain doping process, activation anneal and all-last high-k/metal gate process were implemented by regular bulk FinFETs integration process After the self-aligned PTSP IMP, the 1050C spike anneal is conducted to active SD and channel dopants at the same time. The Hf0.5Zr0.5O2 layer was deposited by ALD. After the TiN/TaN/TiN/W metal gates deposition, rapid annealing

process at 600� for 30s to crystallize HZO. The structure schematic, TEM image and the spectrum of EDX mapping over the cross-section of the device are shown in **Fig.4**. Fin structure with 9nm width/20 nm length and Si/IL/HZO (9.37nm)/TiN/TaN/TiN/W gate stack was confirmed.

**RESULTS AND DISCUSSION**

***Coexistence of Charge Trapping and Domain Switching***

To confirm the ferroelectric property of Si/IL/HZO/TiN structure, planar device with 5nm TiN top electron was characterized. **Fig.5** shows the TEM image of planar Si/IL(0.8nm)/HZO(10.7nm)/TiN/W stack with 600o�/30s annealing. Interfacial layer (SiO2) between the HZO layer and Si substrate can be observed.**Fig.6** shows the XRD Spectra of HZO film before and after 30s annealing at 400, 500 and 600oC, respectively. The peak of the orthorhombic phase increased as the annealing temperature increases. Considering that various factors may contribute to the polarization which could be �������������������������������������������������������-�����������������������. The remanent hysteresis could be obtained by PUND test, as described in **Fig.7. Fig.8** exhibits the P-V characteristics of Si/IL/HZO/TiN structure after 30s annealing at 400, 500 and 600oC and the corresponding changes of2Pr as a function of TiN thickness. Higher annealing temperature will result in stronger true-remanent polarization. The result shows there is almost no influence of thin 5nm TiN TE on the ferroelectricity compared with the thicker TiN TE. On the contrary, a slight

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enhancement was observed. The coercive voltage of the Si/IL/HZO/TiN structure is larger than the control sample withTiN/HZO/TiN structure[3], which was resulted from the voltage drop on SiO2 IL (**Fig.8**).The trap in the HZO layer could be analyzed by Random Telegraph Noise (RTN) which is generated by electron capture/emission in the trap site.**Fig. 9a and b** show the RTN signal of IG measured under 2.5V with SR=105Hz. Five peaks RTN signal was observed (**Fig. 9c**).The PSD result shows that multi-traps existed in the HZO layer (**Fig.9d**).

As shown�in�**Fig. 10,** the charge trapping induces VT shift, which is opposite��o the VT shift caused by the ferroelectric domain switching in�the same polarity of the gate voltage. For example, holes trapped in the gate dielectric at positive gate voltage result in a positive shift of the VT. On the other hand, positive ferroelectric polarization induced by the same positive gate voltage leads to a negative VT shift. Both of charge trapping and ferroelectric switching was found in the same FinFET device with a Si/IL/HZO/TiN/TaN/TiN/W gate stack. As shown in **Fig. 11**, after a -5V voltage sweep, the polarization was poled up and holes were trapped in the HZO layer. The VT was shift to -1.5V due to the domination of charge tapping effect. After 1 V voltage sweep, the VT begins to move to the positive side. As the sweep voltage increased to around 3V, the charge trap memory window reached to the peak value. When higher voltage was applied on the device, ferroelectric switching behavior began to dominate the performance (negative shift of VT). The voltage drop on SiO2 IL results in the increase of ferroelectric switching voltage. The FE-FET memory window is larger than the CTM. These special characteristics of charge trapping and domain switching coexistence can be used for both 1T e-DRAM and e-NVM applications.

***Charge trap behavior for 1T-DRAM application***

The down-scaling in a conventional combination of 1T1C DRAM is becoming increasingly difficult at 1z node, in particular due to the high demand for non-scalable cell capacitance.1T-DRAM has been proposed to solve this issues. For the 1T-DRAM application, some critical properties need to be solved, such as high speed, high endurance and low power. **Fig. 12**represents consecutive DC cycles of the device for 100 cycles with a sweeping gate voltage of -3V to 2V and drain voltage of 100mV. ��������VT window, low off state current ~10-11 and large Ion/Ioff ratio of >104 were achieved. The cumulative distribution of VT of ���� ������� ���� �������(**Fig.13**) shows high cycle to cycle uniformity of this device. **Fig. 14a** and **14b** show the dependence of switching speed on pulse amplitudes for program and erase operations, respectively. Higher programming voltage corresponds to

options[4-6], The Fe-FinFET in CTM mode exhibit excellent switching speed (20ns), lower operation voltage (<3V), lower read current (<10 �A) and excellent endurance (**Fig.17**).

***Domain switching effect of FE-FET for embedded NVM***

As the conventional e-FLASH encountering severe limitations on integration into the high-k/metal gate (HKMG) process and FinFET process, the upcoming IoT era shows huge demands on the new types embedded non-volatile memories (eNVM) with low cost, low power and good compatibility with advanced logic process. The Fe-FinFET

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problems.**Fig.18** shows Fe-FET behavior of the device by pulse operation with pulse height >6V. Positive gate voltage leads to a negative VT shift, while negative gate voltage leads to a positive VT shift. After 30 pulse cycles, a 1.2V memory window was confirmed and this device shows high uniformity by AC cycling (**Fig.19**). Under successive voltage pulses with 6V/20ns and -6V/20ns, 100k endurance was achieved (**Fig.20**). The device could retain over 10 years at 25C, which is sufficient to meet the requirement of eNVM. **Table 1** summarizes the specifications of different candidates of eNVM for low power SOC applications at 14 nm technology node and beyond.

**CONCLUSION**

In summary, the coexistence of charge trapping and domain switching phenomenon in one FE-FinFET device was demonstrated for the first time. Excellent switching speed (20ns), lower operation voltage (<3V), lower read current (<10 � A) and high endurance (>1012), the CT mode show great potential to be used as 1T e-DRAM. The domain switching behavior of this device exhibits high uniformity, good retention and low power consumption, which is quite suitable for eNVM application.

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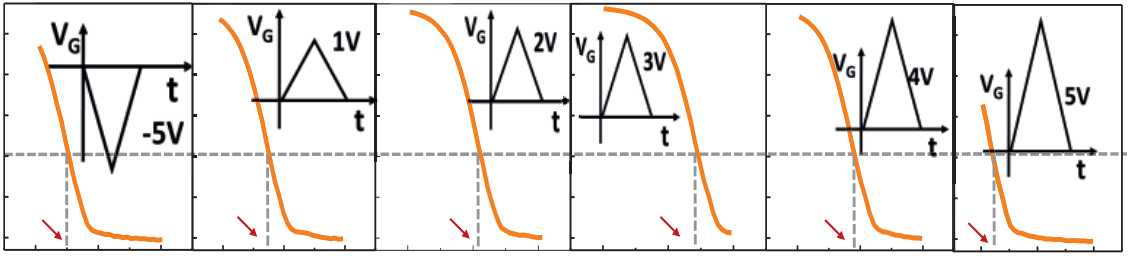
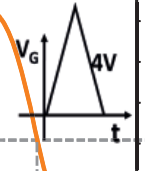
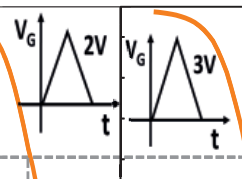
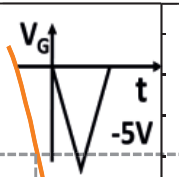
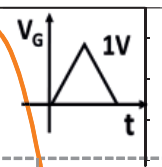
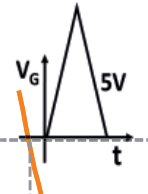
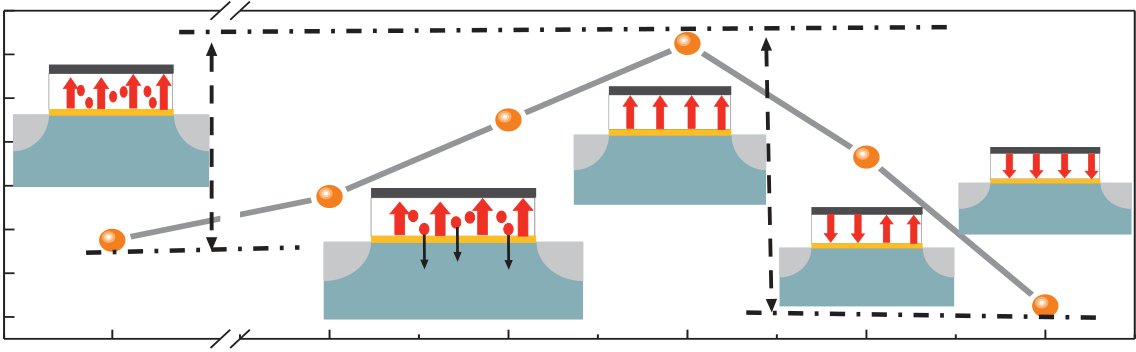
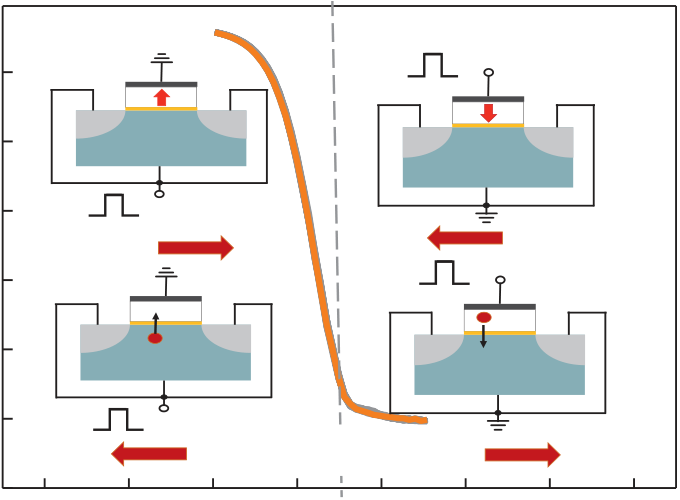
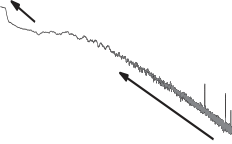
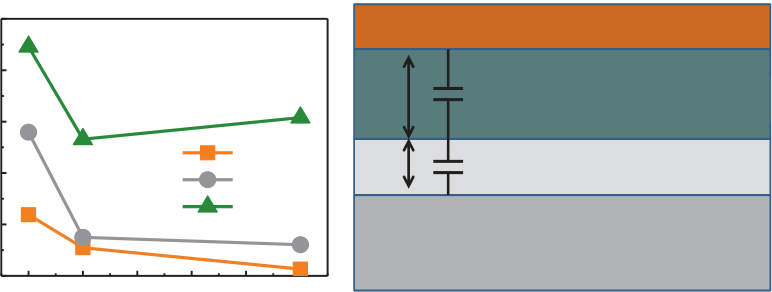
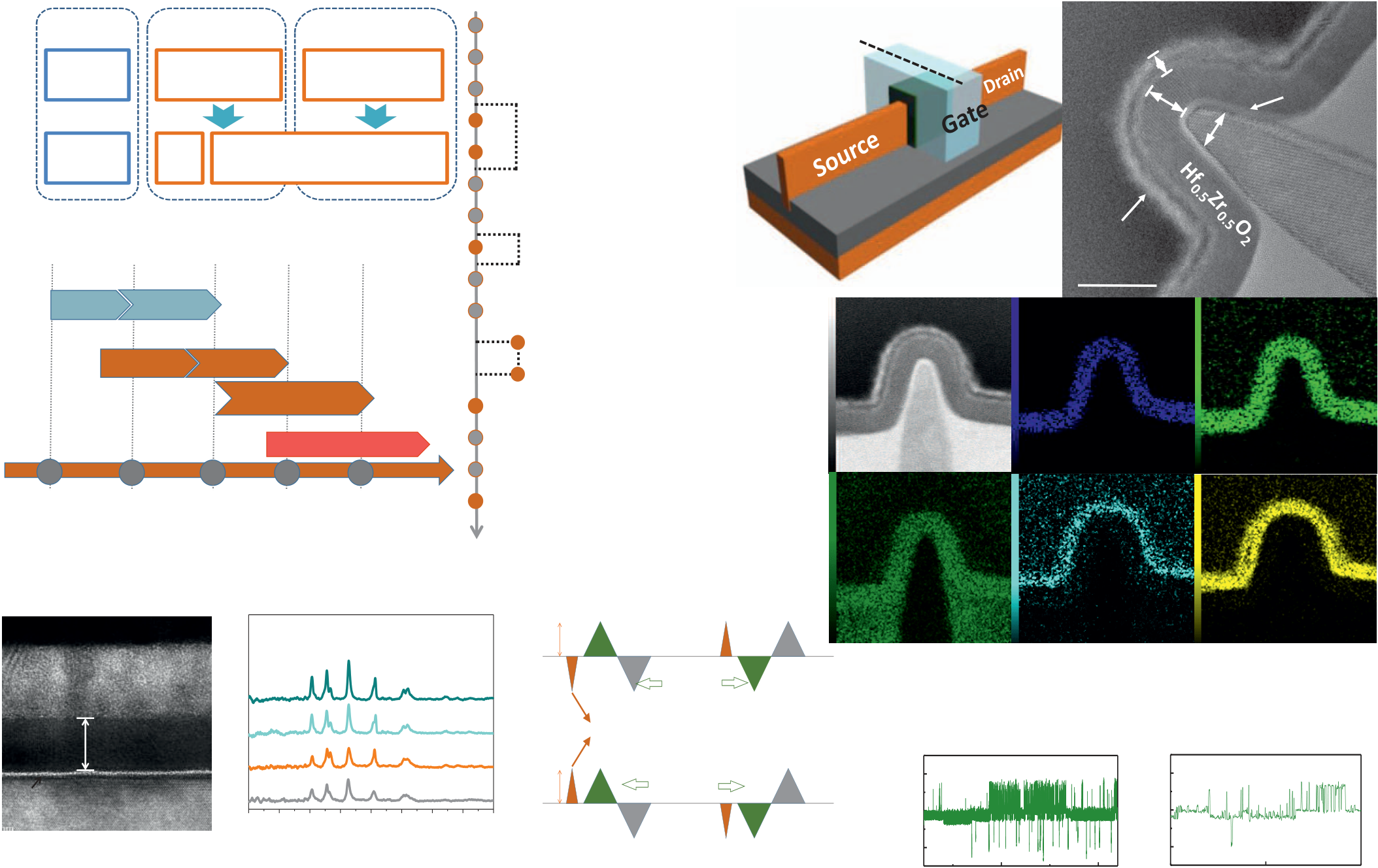
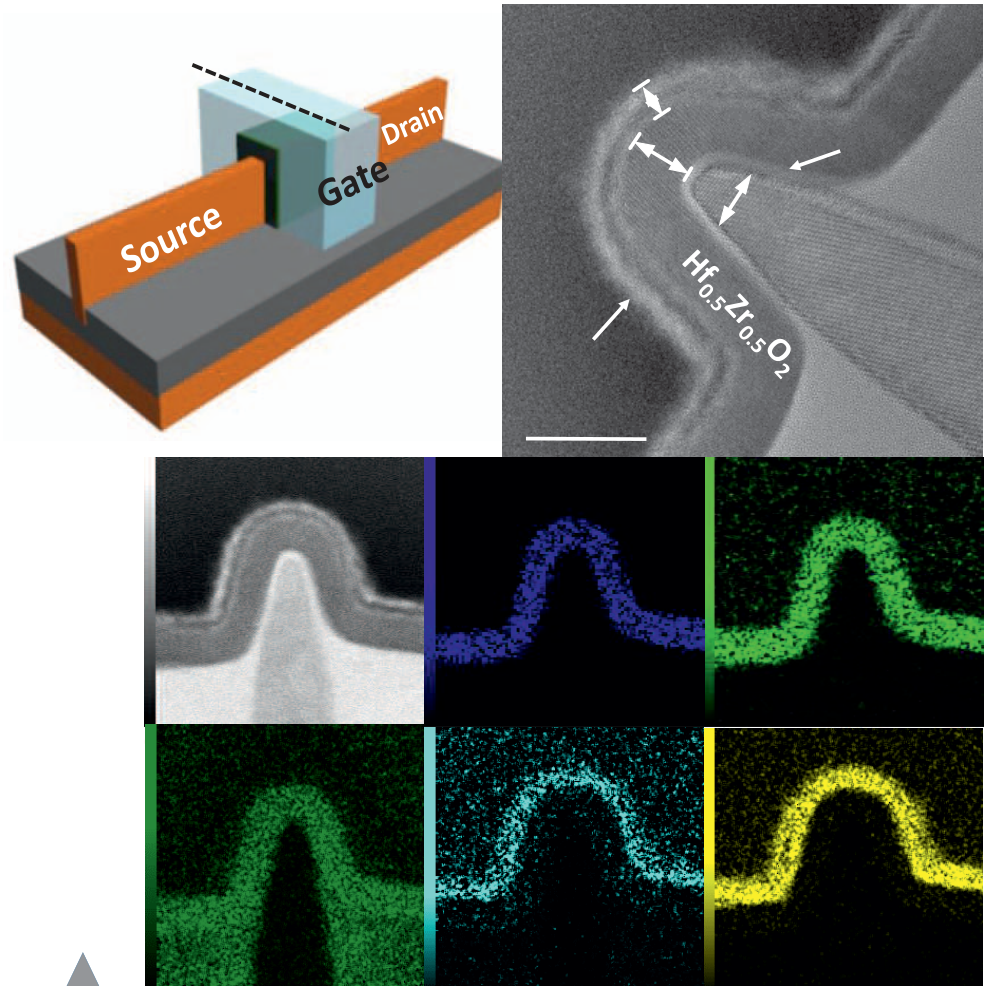
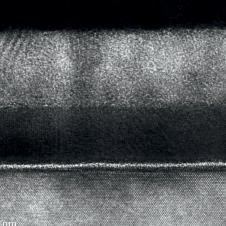
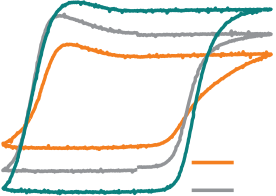
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| shorter switching time. Programming and erase speed as high | | | | | | | | [4] | D.-I. Moon, et al.���������������������������-speed and prolonged |
| as | 20ns | was | achieved | under | 2.6V | and | -3.8V, | [5] | �������������������������������������������������������������������� |
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| respectively.**Fig.15** shows the endurance test result under | | | | | | | |
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| successive voltage pulses with 3V/20ns for program and - | | | | | | | | [6] | storage in 28 nm HK��������������������������������������������� |
| 4V/20ns for erase. After 1012 cycles, the �V~0.5V can still be | | | | | | | | pp. 25�26. |
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| well maintained. Stable retention was also confirmed at 85 � | | | | | | | |
| featuring steep sub-60-mV/decade operation, fast 20-ns speed, and |
| for 104 s as shown in **Fig. 16.**Compared with other 1T-DRAM | | | | | | | |
| robust 85 °C-extrapolated 1016 ������������ ��� ������ ������ ����� |

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| **Compute** | | **Memory** | | **Storage** | | **Well implant** | **(a)** | **A** | **Si** | **B** | **Hf** | **W** | ������� | **(b)** |
| **Fin formation by SIT** | |
| **CPU** | | **SRAM** | | | **eFlash** |
| **STI recess** | | **IL** | |
| v | | | | | |
| **CPU** | | **SR** | **eDRAM&eNVM** | | | ***PTSL IMP*** | | **O** | ������� | | **Si** |
| ������� | |
| ***RTA (800C 60s)*** | |
| **AM** |
| **Dummy gate formation** | |
| ; | Fig.1 Evolution of memory hierarchy in embedded system. | | | | | **TiN/TaN/TiN** | |
| **Spacer + SD imp** | |
| ***SD anneal (1050C spike)*** | |
| **20 nm** | |
| **e-Flash** | | | | | | **ILD0 + CMP**  **dummy gate removal** | **(c)** |
| **55nm** | | **40nm** | | | | **Zr** | |
| **e-RRAM&e-MRAM** | | | | | | ***Self-aligned PTSP IMP*** | |
| **130nm** | | | **40nm** | | |
| ***RTA (1050C spike)*** | |
| **28/22nm**   **14nm**� | | | | | |
| **Hf0.5Zr0.5O2 dep. By ALD** | |
| **N** | **Ti** | |
| **TiN/TaN/TiN/W fill + CMP** | |
| **ILD1 + Contact** | |
| **2014 2016**  **2018 2020 2022**  Fig.2New memory will become the main | | | | | |
| **RTA Hf0.5Zr0.5O2 crystallization** | |
| Fig.3 Process flow of FE-FinFET. | |
| solution of embedded NVM in advanced | | | | | |

technology nodes.

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| **(a)**  **W**  **GXRD**  **(b)**   **Hysteresis Hysteresis**   **Volt Volt**   **S1**   **112o**   **020o 200o**   **111o** 2Pr (uC/cm)   **130o**  **TiN**  **600C**   **(i)**  **LOGIC 1**  **(ii) S2**  Fig. 4a)The structure schematic,(b)TEM image and c)the  EDX mapping for Hf, Zr, O, N and Ti over the cross- **311o 222o**   **004o**   **133o**  Intensity (a.u.)   **500C**  **Present Pulse**  **S = SWITCHING**  section A-B of the device.  **10.7 nm Hf0.5Zr0.5O2**  **400C**  **NS = NON-SWITCHING**  Current (pA) PSDA2/Hz   Current (pA) Number  **(i)**  **(ii)**  70 70  **IL**  **RT**  **NS1**  **LOGIC 0**  **Si**  **10**  **20**  **30**  **40**  **50**  **60**  **70**  **80**  **90**  **NS2**  60 60  2 Theta (o)  Fig.6 Remanent hysteresis could be 50 **(a)**  50 **(b)**  Fig.5 a) TEM of planar HZO capacitor with ~0.8  nm interfacial layer (IL) SiO2. b) GXRD of HZO.  -10  -20  20  10  0   |  |  |  | | --- | --- | --- | | |  |  | | --- | --- | | **(a)** | **TiN-5nm**�  **400 oC**  **500 oC**  **500 oC** | |   35  30  25  20  15  10  5 10 15 20 25 30   **400**�  **500**�  **600**�  obtained by PUND test (subtract the  current of Logic 1 and Logic 0).  **(b)** (b)  **E1**  **E2**  **E2>E1**   **HZO (�r�30,d1=10nm)**  **SiO2 (�r=3.8,d2=0.8nm)**   **TiN**  **Si V=E1d1+E2d2**  Fig.9 a-b) the RTN signal of IG, c) There are five   6000  3000  0   |  |  |  |  | | --- | --- | --- | --- | |  | | | | | **(c)** | | | |   55  Current (pA)  0.05  Time (s)  60 65   0.10  70   **10**  **10**  **-18**  **-23**  10   |  |  |  |  | | --- | --- | --- | --- | | **f2/1**  **(d)**  **f2/1** | | | |   1  Frequency (Hz)  Time (s)   0.049  10 3 10 5 Polarization (uC/Cm)  Fig.7 a)P-V characteristics of Si/IL/HZO/TiN with   -4 -2  Voltage (V)   0 2 4  TiN Thickness (nm) Fig.8 Voltage drop on IL lead to  the large coercive voltage   peaks of the IG RTN signal. d) The PSD curve  indicatesthe existence of multi-traps in HZO. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| different annealing temperature.b) Summary of the | | | | | | | | | | | | -6  10 | | | | | | | | | | | | | | | | | | | | | |
| changes in 2 Pr as a function of TiN thickness. | | | | | | | | | | | | ID (A)  -8  10 | | | | | | | | | | | | | | | | | | | | | |
| **Negative Voltage (-V)** | | | | | | | **Positive Voltage (+V)** | | | | |
| 10 | -6 | -4 | **FEFET** | | | | | **VG** | | 3 | VT | | -10 10 | **VT** | | -1  VG (V) | 0 | **VT** | **VT** | | | | | 0 | -2 | **VT** | 0 | **VT** | **VT** | | | | |
| 10 | -7 |
| **FEFET** | | -0.2 | -2 | -1  VG (V) | 0 | -2 | | -1 | -1  VG (V) |
| -2 | | -2 | -1  VG (V) | 0 | -2 | -1  VG (V) | 0 |
| 10 ID (A)  10 | -8-9 | **VT** | **VSDB** | | | | VG (V) |
| **VT** | | **Charge trap** | | | | | | **FEFET** | | | | | |
| -0.4 |
| **VG** | |
| -0.6 |
| **holes**  **CTM** | | | | | **memory window** | | | | | | **memory window** | | | | | |
| -10 10 | | **holes** | |
| -0.8 |
| **CTM** | |
| -11 10 | | -1.0 |
| **VSDB** | | | | |
| **VT** | | -1.2 |
| **VTIntitial VT** | | | | |
| -12 10 | | -1.4 |
| -3 | -2 | | -1 | 0 | 1 | 2 | -1.6 |
| Fig.10 | | Impact | | of | VG (V)  trapped electric | | | | charges | | and | | | | -5 | | | | 1 | | | 2 3  Sweep Voltage (V) | | | | | | | 4 | | 5 | | |

ferroelectric polarization on the threshold voltage of a field effect transistor.

Fig.11 With different operation voltage (<3V or >5V), this device shows Charge trap memory behavior or Fe-FET behavior.

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**For embedded 1T-DRAM application**

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| -0.2  10  -6  -8   **0.6V**  **Memory behavior**   **Charge Trap**   99.5  95  -0.3  -0.4  -0.5 **Memory**   **Target VT**  **(a)**   -0.4  -0.5  -0.6   **(b)**  5us   **Memory**  **Window**  Cumulative probability (%) Current (A)  ID (A) VT (V)   VT (V)   VT (V)  10  10  10  -10  -12  -3   **Vd=100mV**  -2 -1 0   **100 cycles**  **IV sweep**  1 2 0.1   70  40  10  1  -1.0 -0.8   **0.6V**  -0.6 -0.4  -0.6  -0.7  -0.8  -0.9  -1.0   **Window**  **0.5V**  0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5  5us  1us  100ns  20ns  -0.7  -0.8  -0.9  -1.0  0   **Target VT**  1us  100ns  20ns  1 2 3   **0.5V**  4 5  Fig.12 consecutive DC cycles of   VG (V)  Fig.13 Cumulative probability of   VT (V)  Fig.14The VT shift after VG pulse (a) program and (b) erase operation.   Pulse VG (V) Pulse VSDB (V)  the device for 100 cycles VT after program and erase.  -0.3  -0.4 10  -7 **@85�**  **���������������������������������**  **and the worst assessment scores**   **Speed**  6  5  Fig.15Endurance test. The device  -0.5  -0.6  -0.7  -0.8  -0.9  -1.0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |