Highly Stackable 3D Ferroelectric NAND Devices : Beyond the Charge Trap Based Memory

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| ***Abstract*—In this study, we demonstrate for the first time the** | | formation is influenced by the fabrication conditions, dopant | |
| **multi-level capable 3D ferroelectricNAND (Fe-NAND) device** | | type, and dopant concentration. HfO2 based ferroelectric | |
| **using the 3D NAND test vehicle for mass production. The** | | research is mostly performed based not on 3D NAND, but on | |
| **present 3D ferroelectric NAND shows the potential multi-level** | | 2D ferroelectric capacitor or ferroelectric field effect transistor | |
| **cell operation with the 3.4 V program/erase window. We also** | | (Fe-FET) [4-6]. Thus, the properties and mass-production | |
| **reported cycling and retention characteristics.** | |
| possibilities of HfO2 based 3D ferroelectric NAND(3D Fe- | |
| ***Keywords—3D NAND, Ferroelectric, scalable*** | | NAND) have not yet been verified. Few existing papers | |
| propose the 3D Fe-NAND structure [7] but they utilize 3D | |
| I.INTRODUCTION | | NAND mimicking vehicles which have lower process | |
| integration complexities than that of the current product, | |
| Currently, 3D NAND research focuses on the Bit-Cost | |
| making it difficult to accurately prove the mass production | |
| Scalable(BiCS) flash memory technology to integrate the high | |
| possibility of the 3D Fe-NAND. | |
| density memory cells in the 3D NAND chip. However, charge | |
| trap nitride(CTN) based 3D NAND, the main-stream flash | | The present research proposes the 3D Fe-NAND by | |
| memory technology, faces physical limits on cell density | | designing ferroelectric cell integration processes on the | |
| improvement. The cell density improvement of the CTN | | conventional 3D CTN NAND test vehicle for mass production | |
| based 3D NAND is limited largely by two main factors: i) | | by substituting the ONO layer with the HfO2 ferroelectric | |
| threshold voltage(Vth) shift due to the cell to cell interference | | layer. The fabricated 3D Fe-NAND enables the multi-level | |
| caused by charge migration and dispersion and ii) spacer oxide | | cell(MLC) operation of the 3D Fe-NAND by having 2.4 V of | |
| thickness limitation due to the high voltage operation. | | the program/erase(P/E) window and 365 days of the data | |
| retention properties, thereby proving that HfO2 cells in the 3D | |
| Ferroelectric 3D NAND can be considered one of the | |
| Fe-NAND have uniform performances. Additionally, the | |
| possible alternatives to improve the cell density of the 3D | |
| present research shows that the 3D Fe-NAND is applicable to | |
| NAND by overcoming the weakness of the CTN based 3D | |
| the next generation 3D NAND by experimentally verifying | |
| NAND mentioned above. In particular, the HfO2 based | |
| the cell characteristics prepared with the same level of | |
| ferroelectric cell is known for maintaining the polarity in the | |
| fabrication complexity and cell density as those of the 3D | |
| ferroelectric cell numerically down to 3 Å [1] and 2 nm [2], | |
| CTN NAND product. | |
| minimizing the interference between the cells and enabling | |
| cell density improvement. The Ferroelectric cells change the | | II.EXPERIMENTS,RESULTS AND DISCUSSION | |
| program and erase (P/E) state at lower voltage than that of the | | *A.Experimental design* | |
| CTN [3], therefore reduces the required spacer oxide | |
| thickness. Thus, it can mitigate aggressiveness of stack up | | The 3D Fe-NAND is fabricated on the conventional 3D | |
| trend of conventional CTN based 3D NAND. | | CTN NAND test vehicle in order to have similar process | |
| complexity to the 3D CTN NAND mass production vehicles. | |
| The various electrical properties of the HfO2 complicate | |
| The 3D Fe-NAND integrates the HfO2 ferroelectric layer, | |
| its integration into the 3D NAND fabrication processes due | |
| replacing the ONO(Oxide/Nitride/Oxide) stack of the | |
| to the co-existence of the multiple phases[4] of the HfO2 layer. | |
| conventional 3D CTN NAND. Figure 1 shows the schematics | |
| The composition of the multiple phases of the HfO2 layer is | |
| of the fabricated 3D Fe-NAND of the present work. As shown | |
| determined by the process conditions. The HfO2 has three | |
| in Fig.1(a), the gate is composed of TiN and W. The HfO2 | |
| major electrical properties: dielectric, anti-ferroelectric, and | |
| ferroelectric layer is sandwiched by the SiO2 layer and the | |
| ferroelectric. The property depends on the phases of which | |
| poly silicon layer which is the ferroelectric protection layer | |

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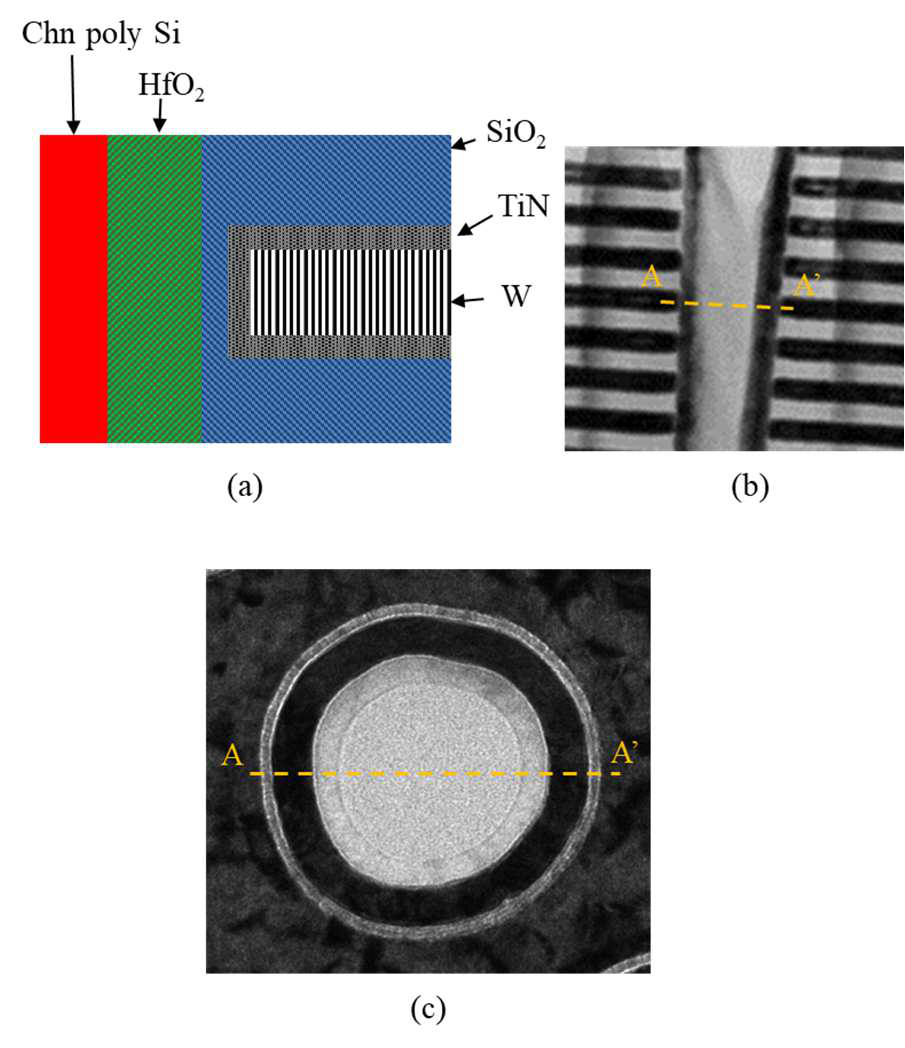


Fig. 1. 3D ferroelectric NAND(3D Fe-NAND)   
structure: (a) schematic cross-section structure; (b) cross-section TEM; (c) plane TEM of A-A’ of Fig. 1(b)

and channel layer, respectively. The HfO2 ferroelectric layer is carefully prepared by atomic layer deposition(ALD) with fine control of the composition for optimum ferroelectric properties. It is then integrated into the process flow similar to the conventional 3D CTN NAND with the same subsequent thermal budget. A typical TEM cross-section and plan-view image of the cell is shown in Fig.1 (b) and (c), respectively. The properties of the 3D Fe-NAND for data storage, such as data retention time and the P/E windows, are experimentally verified . The MLC operation of the 3D Fe-NAND is tested by measuring the Vth distribution to estimate the possibility of 3D Fe-NAND mass production at the research level,.

The Vth of the 3D Fe-NAND moves in the opposite direction compared to the conventional 3D CTN NAND. The Vth of the 3D Fe-NAND decreases or increases when applying postive or negative bias on the HfO2 ferroelectric layer respectively, because of the ferroelectric characteristics as explained in Fig. 2.

The P/E window is defined as the difference between the maximum and minimum Vths by applying the program bias voltage in the range of 6 to 13 V after applying the erase bias voltage of 10 V. The data retention and 3k cycling endurance are also tested. The data retention property of the 3D Fe-NAND in this research is defined as the 0.6 V degradation of the Vth in 365 days. The data retention is measured by the time dependent Vth degradation of the 3D Fe-NAND. The Vth degradation time required for 0.6 V of the Vth displacement is extrapolated after the Vth shift measurement for 6 minutes. The Vth degradation slope less than 0.121 V/Dec in Vth-time(log scale) corresponds to the Vth displacement less than 0.6 V , or to the data retention time over 365 days. The endurance properties are verified by the P/E window change between the initial P/E window and the window after applying the P/E bias of -9 and 12 V up to 3000 times. The TLC operation possibility is tested by measuring the Vth

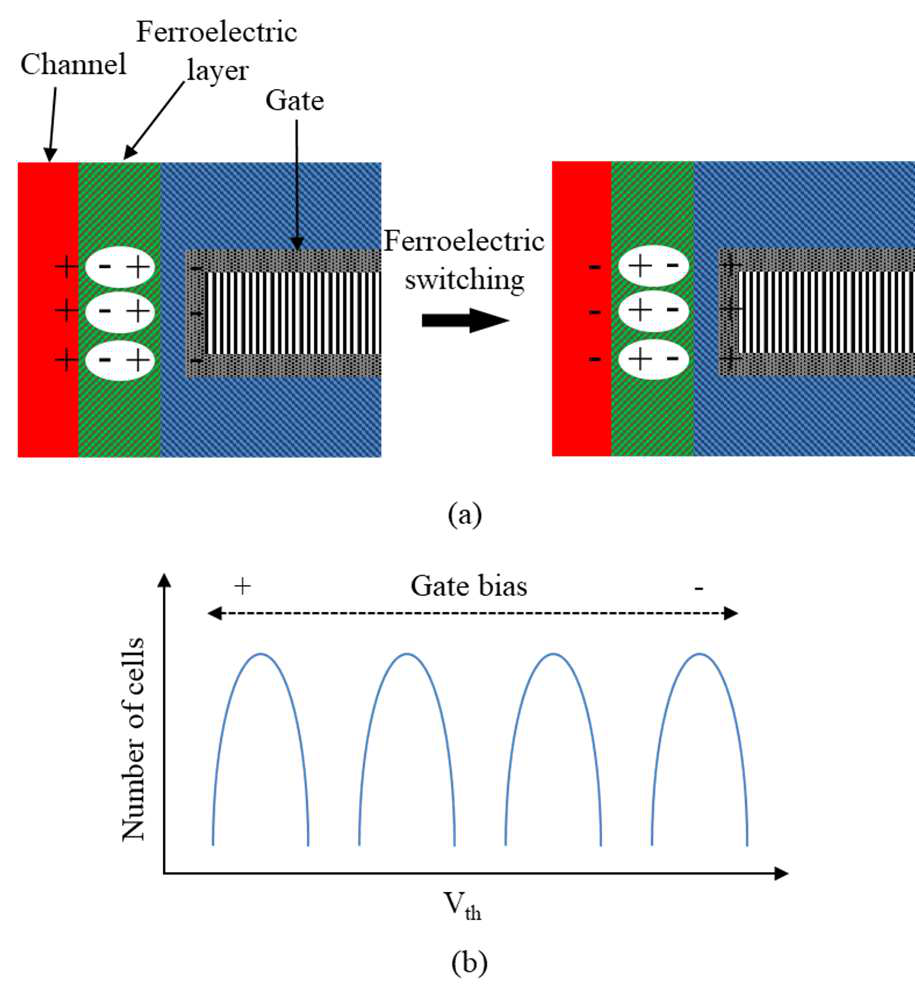


Fig. 2. Working principle of the 3D Fe-NAND: (a) ferroelectric switching mechanism; (b) threshold   
voltage(Vth) movement direction depending on the gate bias.

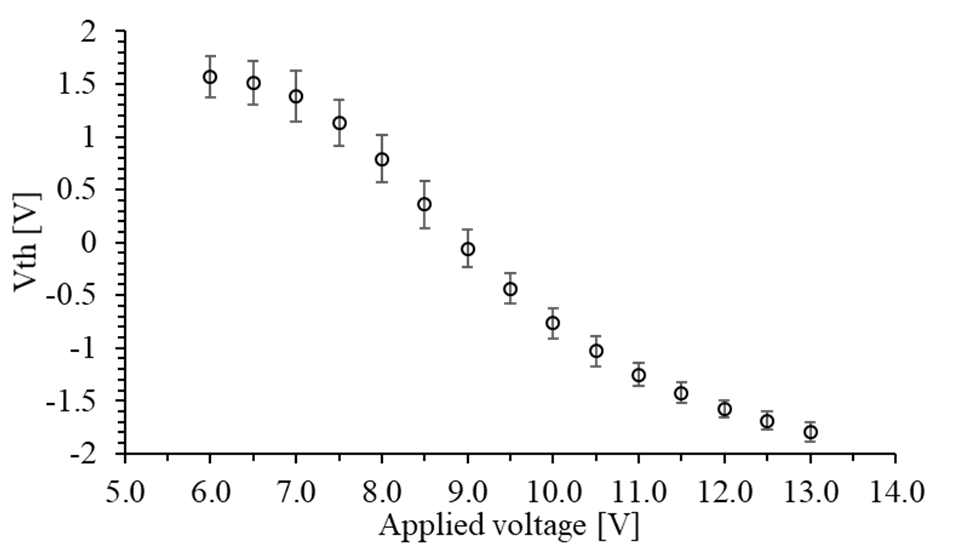


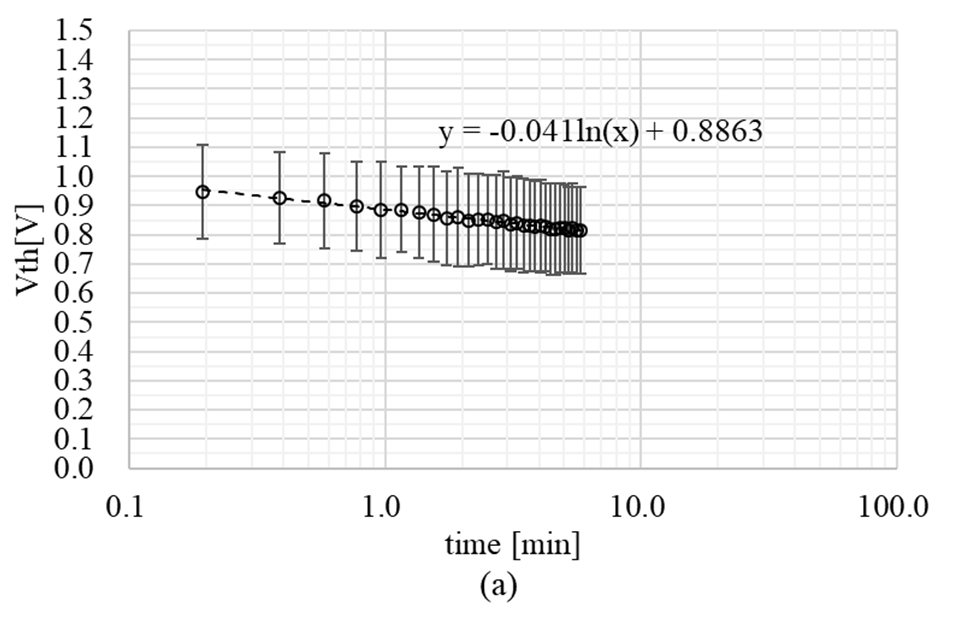
Fig. 3. Vth movement of the 3D Fe-NAND by applying the program bias in the range of 6 to 13 V after the erase operation

distribution in the Vth range of -1.80 and 1.35 V at 0.45 V intervals considering the given P/E window. The TLC operation after the 3k cycling is also verified. All the experimental data in this paper are collected from 13 points in one wafer.

*B.Experimental results and discussion*

The fabricated 3D Fe-NAND in the present research shows the P/E window of the 3.4 ± 0.29 V (See Fig. 3). It also shows the data retention slope of the 0.041 V/Dec (See Fig. 4a), and the P/E window shift after the 3k cycling 0.5 ± 0.27 V (See Fig. 4b). The Triple-level cell(TLC) operation of the device is tested by including 8 levels of the Vth states in the P/E window with the minimum gap margin of 0.16 V(See Fig. 5). The 8 states of the Vth for the TLC operation targeted at -1.70 V, -1.35 V, -0.90 V, -0.45 V, 0.00 V, 0.45 V, 0.90 V, and

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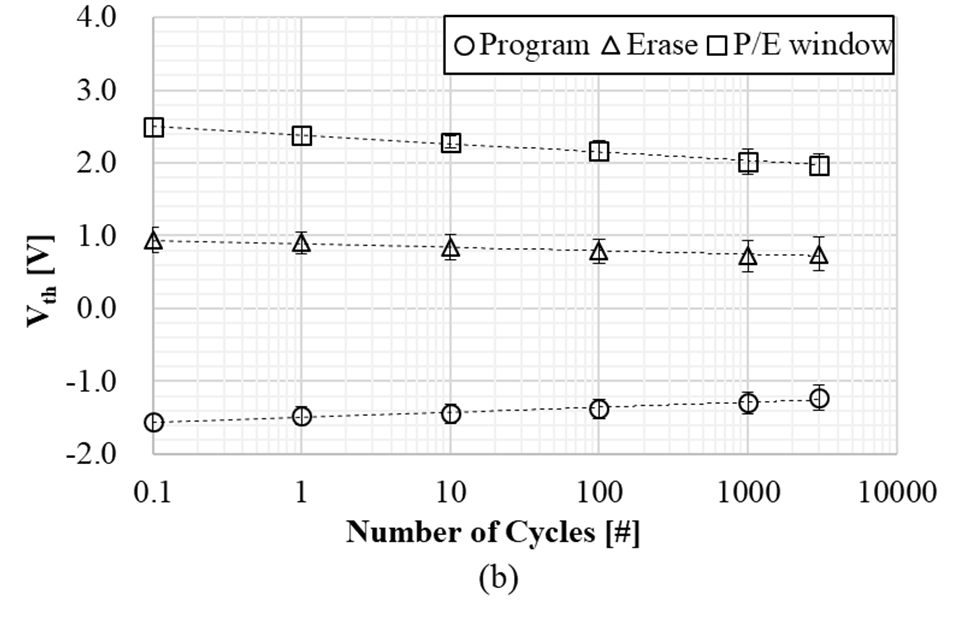
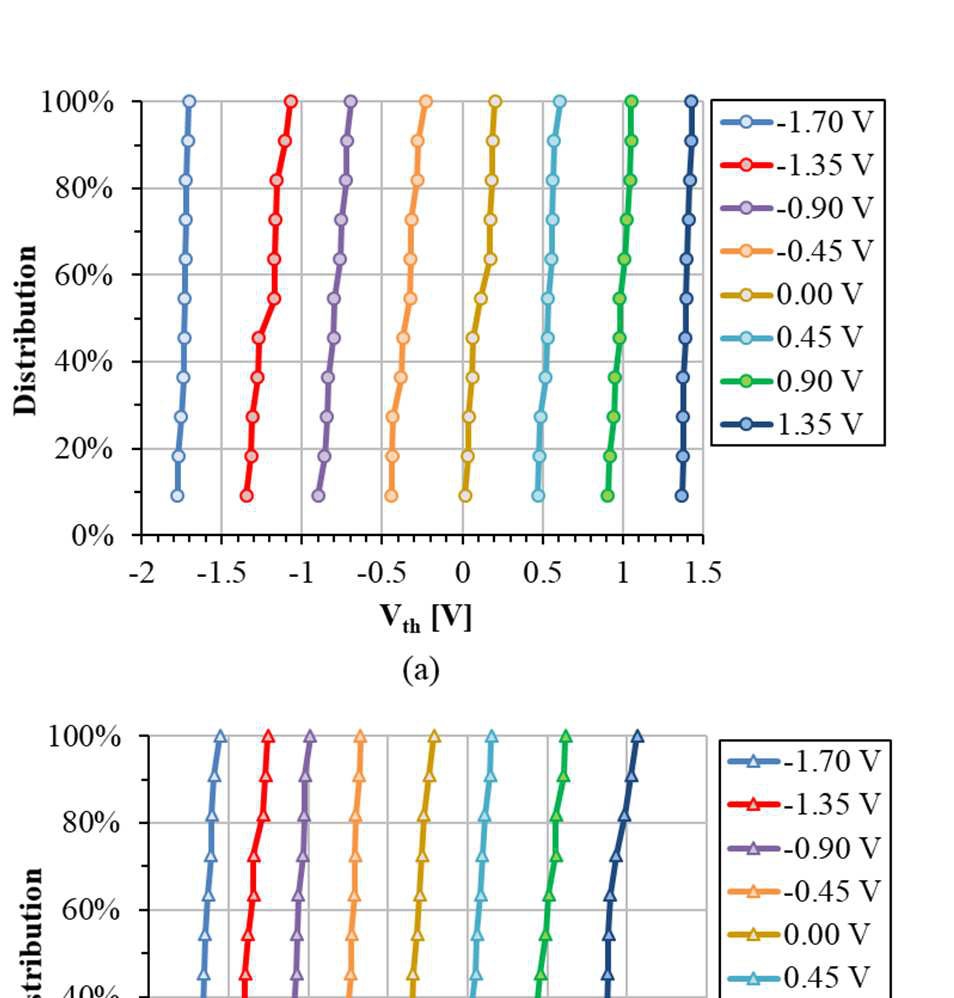


Fig. 4. Endurance test results of the 3D Fe-NAND: (a) Vth movement depending on time; (b) Vth movement depending on the cycling numbers of the program bias (12 V) and the erase bias (-9 V).

1.35 V. The Vths verified at -1.73 � 0.023 V, -1.21 � 0.093 V, -0.79 � 0.065 V, -0.35 � 0.072 V, 0.12 � 0.068 V, 0.53 �0.043 V, 0.99 � 0.054 V, and 1.40 � 0.022 V are moved to -1.64 � 0.046 V, -1.35 � 0.062 V, -1.06 � 0.046 V, -0.73 �0.072 V, -0.32 � 0.068 V, 0.05 � 0.069 V, 0.48 � 0.091 V, and 0.91 � 0.087 V, respectively, thereby showing the minimum gap margin of 0.16 V in TLC operation. The 8 verified Vths are moved to -1.65 � 0.030 V, -1.41 � 0.023 V, -1.10 � 0.042 V, -0.80 � 0.063 V, -0.48 � 0.074 V, -0.1 �0.11 V, 0.2 � 0.13 V, and 0.6 � 0.15 V after the 3k cycling (See Fig. 6). The gap margin of 0.16 V is reduced to 0.04 V after the 3k cycling.

The cell Vth distribution of the 3D Fe-NAND is not tight enough for the TLC operation considering the gap margin after the 3k cycling. However, the Vth verification in 8 states in the P/E window with the Fe-FET is reported for the first time in the present research, to our knowledge. The TLC Vth verification in this research shows the ferroelectric cells in the 3D Fe-NAND have characteristics uniform enough for mass production, even with the fabrication process complexity of the conventional 3D CTN NAND.

The TLC operation of the 3D Fe-NAND requires the larger P/E window and the longer data retention time. The P/E window of the Fe-FET could be enlarged by adding dopants in the HfO2 based ferroelectric layers[8] by increasing the coercive voltages(Vc) of the Fe-FET. Such dopants include Si, Gd, Y, Zr, or La[8]. These dopants can easily be incorporated into the ferroelectric layer during the ALD process. The P/E window is known to be proportional to the Vc [9]. The data



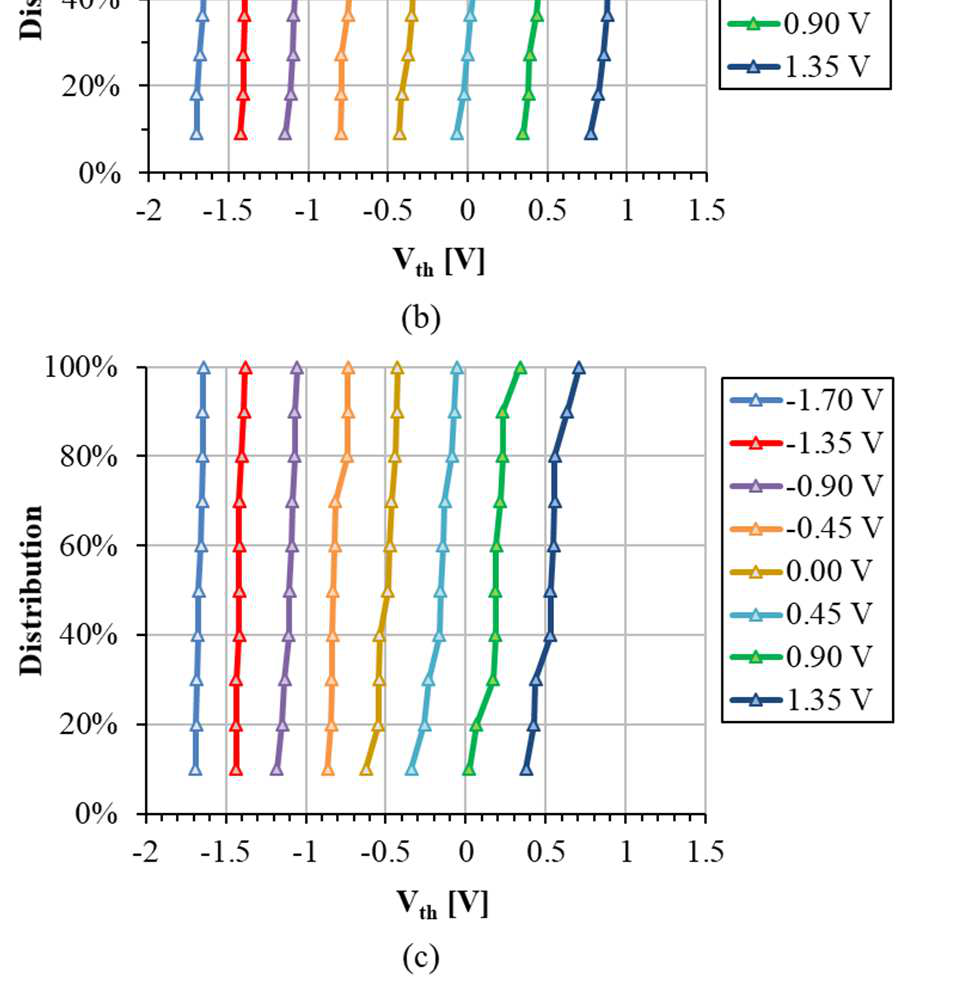


Fig. 4. TLC verification of the 3D Fe-NAND: (a) initial Vth distribution; (b) Vth distribution after the read   
operation; (c) Vth distribution after the 3k cycling of the program bias (12 V) and the erase bias (-9 V).

retention time can be improved by further understanding the charge injection mechanisms at the interfaces between the ferroelectric layers and the gate or channel.

III.CONCLUSION

In summary, we fabricated and characterized the HfO2 based 3D Fe-NAND using conventional CTN NAND based integration process flow. The 3D Fe-NAND MLC operation was verified experimentally for the first time to our knowledge with the P/E window of 3.4 ± 0.29 V and data retention time over 365 days. We also demonstrated TLC Vth placement, proving the uniform characteristics of the cells and subsequently suggesting the viability of potential mass

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production capability. Yet, the process still requires further improvement in the P/E window and the data retention for the MLM operation at a product level. Regardless, it is a strong candidate for next generation 3D NAND memory.

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