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**First Demonstration of Vertically Stacked Ferroelectric Al Doped HfO2 Devices for NAND Applications**

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**Abstract:** A 3D ferroelectric Al doped HfO2 device for NAND applications was fabricated for the first time. The polysilicon (poly-Si) channel, whose diameter ranges from 60 to 200 nm, was highly doped for a better understanding of the ferroelectric properties. Electrical results confirmed the presence of the ferroelectric phase with a coercive voltage (2Vc) of 6 V extracted from the hysteresis loop. The drain anneal was found to have a significant impact on HfO2 properties and needs to be reduced to preserve the ferroelectricity. Finally, reliability investigations showed an estimated time to failure of more than 10 years at 85 °C. This study lays the foundation for the fabrication of 3D ferroelectric field effect transistors (FeFET).

**Introduction:** Ferroelectric (FE) materials are very promising candidates for memory applications due to their spontaneous polarization, which can be reversed by the application of an electric field. New interests have recently emerged in this area with the discovery of ferroelectricity in HfO2 [1]. The presence of a small amount of dopants, a capping layer and a thermal anneal facilitates the transformation of the monoclinic phase into a non-centrosymmetric orthorhombic phase, responsible for the ferroelectric behavior. Most of the published papers report on the fabrication of planar capacitor using TiN as metal electrodes [2-4]. Polakowski *et al.* reported the fabrication of deep trench capacitors based on Al:HfO2 with a 13:1 aspect ratio and TiN as metal electrodes [5].

In this paper, we report for the first time the fabrication of a vertical 3D NAND device with poly-Si gates, ferroelectric Al:HfO2 gate oxide and poly-Si channel.

**Device Fabrication:** Fig. 1 shows the process sequence for the cylindrical vertical channel with three cells in series. In this channel-last process, the Si substrate is firstly implanted to form the source junction and then annealed at 1050 °C for dopant activation. The 50 nm thick doped poly-Si gates are then successively deposited, separated by 30 nm thick SiO2. After dopant activation, vertical cylindrical holes with diameters ranging from 60 to 200 nm are etched. 9.5 nm thick FE-HfO2 is then deposited by atomic layer deposition, followed by a thin a-Si protective layer. The bottom of the hole is then opened and the hole is filled with a-Si, highly doped in this study, which serves as channel and drain after a further As implant. The stack is then annealed at temperatures ranging from 750 °C to 1050 °C for drain activation as well as FE- layer crystallization. Finally, the staircase is formed followed by metal contacts [6]. The schematic view of the vehicle is shown in Fig. 2. The cross-section of the final device can be seen in Fig. 3 with a hole diameter of ~70 nm. The bottom opening with recess in Si substrate can clearly be observed (Fig. 3 (a)) as well as crystallization of the channel (Fig. 3 (b)).

To analyze the crystal structure of FE-HfO2 through Grazing Incidence X-Ray Diffraction (GIXRD), a special layout was designed, in which the density of the holes was increased (Fig. 4), to amplify the signal intensity. After HfO2 deposition

along the holes, the layer was etched back to leave it only in the sidewall. Thus, only the signal from the vertical HfO2 in the holes was measured through GIXRD.

**Material and electrical characterizations:** GIXRD data can be observed in Fig. 5. A mixture of monoclinic and orthorhombic/cubic phases was detected.

Electrical measurements were performed using a 100k holes array. Polarization-Voltage (P-V) measurement after 1000 bipolar cycles at 5 V and a drain anneal of 850 °C is shown in Fig 6. A remnant polarization (2Pr) of 17 μC/cm2 and a coercive voltage (2Vc) of 6 V were extracted. The impact of drain anneal is shown in Fig. 7. High thermal budget seems to degrade the FE-layer, until it loses FE-phase.

Endurance was studied by applying successive bipolar pulses (Fig. 8). A drawback of FE-HfO2 is that the coercive voltage is close to the breakdown voltage. The endurance is thus limited by the applied voltage (greater than Vc). Before hard breakdown, the presence of leakage current deforms the P-V hysteresis (Fig. 9). A comparison in term of 2Pr, 2Vc and endurance at 4.5 V is given in Fig. 10. This clearly confirms the degradation of the ferroelectric property with increasing temperature.

Retention measurements were carried out at 85 °C and 150 °C at 5 V after 500 cycles, on the sample annealed at 750 °C. The procedure, based on [7], is given in Fig. 11. The imprint phenomenon was studied separately. As can be seen in Fig. 12, an asymmetrical horizontal shift, depending on the baked state, is observed with time, typical for imprint. Extrapolation with time for the larger Vc shift in each case is given in Fig. 13 with the assumption of a Vc limit of 4.5 V, at which all domains can no longer be switched, leading to a loss in 2Pr. An example of P-V results after retention testing is given in Fig. 14. Pr same state (Pr SS) is obtained by subtracting A’ from A and Pr opposite state (Pr OS) by subtracting B from B’ (Fig. 14). Extrapolation with time is given in Fig. 15. Assuming a remnant polarization limit of 9 μC/cm2 (~half of initial 2Pr), the predicted time to failure of Pr SS and Pr OS at 85 °C is more than 10 years.

Finally, TCAD 3D simulations were done and a good match was found between experimental and simulated data (Fig. 16).

**Conclusions**: A 3D ferroelectric Al:HfO2 device for NAND application has been fabricated for the first time. Electrical and material studies confirm the presence of the ferroelectric properties and reliability studies show the potential of this device for nonvolatile memory applications.

**References:** [1] T. S. Böscke, *APL*, 99, 102903 (2011). [2] S. Mueller, *AFM*, 22, pp. 2412-2417. [3] S. Mueller, *ECS J.*, 1, pp. N123-N126, 2012. [4] T. Schenk, *ESSDERC*, 2013, pp.260-263. [5] P. Polakowski, *IMW*, 2014, pp. 1-4. [6] E. Capogreco, *IEEE IEDM*, 2015, pp. 3.1.1-3.1.4. [7] J. Rodriguez, *IRPS*, 2004, pp.200-208.

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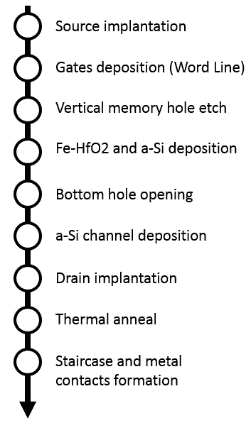
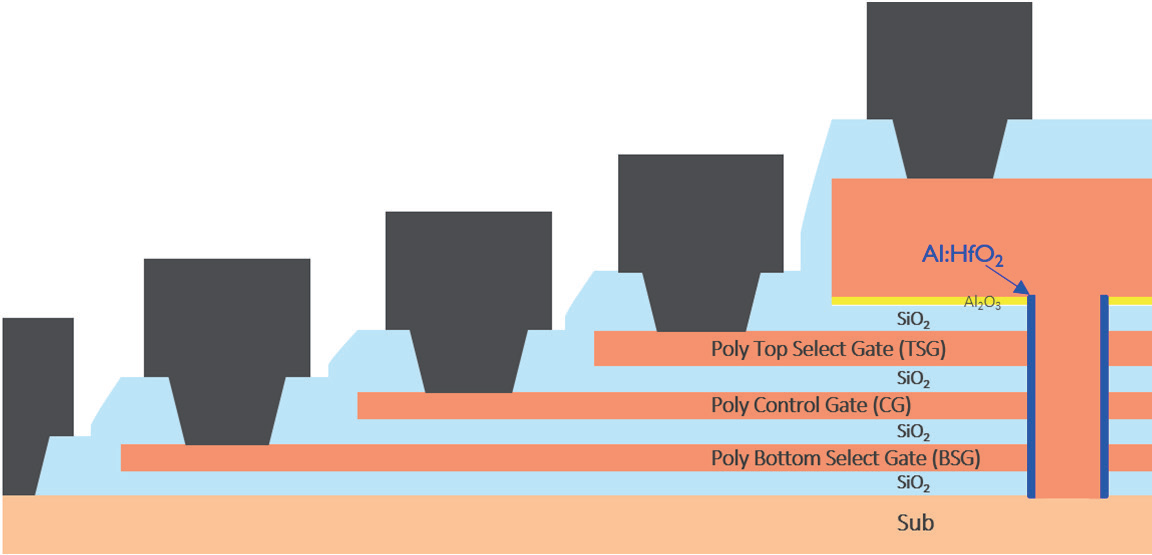
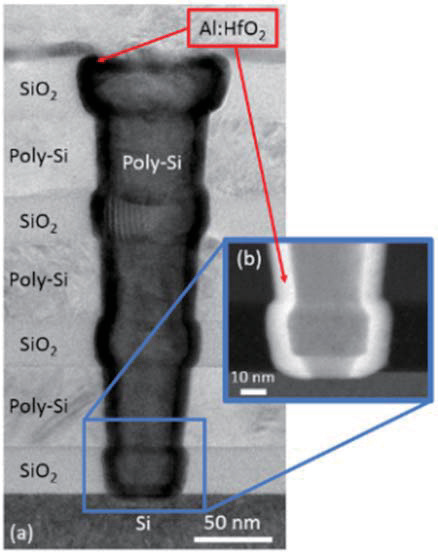
  

Fig. 1 Process flow for Fig. 2 Schematic view of the FeFET: three polysilicon gates, ferroelectric Fig. 3 (a) TEM cross-section. (b)

the vertical FeFET. Al:HfO2 surrounding a cylindrical vertical channel. STEM zoom of the bottom opening.

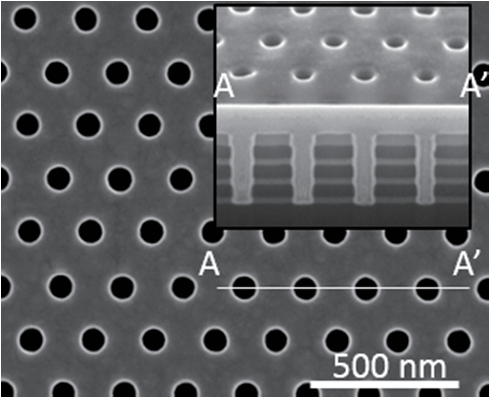
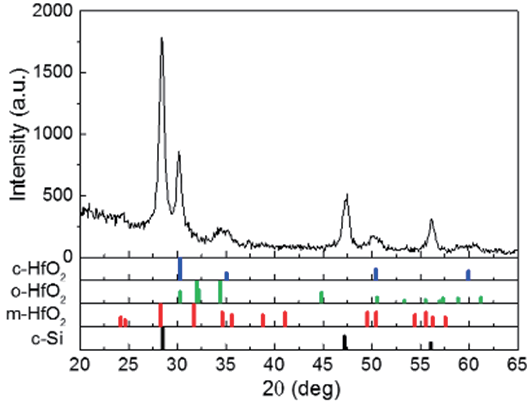
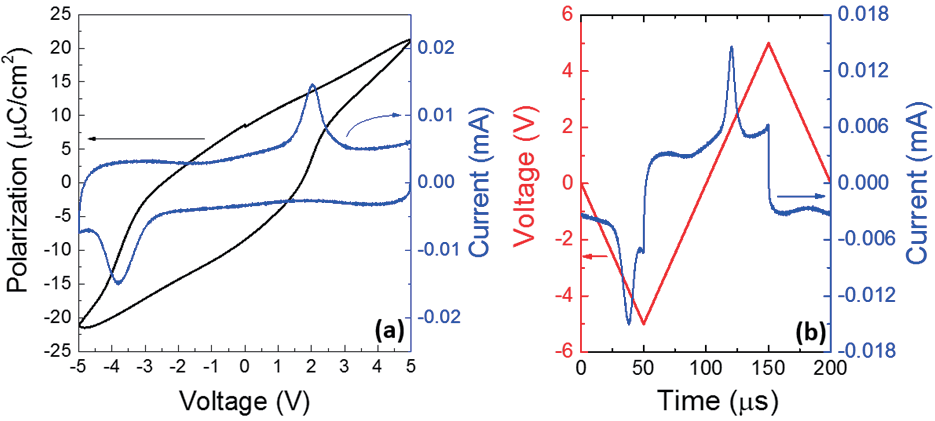
  

Fig. 4 Dense holes layout for Fig. 5 GIXRD data showing a Fig. 6 (a) P-V and I-V of a 100k array with a CD of 70 nm,

XRD. (inset: holes cross-section) mixture of m- and o/c-HfO2. annealed at 850 *°*C. (b) Corresponding V-t and I-t.

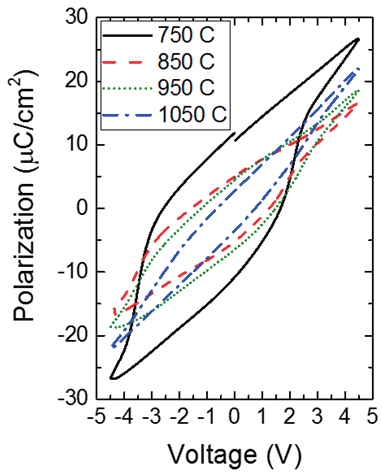
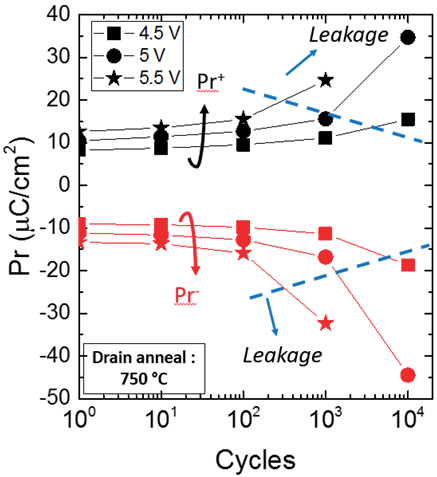
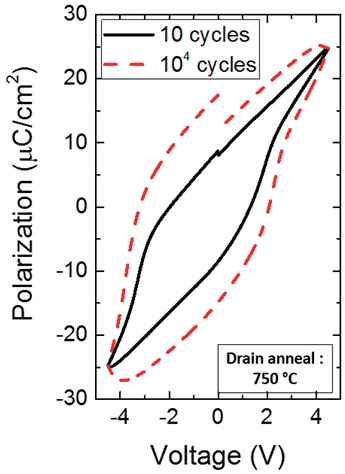
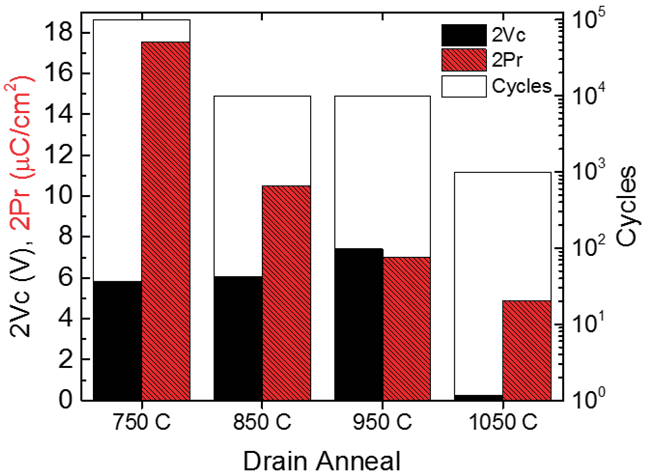
   

Fig. 7 P-V characteristics at Fig. 8 Endurance study at Fig. 9 Effect of leakage Fig. 10 Comparison of 2Pr, 2Vc and

various drain anneals. different voltages. current on P-V hysteresis endurance as a function of drain anneal

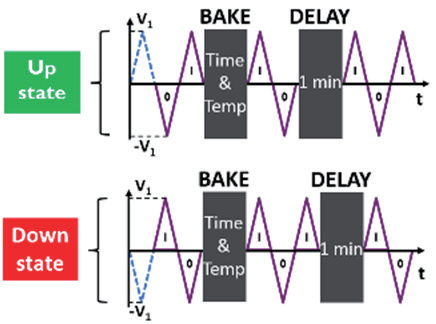
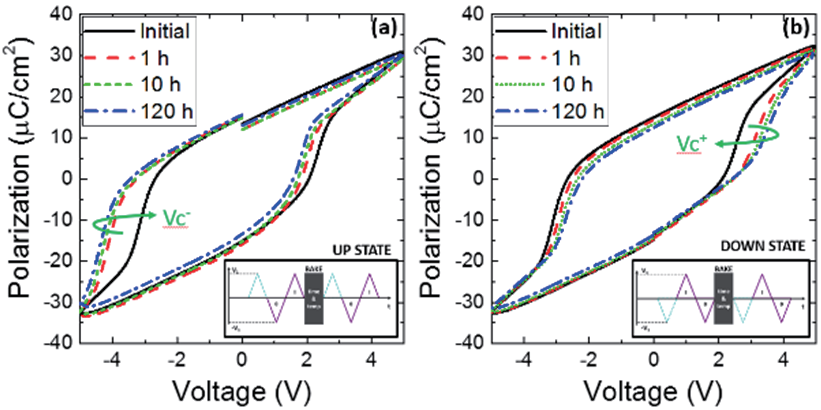
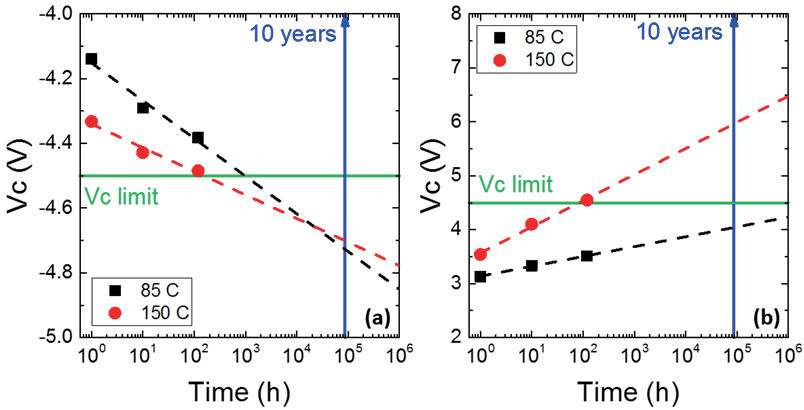
  

Fig. 11 Retention procedure Fig. 12(a) Imprint up state and (b) imprint down state Fig. 13 Extrapolation with time of (a) Vc- imprint up

with 1 min delay*.*  at 85 °C. (insets: imprint procedure) state and (b) Vc+ after imprint down state.

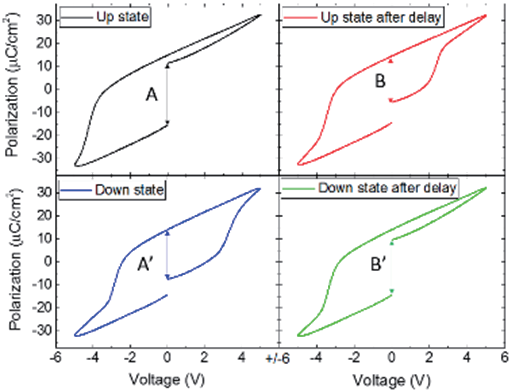
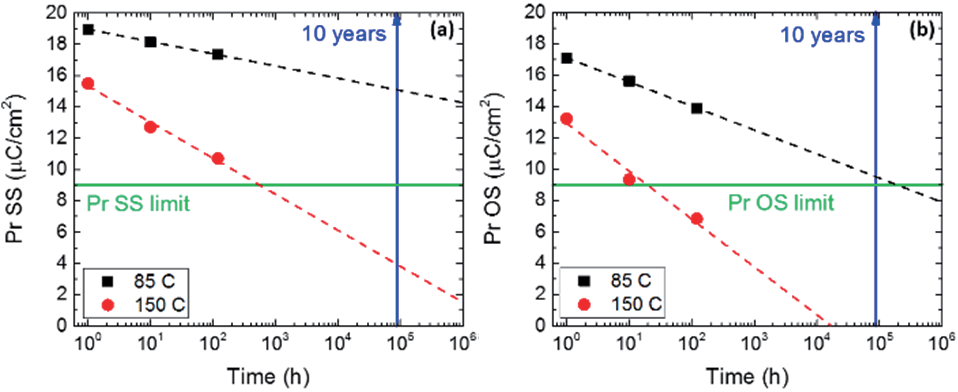
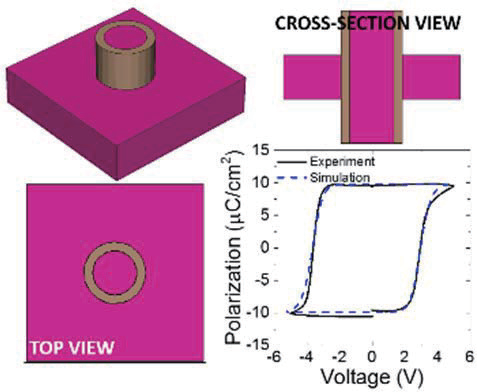
  

Fig. 14 Retention P-V Fig. 15 Extrapolation with time of (a) Pr SS and (b) Pr OS. Fig. 16 TCAD simulation of P-V

measurements at 85 °C after 10 h. hysteresis.

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