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Unraveling the Dynamics of Charge Trapping

and De-Trapping in Ferroelectric FETs

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***Abstract— In this work, a comprehensive study of charge trapping and de-trapping dynamics is performed on n-channel ferroelectric field-effect transistors (nFeFETs) and pFeFETs. It is discovered that: 1) the degree of charge trapping depends on the substrate that nFeFETs exhibit significant electron trapping but negligible hole trapping during memory write while pFeFETs exhibit much less electron trapping but significant hole trapping when heavily stressed; 2) due to enhanced electric field in the interlayer and semiconductor, the like initial polarization states (i.e., initialized by a pulse of the same polarity as the write pulse) could exacerbate charge trapping induced by the write pulse; 3) electron trapping is fully recoverable while hole trapping shows a semi-permanent component which involves interface trap generation; and 4) less significant charge trapping in pFeFETs allows immediate read-after-write at normal operating conditions.***

***Index Terms— Charge trapping, ferroelectric field effect transistor (FeFET), memory window.***

I. INTRODUCTION   
**H** fO2-BASED ferroelectric thin films are considered as the most promising enabler for high-performance and

energy-efficient ferroelectric field-effect transistors (FeFETs)

because of their CMOS compatibility, excellent scalability,

Manuscript received June 24, 2021; revised August 18, 2021, Octo-ber 22, 2021, and December 7, 2021; accepted January 11, 2022. This work was supported by the Semiconductor Research Corporation (SRC) Global Research Collaboration (GRC) Program under Contract 2020-LM-2999. The review of this article was arranged by Editor F. Schwierz. (Corresponding author: Shan Deng.)   
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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3143485.

Digital Object Identifier 10.1109/TED.2022.3143485

and superior energy efficiency [1]–[3]. Significant progresses in improving silicon FeFET performance and reliability have been accomplished ever since its discovery. For example, FeFET with memory window around 1.5-V and 10-ns write latency can be achieved with 4-V write pulses [4]. Process optimization has been underway such that the smallest FeFET size is pushed to 200 nm x 200 nm, above which the device-to-device variation is tightly controlled such that the bit error rate is low [5]. Endurance cycling is improving with the introduc-tion of new structures [6] and new interlayer dielectrics [7] such that 1010cycles are within reach. These advancements are exciting developments in making FeFET a competitive candidate for embedded nonvolatile memory (eNVM).

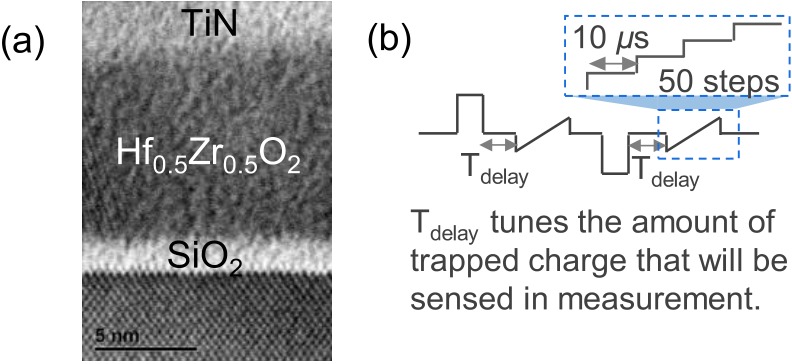
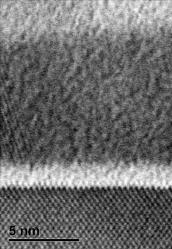
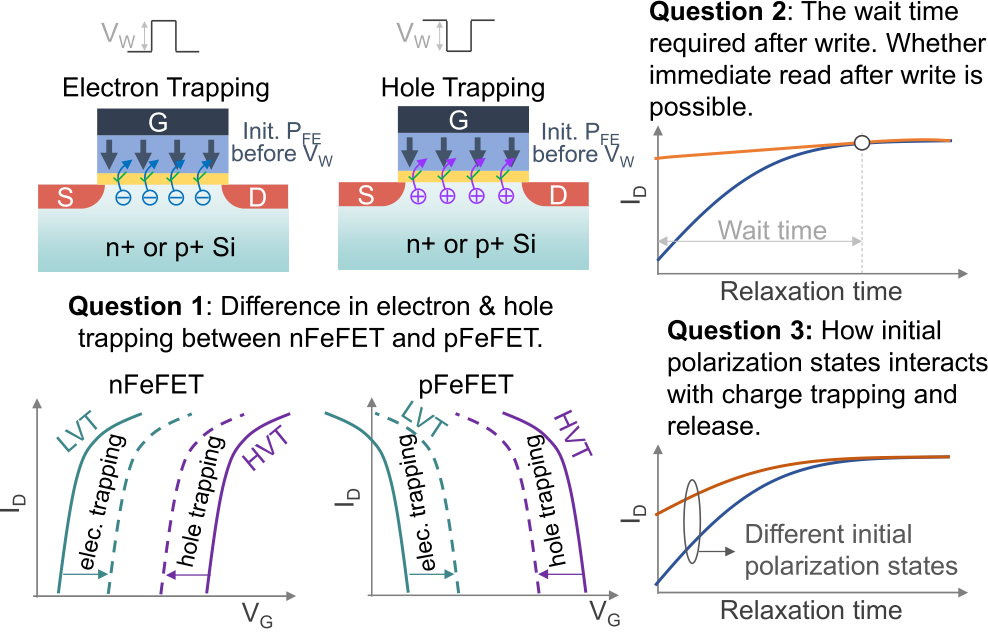
Charge trapping remains a major challenge in FeFETs due to the induced threshold voltage (*V*TH*)* instability [8]–[11], as shown in Fig. 1. HfO2 is known to have a high density of intrinsic defects, and the interface of HfO2/interlayer and interlayer/semiconductor is typically defective, which can trap electrons and holes [12]–[15], counteracting the *V*TH shift induced by polarization switching. For example, polarization switching after a positive gate pulse shifts *V*TH negatively, while the induced electron trapping in the gate-stack results in a positive *V*TH shift, diminishing the benefits of polarization switching.

It has been demonstrated that high polarization charge den-sity switched during memory write significantly stresses the interlayer [9], which as a result induces a significant amount of charge trapping and poses several reliability concerns. For example, to sense the polarization states in FeFETs, typically a long wait after write pulses is inserted before the memory read such that the trapped charges can fully relax and the polarization switching effect will be revealed. However, the charge release process after charge trapping affects the read-after-write operation and limits the operation speed, as shown in Fig. 1.

Up to date, the electron trapping and de-trapping dynamics have been extensively studied in n-channel FeFET (nFeFET) in the past through various experimental characterization tech-niques, including the ultra-fast *ID* − *VG* measurement [8], *Q*–*V* measurement [12], [13], [16], the extended measure-stress-measure characterization [17], and one-spot measure-ment adopted in this work [9]. The detrimental effects of

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Fig. 2. (a) TEM cross section of FeFETs. nFeFET and pFeFET difference   
only exists in the substrate. (b) Gate voltage waveform to measure the   
memory window in an FeFET. The write-to-measure time delay, TDelay,   
between the write pulse and measurement tunes the amount of sensed   
trapped charges.

Fig. 1. Charge trapping in FeFET is a serious challenge and not fully explored. This work aims to answer the listed three key questions using probing the charge trapping and de-trapping dynamics in both nFeFETs and pFeFETs.

electron trapping have been well-understood. However, a simi-lar understanding on hole trapping is not available. A few stud-ies have shown negligible hole trapping in nFeFETs [12], [13], but have not been cross validated using different characteriza-tion techniques and firmly established. Understanding of the asymmetry in electron and hole trapping is incomplete and preliminary so far.

Additionally, it is also unclear how much the memory window is reduced by charge trapping under different write conditions and whether charge trapping is fully recoverable. The required delay time for the trapped charge to fully release is also not clear, which directly affects the read throughput as a long delay time excludes immediate read-after-write. It is also known that charge trapping will be affected by the initial polarization state, which impacts the electric field distribution within the gate-stack, but this has not been verified experimentally.

To address those issues, in this work, we systematically investigate the charge trapping and de-trapping dynamics in both nFeFET and pFeFET. Through comparative study: 1) the advantages and shortcomings of nFeFET and pFeFET from the perspective of charge trapping will be identified; 2) the impact of electrons/holes acting as the majority or minority carriers on charge trapping will be clarified with the availability of both types of channels; and 3) new insights into charge trapping in FeFETs will be revealed. In the following, details on the devices under test, characterization methods, and modeling are shown in Section II. For completeness, results and discussions on electron trapping/de-trapping dynamics in nFeFET and pFeFET and hole trapping/de-trapping dynamics in pFeFET and nFeFET are discussed in Sections III-A–III-D, respectively. Section IV further discusses charge trapping/de-trapping in FeFETs, and finally Section V concludes the article.

II. EXPERIMENTAL DETAILS

base resistivity wafers. The process used the well-established Both nFeFETs and pFeFETs are fabricated on 1–10- · cm

CMOS process flow consisting of local oxidation of silicon (LOCOS) isolated FETs with ion implanted source and drain

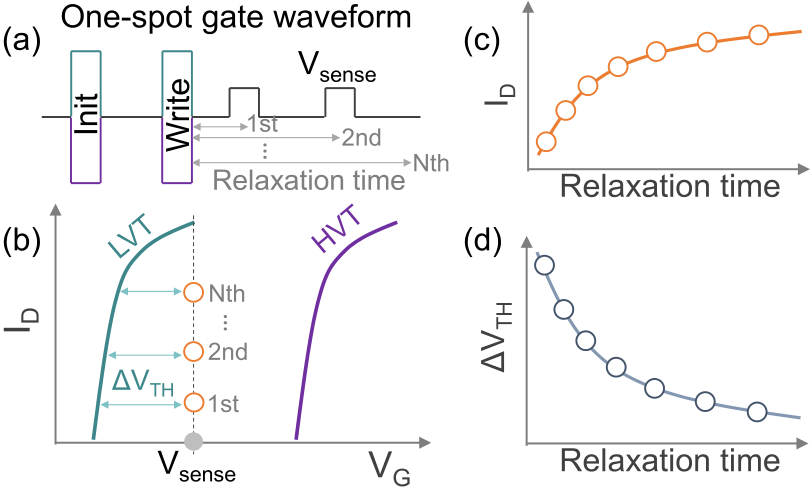




Fig. 3. One-spot measurement for charge trapping and de-trapping dynamics in FeFETs. (a) Applied gate waveform. (b) ID − VG character-istics for the low-VTH and high-VTH states and the ID values measured at different relaxation times. (c) ID and (d) extracted VTH shift (ΔVTH) as a function of relaxation time.

regions. Both the types of FeFETs feature a 10-nm-thick Zr-doped HfO2 (Hf0*.*5Zr0*.*5O2*)* as the ferroelectric thin film, 1.6-nm SiO2 native oxide as the interlayer, and 15-nm TiN as the gate electrode, as shown in Fig. 2(a). The stack is then treated with rapid thermal annealing at 500◦C for 30 s to induce ferroelectricity in HZO.

To unravel the charge trapping and de-trapping dynamics, the one-spot measurements, as shown in Fig. 3(a), are per-formed on both nFeFETs and pFeFETs [9]. In this work, irrespective of nFeFET or pFeFET, the state with *V*TH on the right is named as the high-*V*TH state (HVT) and that on the left as the low-*V*TH state (LVT). First, the devices are initialized into a pre-determined state with ±4-V, 1-*μ*s write pulses, and then a write pulse of a given pulse amplitude and pulsewidth is applied. Immediately after the write pulse, a series of probing pulses are applied at different relaxation times to probe the charge relaxation dynamics [18], [19]. *ID* measured at each probe pulse could be translated into the *V*TH shift to a reference *ID* − *VG* curve by assuming a parallel curve shift due to charge trapping, as shown in Fig. 3(b)–(d). Note that this assumption may yield inaccurate estimation of the *V*TH shift if the subthreshold slope changes due to interface trap generation, which, in that case, serves as an approximation. Repeating these measurements under different write conditions allows to map the full charge trapping and de-trapping dynamics.

For the study, the Keithley 4200 pulse measurement units are used for characterization. The probe pulse has a pulsewidth

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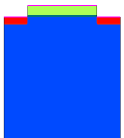
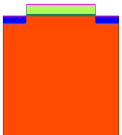
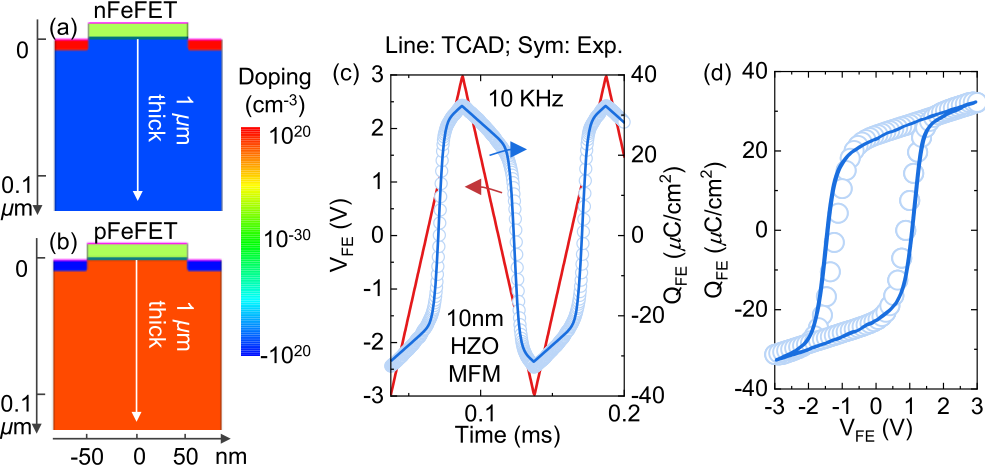
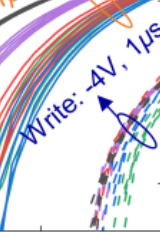
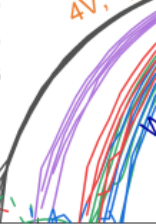
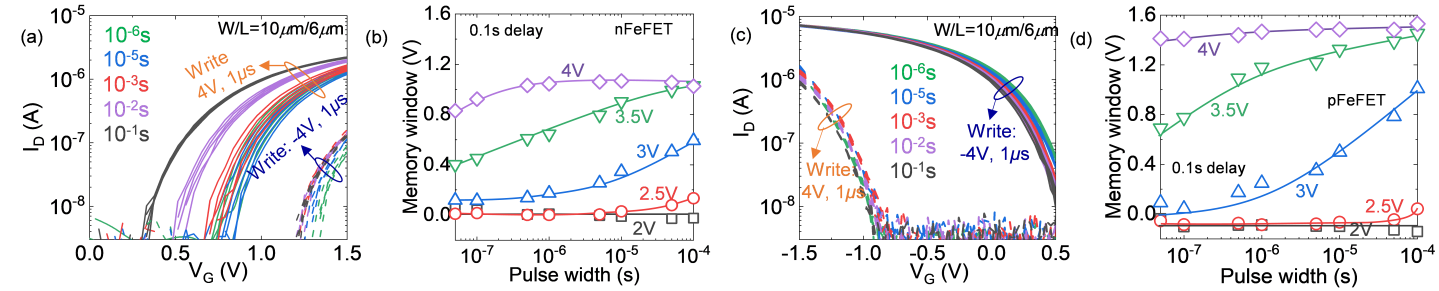


Fig. 4. measure delay. For each delay, five repeated cycles are shown. (b) Memory window in an nFeFET as a function of write pulsewidth for different Characteristics of nFeFET and pFeFET. (a) ID − VG characteristics in an nFeFET after ±4-V, 1-*µ*s write pulses under different write-to-pulse amplitudes. A 0.1-s write-to-measure delay is exerted to minimize the impact of charge trapping on FeFET characteristics. (c) Similar ID − VG characteristics measured in a pFeFET and (d) memory window switching dynamics in a pFeFET.

of 4 *μ*s, and pulse amplitudes [*V*sense shown on Fig. 3(a)] of   
1.4 V for nFeFET and −0.4 V for pFeFET are chosen based on device characteristics (shown in Fig. 4(a) and (c) for nFe-  
FET and pFeFET, respectively) for accurate *ID* measurement.   
Before the one-spot measurement, both nFeFETs and pFeFETs   
are fully woken up and exhibit a full memory window.

To provide a plausible explanation of the difference in the   
charge trapping behavior between nFeFETs and pFeFETs,   
a theoretical investigation will be performed in TCAD. The   
model, as shown in Fig. 5(a) and (b), is built with a

1-*μ*m-thick silicon substrate, a 1.6-nm SiO2 interlayer, and a 10-nm-thick HZO ferroelectric. For simulations, 1016cm−3 n-type and p-type Si substrates are assumed. The ferroelectric is described with the dynamic Preisach model, where the ferroelectric thin film is considered to be composed of multiple independent switching regions, and the model parameters are obtained from calibration with a 10-nm-thick HZO metal–ferroelectric–metal (MFM) capacitors [22]. Fig. 5(c) and (d) shows the TCAD dynamic Preisach model calibration with the measured *Q*FE dynamics, where excellent match can be obtained. Based on this setup, TCAD simulations similar to the experimental protocols will be performed and possible explanations will be analyzed.

III. RESULTS AND DISCUSSIONS

The *ID* −*VG* characteristics of nFeFETs and pFeFETs mea-sured after ±4-V, 1-*μ*s write pulses are shown in Fig. 4. For this measurement, the write-to-measure delay, as illustrated in the gate waveform shown in Fig. 2(b), is adjusted to modulate the amount of remaining trapped charges that will be sensed in measurement. For example, increasing the delay will leave more time for the trapped carriers to release. As a result, less trapped carriers will be sensed and the polarization switching effects will dominate. Note that this measurement only yields qualitative understanding about the impact of delay on FeFET characteristics, because the *ID*−*VG* measurement process itself lasts for 5 ms, which may disturb charge trapping and de-trapping given a relatively wide range of gate biases swept during measurement. The relative shift of *ID* − *VG* curves at different delay times qualitatively shows the impact of delay on the device characteristics.

As shown in Fig. 4(a), reducing the write-to-measure delay time from 0.1 s to 1 *μ*s increases *V*TH of the low-*V*TH state while has a negligible impact on the high-*V*TH state.

Fig. 5. TCAD models of (a) nFeFET and (b) pFeFET. The substrate has a thickness of 1 *µ*m. (c) Preisach model calibration with experimentally measured QFE transients on a 10-nm-thick Hf0.5Zr0.5O2 MFM capacitor. (d) QFE − VFE hysteresis loops with data from (c).

This is because the smaller delay leaves more electrons in the gate-stack, which increases *V*TH. Interestingly, with the−4-V, 1-*μ*s write pulse, negligible hole trapping is observed, confirming the asymmetry of electron and hole trapping in the nFeFET. Similar measurements on pFeFETs are shown in Fig. 4(c). It shows that the write-to-measure delay has a negligible impact on the *ID* − *VG* characteristics of pFeFETs under experimental write conditions. It indicates the possibility of immediate read-after-write in pFeFETs, better than its n-channel counterparts. However, in this work, to minimize the read-induced disturb, the fast one-spot measurement, rather than the slow *ID*−*VG* measurement, is adopted for quantitative evaluation.

The switching dynamics in nFeFETs and pFeFETs under different write pulse widths at various pulse amplitudes from 2 to 4 V are shown in Fig. 4(b) and (d), respectively. Both the types of FeFETs exhibit a high-speed operation (∼50 ns) and a large memory window (∼1 V) under 4-V write ampli-tude. It is interesting to see that pFeFETs exhibit a slightly better memory window and switching speed compared with nFeFETs. However, it is insufficient to conclude that pFeFETs fundamentally outperform nFeFETs as different trends where nFeFETs exhibit a better memory window than pFeFETs have been reported [13], [20], [21]. Therefore, in this work, this difference is probably related to device fabrications and needs more comprehensive investigations, which is beyond the scope of this work. With the device properties fully characterized, in the following, the charge trapping and de-trapping dynamics are studied.

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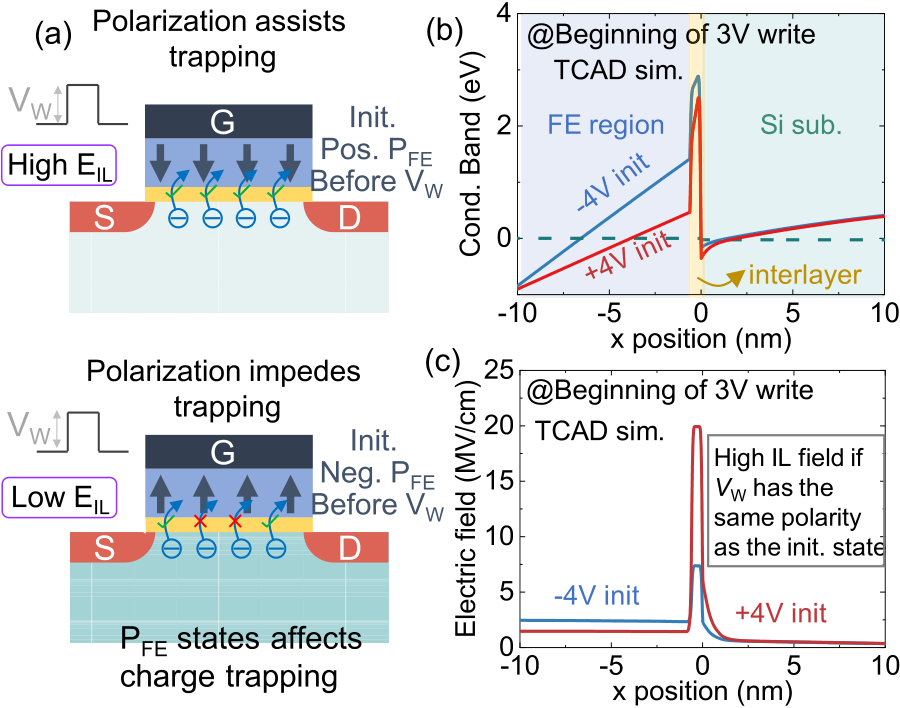


Fig. 6. (a) Under the same applied write pulse, different initial polarization states will facilitate or suppress charge trapping depending on whether the write pulse has a like or dislike polarity with initial polarization. Simulated (b) band diagram and (c) electrical field in nFeFET using TCAD tools at the beginning of 3-V write pulse under ±4-V initialization.

A. Electron Trapping and De-Trapping Dynamics in nFeFETs

The dependence of charge trapping on the initial polariza-tion states is first investigated. Due to charge continuity across the gate-stack, as shown in the following equation:   
 *P*FE + *ε*FE*E*FE = *ε*IL*E*IL (1)

where *P*FE is the polarization, and *ε*FE/*ε*IL and *E*FE/*E*IL are the dielectric constant and electric field in the ferroelec-tric/interlayer, respectively. The polarization will therefore determine the electric field in the interlayer and semiconductor, thus affecting the charge trapping dynamics.

As shown in Fig. 6(a), when applying a positive write pulse to FeFET, the interlayer electric field is strengthened by polarization pointing at the channel (e.g., considered as positive polarization in this work), which thus facilitates electron injection into the gate-stack. On the contrary, polar-ization pointing toward the gate (i.e., negative polarization) weakens the interlayer electric field, thus suppressing electron trapping. Similarly, under the negative write pulse, a negative polarization helps hole injection into HfO2, while a positive polarization suppresses hole injection. Therefore, if the write pulse has a like polarity as the initial polarization, charge injection will get enhanced.

Fig. 6(b) and (c) shows the band diagram and the electric field in an nFeFET at the beginning of a 3-V write pulse given two different initial states defined by ±4-V write pulses. The polarization is relaxed to be 1.3 *μ*C/cm2/−1.6 *μ*C/cm2after the +4-V/−4-V write pulse, respectively, for both nFeFET and pFeFET. It shows that the like initial state (i.e., +4 V initialization) has a much larger interlayer electric field than the opposite initial state (i.e., −4-V initialization), which will cause a higher charge injection in the case of like initial state. The high interlayer electric field, as also predicted in [9] and [23], due to the low interlayer dielectric constant and the polarization charge, poses significant challenges to FeFET

To verify this initial state dependence, electron trapping and de-trapping are first characterized in nFeFETs. Fig. 7(a) shows the real-time *V*TH after 1-*μ*s write pulses of different pulse amplitudes from 2 to 4 V with a step of 0.2 V, given the−4-V, 1-*μ*s initialization. *V*TH extraction is based on the LVT state *ID* − *VG* characteristics, as explained in Fig. 3(b). The results show that with pulse amplitudes from 2 to 2.8 V, the nFeFET remains in the HVT state defined by initialization. No polarization switching and charge trapping have been observed, consistent with Fig. 4(b). With the increase in the pulse amplitude, polarization starts to switch, and therefore *V*TH after a long relaxation time (e.g., 1 s) approaches the LVT state. However, the increased amplitudes also induce electron trapping as *V*TH immediately after the write pulse (e.g., 5-*μ*s relaxation time) is higher than the final stabilized *V*TH. The difference grows with the pulse amplitude, indicating a significant number of electrons trapped immediately after write and get released thereafter.

1-*μ*s initialization, as shown in Fig. 7(b), where the nFeFET Similar measurements are also performed for the +4-V,

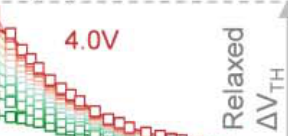
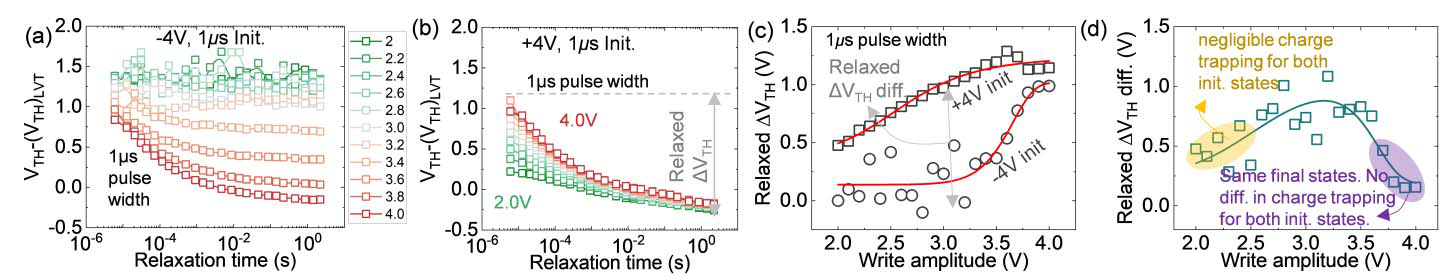
starts from the LVT state. With the increase in the pulse amplitudes, *V*TH immediately after write increases due to increased trapped electrons in the gate-stack, but the stabilized *V*TH converges, irrespective of the write pulse amplitudes as the nFeFET has already been in the LVT state and no polarization reversal is induced by the write pulses. Interestingly, electron release is observed even with 2-V write pulse, different from electric field, as explained in Fig. 6. In both Fig. 7(a) and (b), the −4-V initialization case. This is due to the higher interlayer *V*TH under 4-V write amplitude at 0.1-s relaxation time (i.e., same as the *ID* − *VG* measurement of the LVT state) is about 0.1 V lower than the LVT state *V*TH. This small difference, likely due to the different measurement time (i.e., 10 *μ*s per bias in *ID* − *VG* measurement, while 4 *μ*s in one-spot measurement) and FeFET cycle-to-cycle variation, does not affect the overall conclusion.

To quantitatively evaluate the dependence of charge trapping on the initial state, the relaxed*V*TH is defined to be the *V*TH difference at relaxation time immediately after write (e.g., 5-*μ*s relaxation time) and time where *V*TH stabilizes (e.g., 2-s relaxation time), as illustrated in Fig. 7(b). It reflects how much electrons are being released after memory write, also indicative of trapped electrons induced by the write pulses. Fig. 7(c) summarizes the relaxed*V*TH as a function of write pulse amplitudes at two different initial states. It clearly suggests more electron trapping induced by the write pulses at the like initial states.

Fig. 7(d) shows the difference in the relaxed*V*TH between the two initial states, as defined in Fig. 7(c). It exhibits an interesting peak around 3-V write amplitude. This is because at low amplitudes, not much electron trapping is induced anyway, so the difference in relaxed*V*TH is negligible. At high enough amplitude, polarization switching completes in a short time (*<*100 ns as shown in Fig. 4), much less than the write pulsewidth applied (i.e., 1 *μ*s), and therefore, the initial states are erased by the write pulses. As a result, similar amount of electrons gets trapped under write pulses with large pulse

reliability [9]. amplitudes, irrespective of the initial states.

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Fig. 7. Electron trapping and de-trapping in nFeFET. VTH versus relaxation time using the LVT state VTH as a reference at initial states defined by (a) −4-V, 1-*µ*s and (b) +4-V, 1-*µ*s write pulses. (c) Relaxed ΔVTH versus write pulse amplitude at different initial states. (d) Difference in relaxed ΔVTH between the two different initial states.

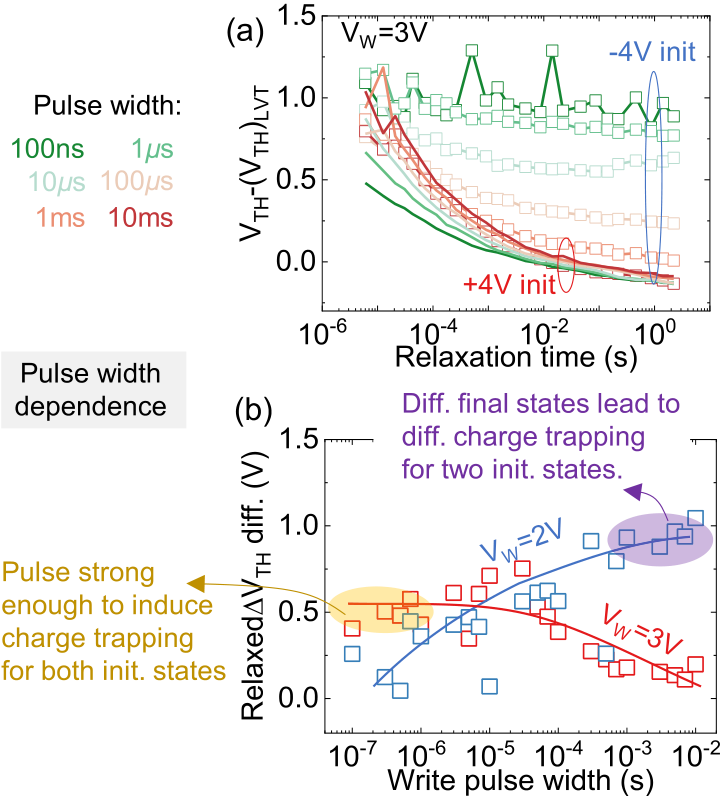


Fig. 8. (a) VTH versus relaxation time for different pulse widths at two different initial states. (b) Difference in relaxed ΔVTH between the two initial states for write pulse amplitudes of +2 and +3 V.

A similar dependence of charge trapping on the initial

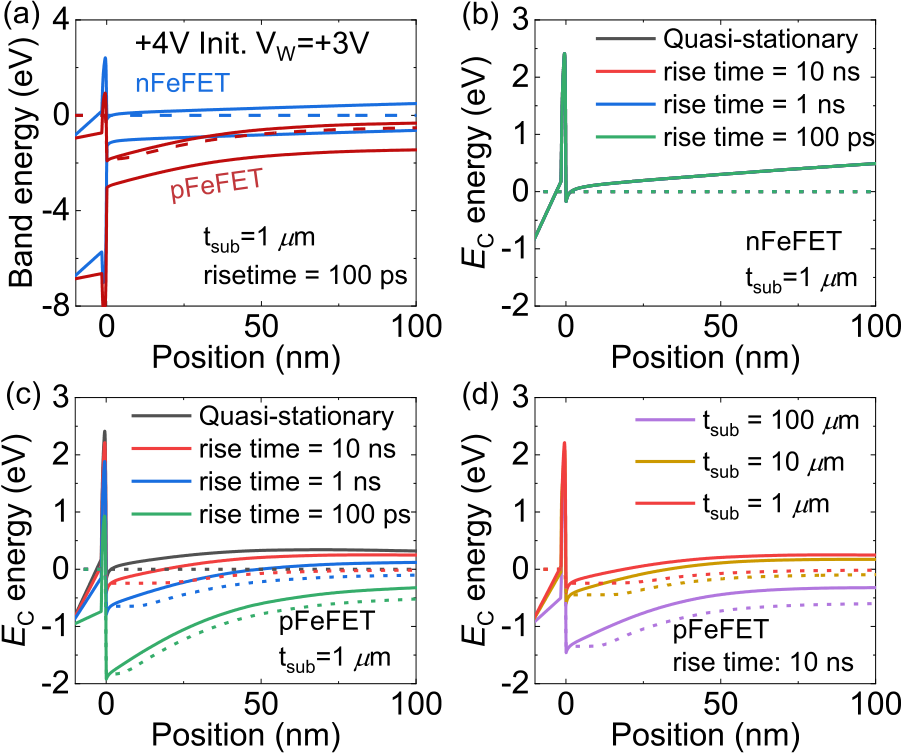


Fig. 9. (a) Simulated band diagram for nFeFET and pFeFET at the beginning of a 3-V write pulse after initialized by a 4-V memory write. Si substrate sits at x *>* 0, while the gate-stack sits at x *<* 0. Dashed lines are the electron quasi-Fermi level. Conduction band diagrams as a function of the rise time of the 3-V write pulse for (b) nFeFET and (c) pFeFET for a substrate thickness of 1 *µ*m. (d) Conduction band diagram at a fixed rise time of 10 ns for different substrate thicknesses.

states is observed for different write pulse widths, as shown   
in Fig. 8. Across a wide range of write pulse widths from

100 ns to 10 ms, more electrons get released under +4-V initialization than −4-V initialization, as shown in Fig. 8(a). For pulse widths below 1 *μ*s, negligible polarization switching and charge trapping are observed in nFeFETs when initialized with −4 V. However, electron trapping is present even with 100-ns pulsewidth when initialized with +4-V write. The difference in the relaxed*V*TH between the two initial states, as summarized in Fig. 8(b), shows a different trend for two write pulse amplitudes. For *V W* = 3 V, the initial states are wiped away at large write pulse widths (e.g., 10 ms) while still affecting the electron trapping at short pulse widths (e.g., 100 ns). For *V W* = 2 V, negligible electron trapping is induced at short pulse widths (e.g., 100 ns) and polarization switching is incomplete at large pulse widths (e.g., 10 ms). As a result, a different trend is observed for the two pulse amplitudes.

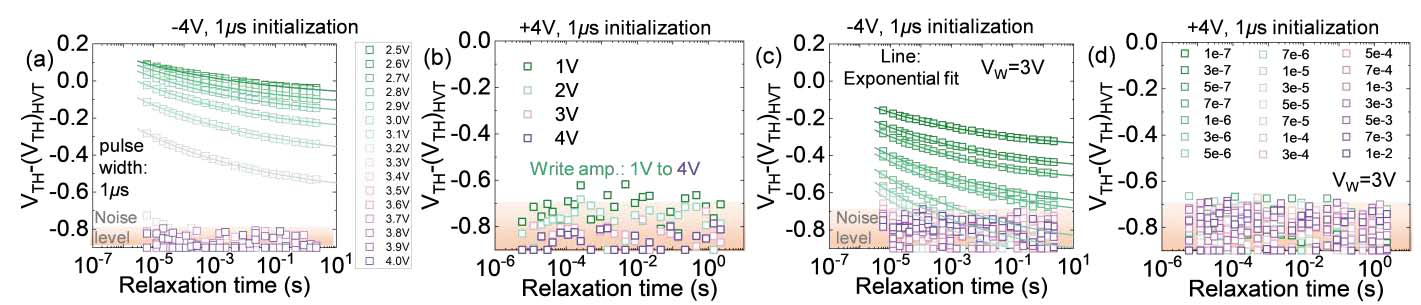
B. Electron Trapping and De-Trapping Dynamics in pFeFETs

In this section, electron trapping and de-trapping in pFeFETs are examined. First, to understand the relative amount of electron trapping in nFeFETs and pFeFETs, the

gate-stack electric field at the beginning of write pulses (e.g., 3-V write pulse) is simulated through TCAD. Fig. 9(a) shows the band diagrams at +4-V initialization. It shows that n-type silicon substrate (i.e., pFeFET) has a significant voltage drop compared with the p-type silicon substrate (i.e., nFeFET). As a result, the gate-stack electric field is much less in pFeFET compared with nFeFET, which will incur less amount of electron trapping in pFeFET.

Although the electric field in the gate-stack is the same for nFeFET and pFeFET in the steady state by comparing Fig. 9(b) and (c), it is different during the transient voltage ramp. For nFeFET, different rise time of a positive write pulse does not have the impact on the voltage drop in the gate-stack, as shown in Fig. 9(b). This is because of the small source/drain resistance, which can instantaneously provide the electrons. However, for pFeFET, the transient voltage ramp leaves the substrate in the non-steady state. Temporarily, a large voltage can drop across the n-type substrate when the electron supply cannot follow the fast voltage sweep, as shown in Fig. 9(c), similar to the resistor voltage drop in an *RC* circuit. In addition, for a slow write pulse sweep, as shown in Fig. 9(d), an increase in the substrate thickness, hence the

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Fig. 10. Electron trapping and de-trapping in pFeFET. VTH versus relaxation time for different write amplitudes at initial states defined by (a) −4-V, 1-*µ*s and (b) +4-V, 1-*µ*s write pulses. The HVT state VTH is used as a reference. (c) VTH versus relaxation time for different write pulse widths at initial states defined by (c) −4-V, 1-*µ*s and (d) +4-V, 1-*µ*s write pulses. (c) and (d) share the same legend.

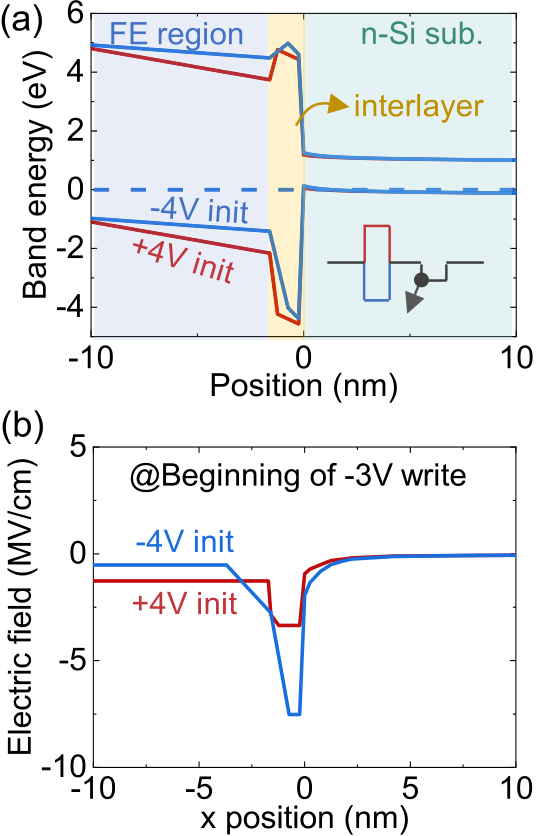


Fig. 11. Simulated (a) band diagram and (b) electrical field in pFeFET at the beginning of −3-V write pulse under ±4-V initialization.

substrate resistance, also leaves the substrate in the non-steady state and increases the substrate voltage drop. These results point out a possible difference between nFeFET and pFeFET in their transient response, which might cause different charge trapping and de-trapping response.

Fig. 10(a) and (b) shows the electron trapping and detrap-ping results at −4- and +4-V initialization, respectively. ization. This is because the sensed current from the one-spot Interestingly, no *V*TH relaxation is observed at +4-V initial-measurement is at noise floor [i.e., around a few nA as shown in Fig. 4(c)], and therefore, the extracted *V*TH is also purely noise. This indicates that the voltage shift induced by trapped electrons in pFeFET is less than 0.4 V, considering that the probe voltage is at −0.4 V and the pFeFET noise boundary is at −0.8 V for the LVT state, as shown in Fig. 4(c). This small amount of electron trapping has been observed for write pulse amplitudes ranging from 1 to 4 V, given that the pFeFETs start from the LVT state. This is much less compared with nFeFETs [i.e., about 1.2-V trapped electron-induced *V*TH shift at 4-V write pulse as shown in Fig. 7(c)] at the same initial states. As explained in Fig. 9, it is likely due to the much lower gate-stack electric field in pFeFET than nFeFET.

polarization switching and electron trapping shapes the For pFeFETs initialized with −4 V, the interplay between

dynamics of *V*TH, as shown in Fig. 10(a). Unlike the nFeFETs shown in Fig. 7(a) where *V*TH immediately after write remains close to the HVT state for different amplitudes, *V*TH in pFe-FETs closely follows polarization switching with increasing pulse amplitudes. *V*TH is completely within the noise level when write pulses larger than 3.8 V are applied, above which the pFeFET is written into the LVT state and the small *V*TH shift induced by trapped electrons (i.e., *<*0.4 V) will cause the measured current below the noise floor. Fig. 10(c) and (d) shows similar measurements but under different write pulse widths for both initializations. Similar behaviors are observed as in the pulse amplitude studies. These results suggest that in pFeFETs, immediate read-after-write is possible due to the small amount of trapped electrons.

It is worthwhile to note a possibility that the smaller amount of electron de-trapping sensed in pFeFET than nFeFET might be caused by different probe pulse amplitudes, i.e., 1.4 V in nFeFET and −0.4 V in pFeFET, where the negative probe pulse during sensing facilitates electron de-trapping. To rule out this possibility, charge relaxation in nFeFETs after 3-V write pulse at +4-V initialization is characterized with an interrupt pulse of −0.4 V, 4 *μ*s during relaxation. By comparing the case without interrupt pulse, it allows to evaluate the impact of the negative probing pulse on electron de-trapping. The results (not shown here) indeed show that the negative interrupt pulse reduces the amount of de-trapped electrons compared with the case without interrupt pulse, but the difference is less than 0.2 V. This small difference, however, does not change the conclusion that trapped electrons are much more in nFeFETs compared with pFeFETs.

C. Hole Trapping and De-Trapping Dynamics in pFeFETs

Hole trapping and de-trapping in pFeFETs are investigated in this section. Similar to nFeFETs discussed in Section III-A, hole trapping also exhibits initial state dependence. Fig. 11 shows the simulated band diagram and electric field vertically through the gate-stack of pFeFETs at the beginning of −3-V write pulse. It shows that the interlayer electric field is much higher for pFeFET initialized with −4 than +4 V. This is consistent with the charge conservation criteria shown in (1) as *P*FE in pFeFETs enhances/counteracts the electrical stress on the interlayer induced by the applied write voltage, when initialized with −4 V/+4 V, respectively. It again suggests that the interlayer electric field induced by the write pulses

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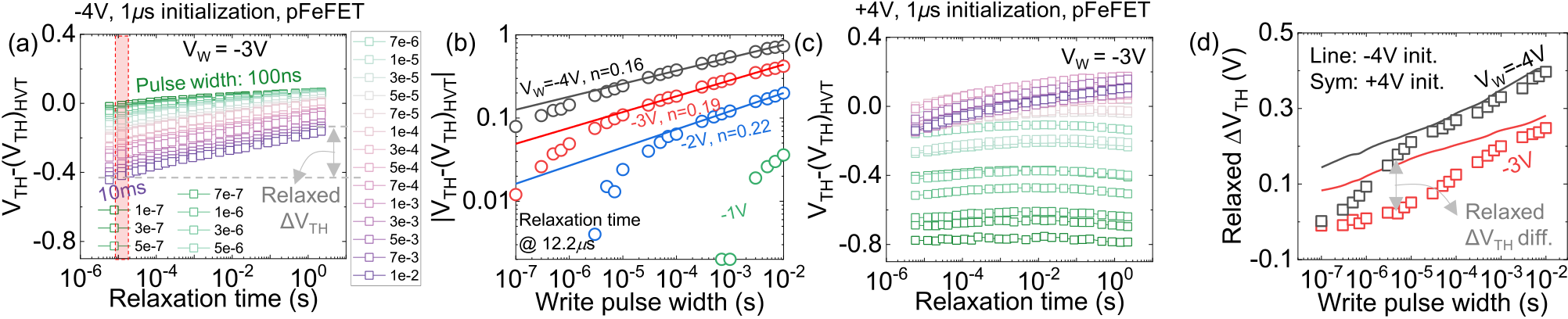


Fig. 12. 1 *µ*s. The HVT state VTH is used as a reference. (b) VTH shift extracted at 12.2-*µ*s relaxation time as a function of write pulse widths. (c) VTH versus Hole trapping and de-trapping in pFeFET. VTH versus relaxation time for different write pulse widths at initial states defined by (a) −4 V,

relaxation time for pFeFET initialized with +4-V, 1-*µ*s write pulses. (d) Relaxed VTH versus write pulse widths under two different initial conditions. (a) and (c) share the same legend.

(i.e., negative) is higher at the like initial states (i.e., −4 V). Therefore, hole trapping is expected to be more significant in pFeFETs initialized with −4 than +4 V. Fig. 12(a) and (c) shows the measured hole de-trapping dynamics in pFeFETs when initialized with −4 and +4 V, respectively. At −4-V initialization, the application of −3-V write pulse causes reduction in *V*TH, indicating hole trapping. The increase in write pulsewidth from 100 ns to 10 ms causes∼0.6-V *V*TH shift. Comparing this result with electron trapping in pFeFET shown in Fig. 10(d), hole trapping during negative write pulses is much more significant. Another interesting feature of the hole detrapping dynamics is the time scale involved, where the trapped holes are not fully released even after 2-s relaxation, much longer than electron de-trapping in nFeFETs, which lasts about 10 ms. This is likely related to the generation of interface trap during memory write with negative write pulses [19].

Fig. 12(b) shows the extracted absolute *V*TH shift at 12.2-*μ*s relaxation time as a function of write pulse widths under different pulse amplitudes. The obtained characteris-tics are similar to the hole trapping characteristics typically observed in negative bias temperature instability (NBTI) mea-surements, which is composed of initial trapping in preexisting defects and later generation of interface traps [19], [24].

At large write pulse amplitudes, for example, −4 V, the *V*TH shift, can be well fit with the relationship of

with the previous analysis on the initial state dependence of hole trapping, the relaxed*V*TH, defined in Fig. 12(a), is larger for the −4-V initialization compared with +4-V initialization, as shown in Fig. 12(d). These results suggest that pFeFET would suffer from hole trapping when stressed from write pulses with large pulsewidth and high pulse amplitude. Though for practical applications, the memory write does not require a long pulse [e.g., 50 ns at −4 V is good enough as shown in Fig. 4(d)], it will be interesting to evaluate whether repetitive write operation will cause accumulation of interface trap density and thus degrade pFeFET.

D. Hole Trapping and De-Trapping Dynamics in nFeFETs

When the silicon substrate changes from n-type in pFeFET to p-type in nFeFET, the amount of hole trapping induced during negative write pulses is significantly reduced, as will be shown in this section. Similar to the study in Fig. 9, the band diagram at the beginning of negative write pulse, *VW* = −3 V, is simulated and compared between nFeFET and pFeFET, when both are initialized with −4 V to have identical polarization, as shown in Fig. 13(a). Interestingly, for nFeFET, the voltage drop across the p-type substrate is significant while it is much smaller in pFeFET. The reason is that for pFeFET, the hole supply comes from source/drain doping, while in nFeFET, it comes from the p-type substrate.

*V*TH*(t)* = *Atn*  (2) As a result, this significant voltage drop in the silicon substrate

reduces the interlayer electric field in nFeFET, hence also hole

which is a linear curve on the log*V*–log(*t)* plot. The extracted trapping.

exponent, *n* = 0.16, is a key signature of interface defect generation [25], [26]. At lower pulse amplitudes, interface trap generation at short stress times becomes less likely and trapping at preexisting defects becomes dominant. With the limited range of write pulsewidth for fitting, the extracted exponent *n* increases slightly with reduced pulse amplitudes.

switching and charge trapping is observed. At short pulse When initialized at +4 V, interaction between polarization

widths (e.g., 100 ns), no polarization switching is observed, nor hole de-trapping. With the increase in pulsewidth up to 30 *μ*s, increased polarization switching is induced while no hole de-trapping exists (i.e., *V*TH is flat with respect to the relaxation time). When the pulsewidth further increases, *V*TH immediately after write actually decreases due to hole trapping and its de-trapping lasts for more than 1 s. Consistent

This is consistent with the experimental observation that hole trapping in nFeFET is much less than pFeFET. As shown in Fig. 13(b) and (c), hole de-trapping is constant with respect to the relaxation time, indicating no hole de-trapping after memory write. Hole trapping is only observable at large write pulse widths (e.g., 10 ms), where *V*TH of nFeFET is reduced compared with the short pulsewidth (e.g., 100 ns), as shown in Fig. 13(c). But this reduction is less than 0.2 V, compared with the 0.6-V reduction in pFeFET with the same initialization, as shown in Fig. 12(a). Fig. 13(d) summarizes *V*TH as a function of write pulsewidth under different initial conditions. *V*TH decrease is observed at large write pulse widths, irrespective of the initial conditions. When initialized at +4 V, the initial *V*TH increase is induced by polarization switching, so a turnaround behavior is present.

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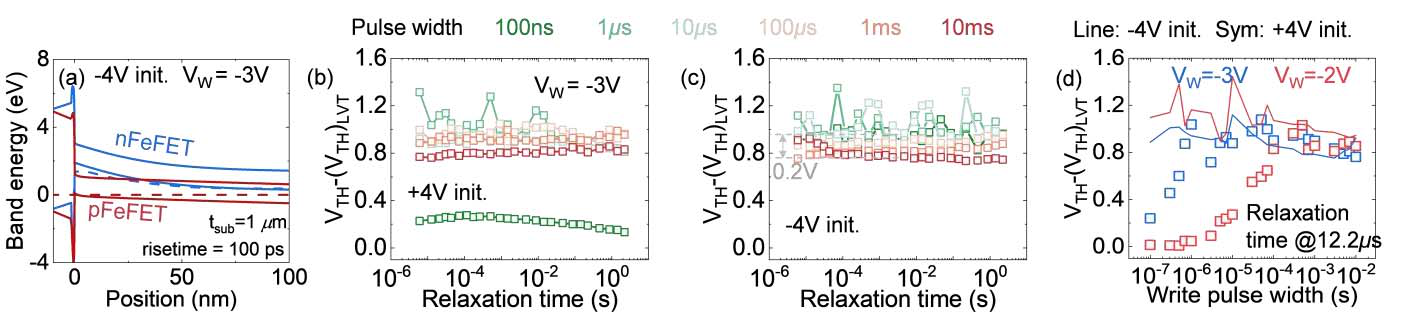


Fig. 13. Hole trapping and de-trapping in nFeFET. (a) Simulated valence band diagram in nFeFET and pFeFET at the beginning of −3-V write voltage when initialized with −4 V. VTH versus relaxation time for different write pulse widths at initial states defined by (b) +4 V, 1 *µ*s and (c) −4 V, 1 *µ*s. The LVT state VTH is used as a reference. (d) VTH shift extracted at 12.2-*µ*s relaxation time as a function of write pulse widths for pulse

amplitudes of −2 and −3 V.

IV. DISCUSSIONS

Note that all the numbers, including the amount of*V*TH, electron/hole de-trapping time constants, switching time, etc., presented in this work, are specific to the testing devices used and may not be reproducible for FeFETs made in different processes or different structures. However, based on this comprehensive set of characterization results, a full picture of electron and hole trapping and de-trapping during memory write operation can be made clear. Considering only a single memory write, several observations can be made. First, nFeFET generally suffers from significant electron trapping which can be fully recovered after around 10-ms delay, while almost immune to hole trapping unless a very long electrical stress is applied. In contrast, pFeFET could suffer significantly from hole trapping through interface defect generation during long negative write voltages, while benefits from reduced elec-tron trapping, though not completely immune, compared with nFeFET. This makes it possible for pFeFET to immediately read-after-write under normal write conditions (e.g., ±4 V, 100 ns), while it is challenging for nFeFET due to the necessity of delay for the electron to release.

The plausible proposed explanation for the difference in charge trapping/de-trapping behaviors between nFeFET and pFeFET is by no means exclusive. According to that expla-nation, it is the difference in the relative resistance between majority carrier supply and minority carrier supply that is responsible for the observed difference between nFeFET and pFeFET. Since these resistances are adjustable and can be engineered, the observed differences in our testing devices are not universal but should be typical as long as the devices have a small source/drain contact resistance. To verify that, similar measurements on complementary channel FeFETs fabricated with different processes would be required.

An interesting difference between electron trapping and hole trapping is that hole trapping is more related to perma-nent defect generation and not fully recoverable, unlike the electron trapping case. This could potentially cause concerns for repetitive write scenarios, e.g., endurance. Like the study of ac NBTI in pMOS logic transistors [25], the continual cycling of FeFETs will create a complex dynamics of interface defect generation during negative write pulse and possible passivation after negative write pulse when sitting idle or write with positive write pulses. It is necessary to perform similar charge trapping and de-trapping studies on FeFETs undergoing

endurance cycling and quantitatively evaluate whether the available ac NBTI models can explain the observed degra-dation, which will be explored in the future.

The initial state dependence study performed in this work, in addition to the insights provided into the charge trapping and de-trapping dynamics, also has practical implications. Though in reality the memory write is only necessary when the opposite state needs to be stored, the like state scenarios (e.g., applying a positive write pulse to an LVT state device) seem to be not applicable. However, this is not true. Considering a 1FeFET memory AND type array, for the array to function properly, inhibition bias schemes to manage the half-selected cells are absolutely necessary [27], [28]. For example, if the half-selected cells store LVT states and the target cell stores the HVT state and need to switch to LVT state, then in the *VW*/2 inhibition bias scheme, some half-selected cells experience half of the write voltage (e.g., 2 V) and induce electron trapping. Similarly, it is possible to generate interface defects when repetitive negative write pulse is applied in extreme cases.

From the results shown in this work, it can be seen that charge trapping is a serious issue during the operation of FeFETs. Ever since the discovery of ferroelectric HfO2 and its integration into FeFET, this challenge has been identified and novel device designs are actively pursued to alleviate this bottleneck [8]. Since charge trapping is related to the interlayer, strategies to reduce the interlayer electric field [9] or avoid the formation of the interlayer are effective approaches to manage charge trapping [6]. The former can be realized through adopting a higher dielectric constant interlayer [7] or separating the ferroelectric from the underlying transis-tor using a metal–ferroelectric–metal–insulator–semiconductor (MFMIS) structure [29]–[31]. The latter has been explored with the channel last integration where the ferroelectric HfO2 is deposited and crystallized first, and then the channel (e.g., low-temperature deposited poly-silicon or metal oxide thin films) is deposited at low temperature [6]. To evaluate the effectiveness of those new device designs, it is important to perform similar charge trapping and de-trapping analysis in the future.

V. CONCLUSION

In summary, this article unraveled the dynamics of charge trapping and de-trapping through extensive one-spot measure-ments in both nFeFETs and pFeFETs. Through comparative

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studies, it reveals that the like initial polarization states enhance charge injection due to strengthened interlayer electric field. We have shown a significant difference in the charge trapping and de-trapping behavior comparing nFeFETs and pFeFETs that nFeFETs suffer significantly from electron trap-ping while pFeFETs are less prone to electron trapping but show significant hole trapping and interface defects’ gen-eration when heavily stressed. We have provided a plausi-ble explanation for this asymmetry between nFeFETs and pFeFETs as a result of temporarily enhanced substrate voltage drop (i.e., smaller gate oxide voltage drop, thus less charge trapping) when screening charge comes from the substrate (i.e., hole trapping in nFeFETs is less than pFeFETs and electron trapping in pFeFETs is less than nFeFETs). These results provide a deeper understanding into charge trapping and de-trapping dynamics in FeFETs, which remains a major roadblock. This work could provide a reference of charge trapping to benchmark the new ferroelectric FET devices in the future.

REFERENCES

[1] A. I. Khan, A. Keshavarzi, and S. Datta, “The future of ferroelectric field-effect transistor technology,” *Nature Electron.*, vol. 3, no. 10, pp. 588–597, Oct. 2020, doi: [10.1038/s41928-020-00492-7](http://dx.doi.org/10.1038/s41928-020-00492-7).

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| [2] A. | Keshavarzi, | K. | Ni, | W. | Van | Den | Hoek, | | S. | Datta, | and |
| A. Raychowdhury, | | “Ferroelectronics | | | | for | edge | intelligence,” | | | *IEEE* |

*Micro*, vol. 40, no. 6, pp. 33–48, Nov./Dec. 2020, doi: [10.1109/MM. 2020.3026667](http://dx.doi.org/10.1109/MM.2020.3026667).

[3] T. Mikolajick, U. Schroeder, and S. Slesazeck, “The past, the memories,” *IEEE Trans.* present, and the future of ferroelectric   
 *Electron Devices*, vol. 67, no. 4, pp. 1434–1443, Apr. 2020, doi: [10.1109/TED.2020.2976148](http://dx.doi.org/10.1109/TED.2020.2976148).

[4] S. Dunkel *et al.*, “A FeFET based super-low-power ultra-fast embed-ded NVM technology for 22 nm FDSOI and beyond,” in *IEDM Tech. Dig.*, Dec. 2017, pp. 19.7.1–19.7.4, doi: [10.1109/IEDM.2017. 8268425](http://dx.doi.org/10.1109/IEDM.2017.8268425).

[5] S. Beyer *et al.*, “FeFET: A versatile CMOS compatible device with game-changing potential,” in *Proc. IEEE Int. Memory Workshop (IMW)*, May 2020, pp. 1–4, doi: [10.1109/IMW48823.2020.9108150](http://dx.doi.org/10.1109/IMW48823.2020.9108150).

[6] A. A. Sharma *et al.*, “High speed memory operation in channel-last, back-gated ferroelectric transistors,” in *IEDM Tech. Dig.*, Dec. 2020, pp. 391–394, doi: [10.1109/IEDM13553.2020.9371940](http://dx.doi.org/10.1109/IEDM13553.2020.9371940).

[7] A. J. Tan *et al.*, “Ferroelectric HfO2 memory transistors with high-*κ* interfacial layer and write endurance exceeding 1010cycles,” *IEEE Electron Device Lett.*, vol. 42, no. 7, pp. 994–997, Jul. 2021, doi: [10.1109/LED.2021.3083219](http://dx.doi.org/10.1109/LED.2021.3083219).

HfO2-based [8] E. Yurchuk *et*  *al.*, “Charge-trapping phenomena in   
 FeFET-type nonvolatile memories,” *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3501–3507, Sep. 2016, doi: [10.1109/TED.2016.](http://dx.doi.org/10.1109/TED.2016.2588439)  [2588439](http://dx.doi.org/10.1109/TED.2016.2588439).

[9] K. Ni *et al.*, “Critical role of interlayer in Hf0*.*5Zr0*.*5O2 ferroelec-tric FET nonvolatile memory performance,” *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2461–2469, Jun. 2018, doi: [10.1109/TED. 2018.2829122](http://dx.doi.org/10.1109/TED.2018.2829122).

[10] M. Pesic, A. Padovani, S. Slcsazeck, T. Mikolajick, and L. Larcher,

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| “Deconvoluting | charge | trapping | and | nucleation | interplay | in |

FeFETs: Kinetics and reliability,” in *IEDM Tech. Dig.*, Dec. 2018, pp. 25.1.1–25.1.4, doi: [10.1109/IEDM.2018.8614492](http://dx.doi.org/10.1109/IEDM.2018.8614492).

[11] N. Gong and T.-P. Ma, “A study of endurance issues in HfO2-based ferroelectric field effect transistors: Charge trapping and trap generation,”*IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 15–18, Jan. 2018, doi: [10.1109/LED.2017.2776263](http://dx.doi.org/10.1109/LED.2017.2776263).

[12] K. Toprasertpong, M. Takenaka, and S. Takagi, “Direct observation of interface charge behaviors in FeFET by quasi-static split C-V and Hall techniques: Revealing FeFET operation,” in *IEDM Tech.*

*Dig.*, Dec. 2019, pp. 23.7.1–23.7.4, doi: [10.1109/IEDM19573.2019. 8993664](http://dx.doi.org/10.1109/IEDM19573.2019.8993664).

[13] K. Toprasertpong, Z. Y. Lin, T. E. Lee, M. Takenaka, and S. Takagi, “Asymmetric polarization response of electrons and holes in Si FeFETs: Demonstration of absolute polarization hysteresis loop and inversion hole density over 2 × 1013 cm−2,” in *Dig. Tech. Papers Symp. VLSI Technol.*, Jun. 2020, pp. 1–2, doi: [10.1109/](http://dx.doi.org/10.1109/VLSITechnology18217.2020.9265015)  [VLSITechnology18217.2020.9265015](http://dx.doi.org/10.1109/VLSITechnology18217.2020.9265015).

[14] S. Deng *et al.*, “Examination of the interplay between polarization switching and charge trapping in ferroelectric FET,” in *IEDM Tech. Dig.*, Dec. 2020, pp. 4.4.1–4.4.4, doi: [10.1109/IEDM13553.2020.9371999](http://dx.doi.org/10.1109/IEDM13553.2020.9371999).

[15] R. A. Izmailov, J. W. Strand, L. Larcher, B. J. O’Sullivan, A. L. Shluger, and V. V. Afanas’ev, “Electron trapping in ferroelectric HfO2,” *Phys. Rev. Mater.*, vol. 5, no. 3, Mar. 2021, Art. no. 034415, doi: [10.1103/PhysRevMaterials.5.034415](http://dx.doi.org/10.1103/PhysRevMaterials.5.034415).

[16] K. Toprasertpong, K. Tahara, M. Takenaka, and S. Takagi, “Evaluation of polarization characteristics in metal/ferroelectric/semiconductor capaci-tors and ferroelectric field-effect transistors,” *Appl. Phys. Lett.*, vol. 116, no. 24, Jun. 2020, Art. no. 242903, doi: [10.1063/5.0008060](http://dx.doi.org/10.1063/5.0008060).

[17] B. J. O’Sullivan *et al.*, “Defect profiling in FEFET Si:HfO2 layers,”*Appl. Phys. Lett.*, vol. 117, no. 20, Nov. 2020, Art. no. 203504, doi: [10.1063/5.0029072](http://dx.doi.org/10.1063/5.0029072).

[18] B. Kaczer, V. Arkbipov, R. Degraeve, N. Collaert, G. Groeseneken, and M. Goodwin, “Disorder-controlled-kinetics model for negative bias temperature instability and its experimental verification,” in *Proc.*

*IEEE Int. Rel. Phys. Symp.*, Apr. 2005, pp. 381–387, doi: [10.1109/ relphy.2005.1493117](http://dx.doi.org/10.1109/relphy.2005.1493117).

[19] S. Mahapatra, *Fundamentals of Bias Temperature Instability in MOS*  *Transistors*. New Delhi, India: Springer, 2016.

[20] M. Lederer *et*  *al.*, “Integration of hafnium oxide on epitax- ial SiGe for p-type ferroelectric FET application,” *IEEE Electron*  *Device*  *Lett.*, vol. 41, no. 12, pp. 1762–1765, Dec. 2020, doi: [10.1109/LED.2020.3031308](http://dx.doi.org/10.1109/LED.2020.3031308).

[21] H.-K. Peng, T.-H. Kao, Y.-C. Kao, P.-J. Wu, and Y.-H. Wu, “Reduced asymmetric memory window between Si-based n- and p-FeFETs with scaled ferroelectric HfZrO*x* and AlON interfacial layer,” *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 835–838, Jun. 2021, doi: [10.1109/LED.2021.3074434](http://dx.doi.org/10.1109/LED.2021.3074434).

[22] K. Ni, M. Jerry, J. A. Smith, and S. Datta, “A circuit compatible accurate compact model for ferroelectric-FETs,” in *Dig. Tech. Papers Symp. VLSI*  *Technol.*, Jun. 2018, pp. 131–132, doi: [10.1109/VLSIT.2018.8510622](http://dx.doi.org/10.1109/VLSIT.2018.8510622). [23] X. Wang *et*  *al.*, “Impact of charges at Ferroelectric/interlayer interface on depolarization field of ferroelectric FET with metal/ferroelectric/interlayer/Si gate-stack,” *IEEE*  *Trans.*  *Electron*  *Devices*, vol. 67, no. 10, pp. 4500–4506, Oct. 2020, doi: [10.1109/TED.](http://dx.doi.org/10.1109/TED.2020.3017569)  [2020.3017569](http://dx.doi.org/10.1109/TED.2020.3017569).

[24] A. E. Islam, H. Kufluoglu, D. Varghese, S. Mahapatra, and M. A. Alam,“Recent issues in negative-bias temperature instability: Initial degra-dation, field dependence of interface trap generation, hole trapping effects, and relaxation,” *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2143–2154, Sep. 2007, doi: [10.1109/TED.2007.902883](http://dx.doi.org/10.1109/TED.2007.902883).

[25] S. Mahapatra *et al.*, “A comparative study of different physics-based NBTI models,” *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 901–916, Mar. 2013, doi: [10.1109/TED.2013.2238237](http://dx.doi.org/10.1109/TED.2013.2238237).

[26] M. A. Alam and S. Mahapatra, “A comprehensive model of PMOS NBTI degradation,” *Microelectron. Rel.*, vol. 45, no. 1, pp. 71–81, Jan. 2005, doi: [10.1016/j.microrel.2004.03.019](http://dx.doi.org/10.1016/j.microrel.2004.03.019).

[27] J. Müller *et al.*, “Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories,” in *IEDM Tech. Dig.*, Dec. 2013, pp. 10.8.1–10.8.4, doi: [10.1109/IEDM. 2013.6724605](http://dx.doi.org/10.1109/IEDM.2013.6724605).

[28] K. Ni, X. Li, J. A. Smith, M. Jerry, and S. Datta, “Write disturb in ferroelectric FETs and its implication for 1T-FeFET AND memory arrays,” *IEEE Electron Device Lett.*, vol. 39, no. 11, pp. 1656–1659, Nov. 2018, doi: [10.1109/LED.2018.2872347](http://dx.doi.org/10.1109/LED.2018.2872347).

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| [29] J. Müller *et al.*, “High endurance strategies | | | | | | for hafnium oxide | | |
| based | ferroelectric | field | effect | transistor,” | in | *Proc.* | *16th* | *Non-* |

*Volatile Memory Technol. Symp. (NVMTS)*, Oct. 2016, pp. 1–7, doi: [10.1109/NVMTS.2016.7781517](http://dx.doi.org/10.1109/NVMTS.2016.7781517).

[30] K. Ni *et al.*, “SoC logic compatible multi-bit FeMFET weight cell for neuromorphic applications,” in *IEDM Tech. Dig.*, Dec. 2018, pp. 13.2.1–13.2.4, doi: [10.1109/IEDM.2018.8614496](http://dx.doi.org/10.1109/IEDM.2018.8614496).

[31] C. Sun *et al.*, “First demonstration of BEOL-compatible ferroelectric TCAM featuring a-IGZO Fe-TFTs with large memory window of 2.9 V, scaled channel length of 40 nm, and high endurance of 108 cycles,” in *Dig. Tech. Papers Symp. VLSI Technol.*, 2021, pp. 1–2.

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