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ZrO2 Ferroelectric FET for Non-volatile Memory Application

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***Abstract— We***  ***demonstrate***  ***for***  ***the***  ***first***  ***time***  ***ZrO2***   
***ferroelectric field-effect transistors (FeFETs) for embedded***   
***non-volatile memory applications. Multiple sweeps of polar-***  
***ization versus voltage measurement demonstrate that a***   
***metal/ZrO2/Ge capacitor is entirely free of wake-up effect***   
***and has significantly improved fatigue characteristics com-***  
***pared to a HfZrOx control device. Thanks to relatively small***   
***remnant polarization and a high-quality ZrO2 /Ge interface,***   
***up to 107cycles program/erase endurance, 10 ns pro-***  
***gram/erase speed, and >10-year data retention at 85 °C are***   
***achieved.***

***Index Terms— Anti-ferroelectric, ferroelectric, ferroelec-***  
***tric field-effect transistor (FeFET), ZrO*2*.***

I. INTRODUCTION   
**H** HfZrO*x*, Si:HfO2*)* are of growing interest for embedded AFNIUM-BASED ferroelectric (FE) materials (*e.g.*

non-volatile memory (NVM) applications [1]–[5]. These mate-rials have been incorporated into FinFET [2] and FDSOI field-effect transistor (FET) [5] devices, to achieve program/erase (P/E) speed as fast as 10 ns. Some technological challenges for FeFETs remain, however: (1) non-stoichiometry of HfO*x* and its poor semiconductor interface quality, leading to reliability issues such as wake-up [6], imprint [7], [8], and fatigue effects[9]; (2) relatively high remnant polarization (*P*r, usually

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Fig. 1. (a) Key process steps for fabricating a ZrO2 FeFET. (b) Schematic cross-section of ZrO2 FeFET. (c) HRTEM images of fabricated ZrO2 FeFET gate stacks showing ZrO2 thicknesses of 4.2 nm. (d) EDS scans along AA’ in (c).

in the range of several *μ*C/cm2to 30 *μ*C/cm2[10]–[13]), causing strong depolarization and hence degraded endurance and retention [14], [15].

Recently, anti-ferroelectric (AFE) materials (*e.g.*, ZrO2*)* were proposed as an alternative, due to their potentially higher endurance and ease of process integration as compared with FE materials [16]. Unlike the hysteretic polarization (*P) vs.* voltage (*V )* loop for FE materials, an ideal AFE material has a “pinched” hysteresis characteristic with zero *P*r, explained by *Landau-Ginzburg-Devonshire* (LGD) theory [17], and hence was presumed to be unsuitable for NVM applications. However, Peši´c *et al.* [8], [16] reported that by using asymmet-ric work functions of the top and bottom electrodes to induce a built-in electric field in the AFE layer, a non-zero *P*r can be achieved. Another way of achieving ZrO2 FE is to introduce compressive strain in the film [18], for instance via depositing ZrO2 on Ge(100) [19]. In this work, we demonstrate for the first time ZrO2 FeFETs suitable for NVM application.

II. DEVICE FABRICATION

Fig. 1(a) shows the key process steps for fabricating ZrO2 FeFETs on 4-inch Ge (100) wafer substrates with a bulk resistivity of 0.088-0.14 · cm. After several cycles of chem-ical cleaning in dilute H2O:HF (50:1) solution and rinsing in deionized (DI) water, the wafer was loaded into an atomic layer deposition chamber to form the 4.2 nm ZrO2 gate dielectric layer. The ZrO2 deposition was performed at 250◦C. The precursors of Zr, Al, and O are Zr[N(CH3*)*2]4, Al(CH3*)*3, and H2O, respectively. Subsequently, a 100 nm-thick TaN

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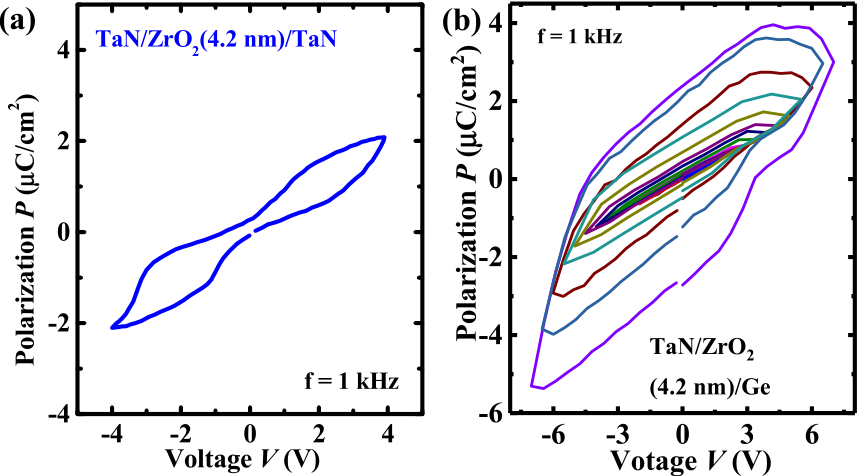


Fig. 2. (a) Measured P-V curve of a TaN/ZrO2/TaN capacitor. (b) Measured minor P-V loops of a TaN/ZrO2/Ge capacitor.

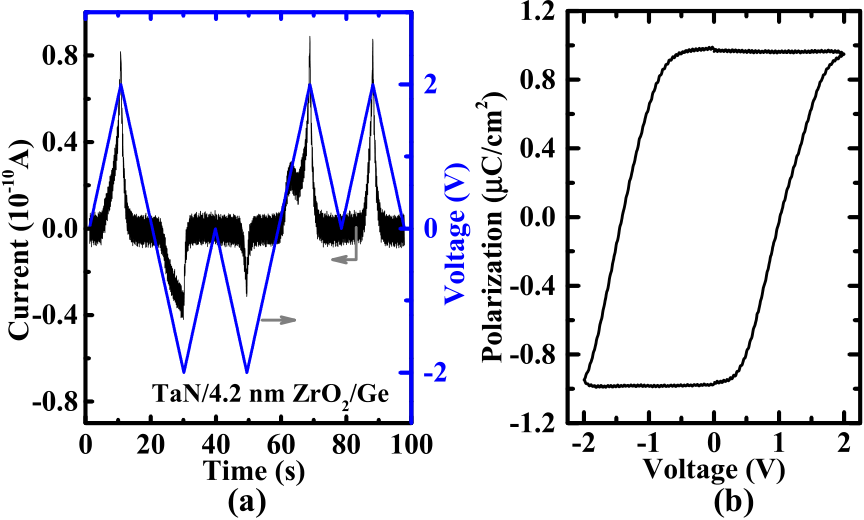


Fig. 3. (a) PUND measurement and (b) extracted polarization charge vs. voltage curve on a TaN/ZrO2/Ge gate stack.

gate layer was deposited by reactive sputtering. After gate patterning via lithography and etch processes, source and drain (S/D) regions were doped by BF+ 2implantation at an energy of 30 keV and a dose of 1 × 1015cm−2. 20 nm-thick Nickel S/D metal electrodes were then formed by a lift-off process. Finally, dopant activation was achieved with a rapid thermal anneal (RTA) at 500◦C for 30 s. TaN/ZrO2/TaN and TaN/HfZrO*x*/Al2O3/Ge FeFET control devices were also fabricated.

A cross-sectional schematic of the ZrO2 FeFET is shown in Fig. 1(b). Fig. 1(c) shows high-resolution transmission electron microscope (HRTEM) image of the gate stack of the fabricated transistor with ZrO2 thicknesses of 4.2 nm. Energy dispersive spectroscopy (EDS) analysis results for Ge, Zr, Hf, O, and Ta profiles along the *AA*’ line in Fig. 1(c) are shown in Fig. 1(d).

III. RESULTS AND DISCUSSION

Fig. 2(a) shows the polarization (*P) vs.* voltage (*V)* curve for a TaN/ZrO2/TaN capacitor, which exhibits AFE behavior with an evident double-loop hysteresis and a remnant polar-ization (*P*r*)* of approximately zero. Fig. 2(b) shows measured minor *P-V* loops of a TaN/ZrO2/Ge device, demonstrating ferroelectric-like characteristics with non-zero *P*r less than 2 *μ*C/cm2. This *P*r value is relatively small as compared to that of reported FE devices [1], which could potentially improve memory retention and P/E endurance (due to weaker depo-larization field) while maintaining a sufficiently large mem-ory window (MW) for sensing. Positive-up, negative-down (PUND) pulsed measurements were used to extract the true polarization (*P)* of the TaN/ZrO2/Ge gate stacks, by isolating the impact of non-switching charge, as shown in Fig. 3.

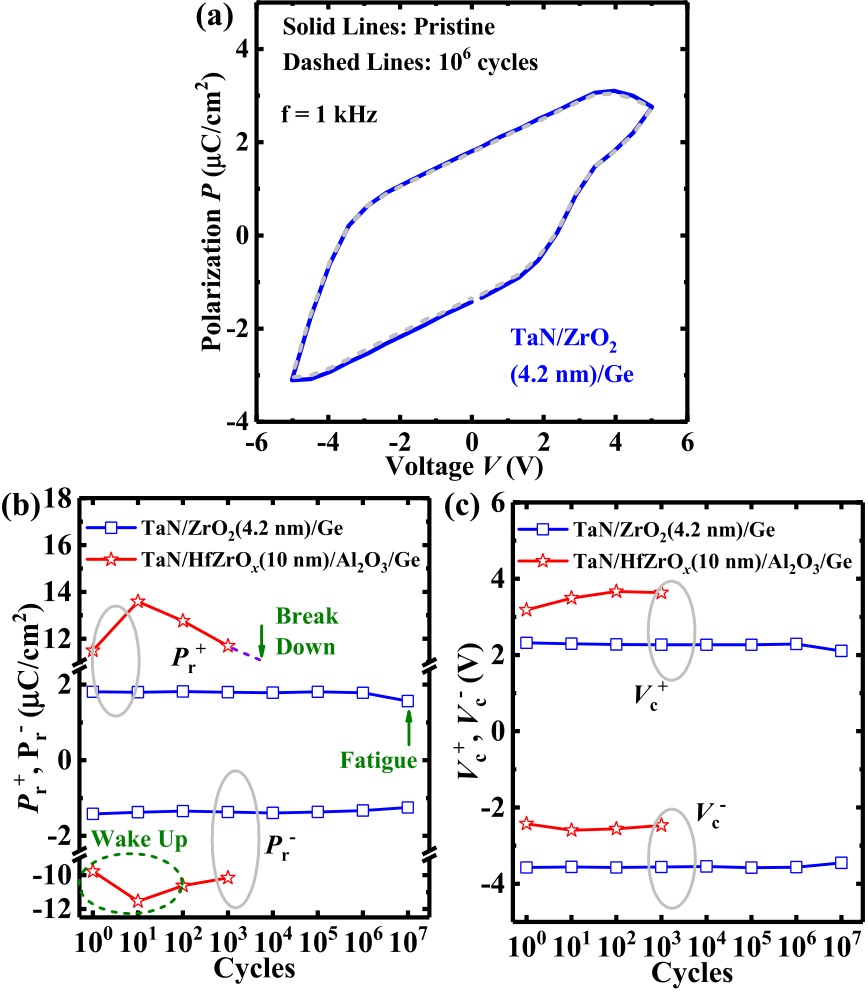


Fig. 4. (a) Measured P-V curves of another TaN/ZrO2/Ge device during 107sweeping cycles. (b) Pr and (c) Vc vs. number of DC sweeping cycles for ZrO2 capacitors and a HfZrOx device. No wake-up or imprint effects are observed for ZrO2. In contrast, HfZrOx exhibits the obvious wake-up effect. TaN/ZrO2/Ge MOS capacitor achieves the significantly reduced fatigue compared to the HfZrOx control device.

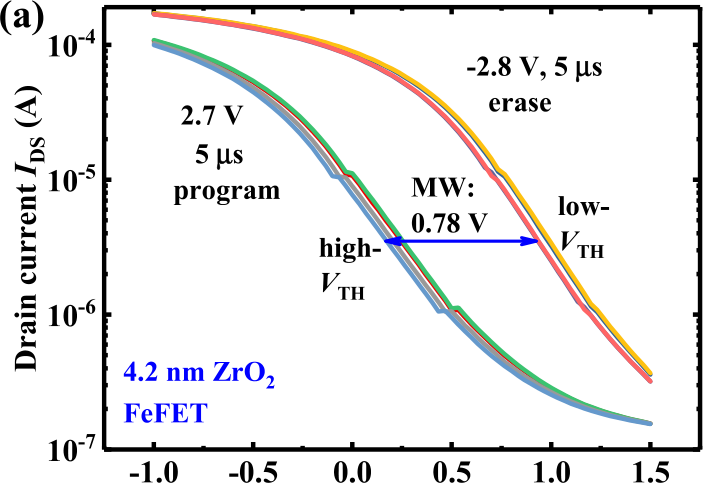
Peši´c *et al.* [8], [16], [21], [22] established a theory to explain the FE-like behavior of ZrO2 sandwiched between electrodes with asymmetric work functions. By applying the first-order reversal curve (FORC) method, the shift of switch-ing density for an AFE layer was found to lead to a centered single distribution corresponding to FE behavior. However, in this work, *Pr* and the coercive voltage (*V*c*)* are substantially enhanced for the TaN/ZrO2/Ge capacitor compared to the TaN/ZrO2/TaN capacitor. In addition, the second *P-V* loop was not observed with increasing sweeping voltage range until the breakdown of the gate stack, as shown in Fig. 2(b). Another possible explanation for the FE behavior observed in this work is that the orthorhombic (Pca21*)* phase formed in ZrO2. Experiments have shown that tetragonal (P42/nmc) and orthorhombic (Pca21*)* phases contribute to AFE and FE behav-ior, respectively, in HfZrO composites [18], [20]. It is known that compressive strain can be induced in crystalline ZrO2 on Ge (100) substrate due to the ∼10% lattice mismatch [19], and *ab-initio* calculations indicate that the FE structure is favored in compressively strained ZrO2 [18].

Fig. 4(a) shows the measured *P vs*. *V* curves for another TaN/ZrO2/Ge MOS capacitor over 107sweeping cycles mea-sured at 1 kHz. (The measurement was stopped after 107 cycles due to the measurement time limit.) Figs. 4(b) and (c) show the extracted evolution of the positive and negative*P*r and *V*c values, respectively, over 107DC sweeping cycles for the TaN/ZrO2/Ge capacitor as well as for the HfZrO*x* control device that clearly exhibits wake-up and fatigue effects, which are long-standing issues for doped HfO2 based memory devices. No wake-up or imprint are observed for the ZrO2 FE capacitor; the fatigue effect appears at 107cycles, which is significantly improved compared to the HfZrO*x* control device.

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LIU et al.: ZrO**2** FERROELECTRIC FET FOR NON-VOLATILE MEMORY APPLICATION 1421





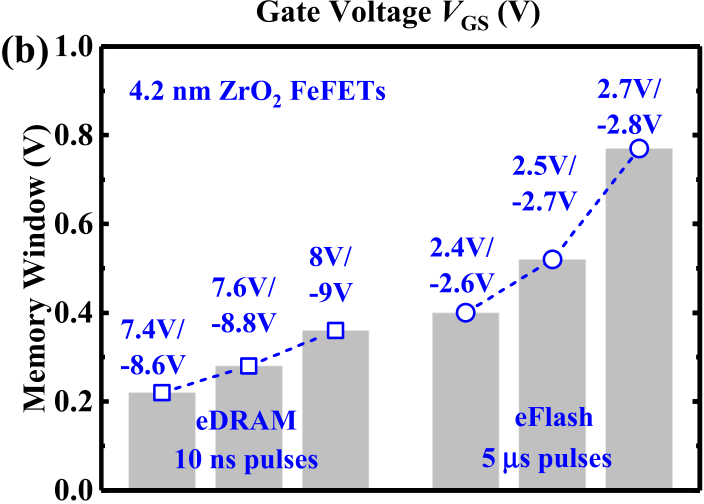


Fig. 5. (a) Measured IDS-VGS curves of a 4.2 nm-thick ZrO2 FeFET for the two polarization states. (VDS = 0.05 V.) VTH is defined as VGS at 100 nA·W/L, and memory window (MW) is the *Δ*VTH between two states. (b) Extracted MW under different P/E conditions for the device.

Program (erase) operation is achieved by applying positive (negative) voltage pulses to the gate of a ZrO2 FeFET, to raise (lower) its threshold voltage (*V*TH*)*. Fig. 5(a) shows how the linear-region transfer characteristics of the fabricated FeFET shift over 100 P/E cycles, measured with 2.7 V program and−2.8 V erase voltages with 5 *μ*s pulse width. *V*TH is defined as *V*GS at 100 nA·W/L, and MW is defined as the maxi-mum change in *V*TH. Although TaN/ZrO2/Ge exhibits a much smaller *P*r compared to reported doped HfO2 devices [1], the FeFET achieves an obvious MW. This is consistent with the simulation results in [15]. The dependence of the MW of the device on P/E pulse conditions is plotted in Fig. 5(b). For embedded NVM applications, a 0.78 V MW can be achieved using 2.7 V program and −2.8 V erase voltages with 5 *μ*s pulse width. For replacing embedded DRAM, program and erase speed as fast as 10 ns can be achieved using 7.4 V program and −8.6 V erase voltages, with a MW larger than 0.2 V. For a 10 ns pulse voltage above 8 V, the gate leakage current is still below 10−4A/cm2. Operation below 3 V is possible for a *μ*s pulse width, but larger program/erase voltages are required for a 10 ns pulse width.

To investigate device endurance, alternating program and erase pulses were applied to the fabricated devices. Fig. 6(a) plots MW *vs.* cycle number for various P/E pulse conditions, showing that a large MW can be maintained without significant degradation over many P/E cycles for both 4.2 nm-thick ZrO2 FeFET. Fig. 6(b) shows the results of data retention testing of the 4.2 nm-thick ZrO2 FeFET, performed at room temperature as well as at elevated temperature (85◦C). Negligible MW degradation is observed after 104s. A MW of 0.4 V is extrap-olated to be maintained over 10 years at 25◦C and at 85◦C. This retention behavior of the ZrO2 FeFET is comparable to that of the best-reported retention properties for HfO2-based FeFETs.

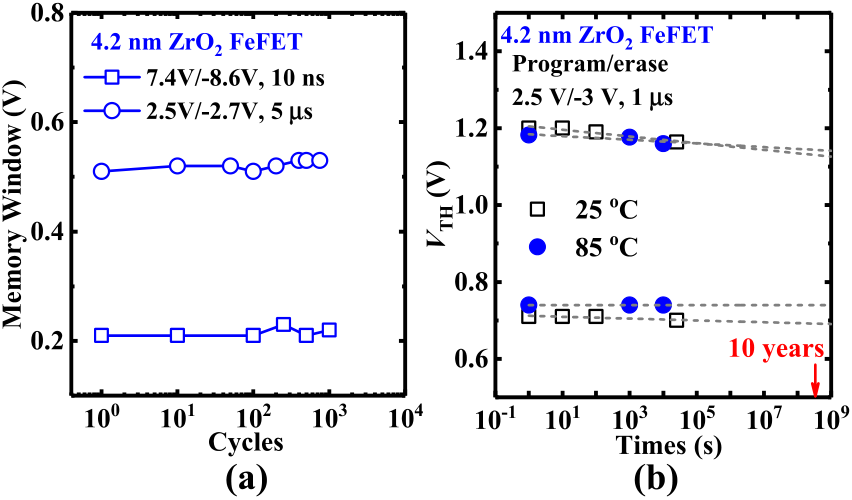
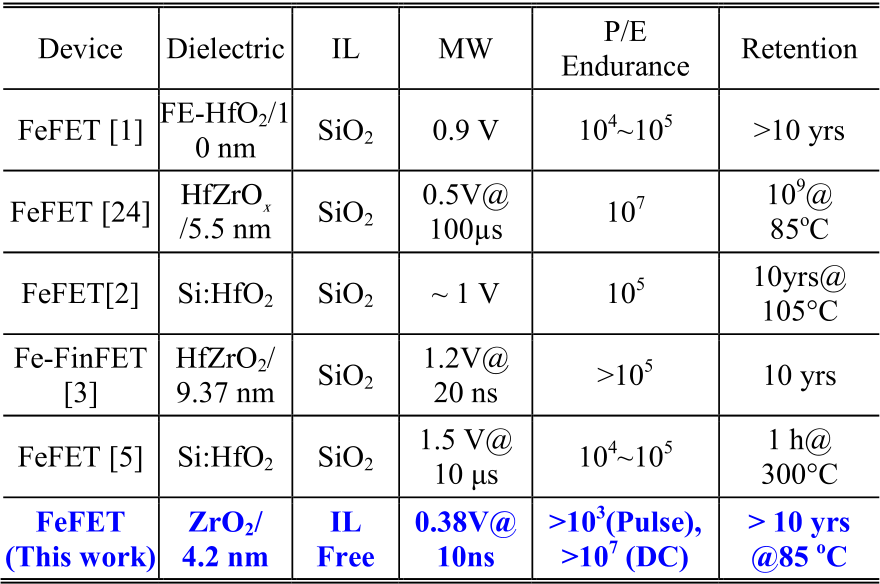


Fig. 6. (a) Endurance measurements under various P/E pulse condi-tions. No MW degradation is observed after 103P/E cycles for 4.2 nm-thick ZrO2 FeFET. (b) Retention testing results showing negligible MW degradation after 104s in 4.2 nm-thick ZrO2 FeFET. A MW over 0.4 V is extrapolated to be sustainable over 10 years at 25◦C and at 85◦C.

TABLE I

PERFORMANCE BENCHMARKING OF THE ZRO2 FEFET IN THIS WORK AGAINST REPORTED FEFET MEMORY DEVICES



Although no interfacial layer (IL) between ZrO2 and Ge is observed in Fig. 1(c), an GeO*x* IL adding ∼ 0.3 nm to the capacitance equivalent thickness (CET) was confirmed via

capacitance measurement [23]. Considering the GeO*x* IL and the effective thickness of ZrO2, Preisach model was used to fit the *P-V* loop of in Fig. 4(a), and the results indicated that the

real *V*c of ZrO2 is about 1.2 V. It should be noted that *V*c for the TaN/ZrO2/Ge gate stack is larger than that for previously reported doped-HfO2 devices [1], which is undesirable for memory cell endurance considerations. In addition to the low

depolarization field, the good endurance of ZrO2 FeFETs can be attributed to the fact that the ZrO2/Ge interface quality is high, even without any surface passivation [23].

Table I benchmarks the FeFET in this work against reported

FeFETs with regard to NVM performance metrics. Note that

the FeFET has the lowest dielectric thickness of 4.2 nm.

IV. CONCLUSION

ZrO2 FeFET is demonstrated for the first time to be suitable for NVM application. Due to their lower *Pr* and high-quality semiconductor interface, TaN/ZrO2/Ge FeFET can be operated with lower P/E voltages (for lower dynamic power consump-

tion) as compared against FeFETs, with high endurance and

long retention. 10 ns writing speed and 10 years retention at 85◦C are achieved in 4.2 nm-thick ZrO2 FeFET, making them a good candidate for embedded DRAM/Flash memory

applications.

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