

382 IEEE ELECTRON DEVICE LETTERS, VOL. 43, NO. 3, MARCH 2022

Logic Compatible High-Performance

Ferroelectric Transistor Memory

Sourav Dutta, Member, IEEE, Huacheng Ye, Graduate Student Member, IEEE,

Akif A. Khandker, G[ra](https://orcid.org/0000-0002-8162-9155)duate Student Member, IEEE,

Sharadindu Gopal Kirtania, Graduate Student Me[m](https://orcid.org/0000-0002-3628-3431)ber, IEEE,

Abhishek Khanna, Graduate Student M[e](https://orcid.org/0000-0001-6044-5173)mber, IEEE, Kai Ni, Member, IEEE,

and Suman Datta, Fellow, IEEE

***Abstract— Silicon channel ferroelectric field-effect tran-sistors (FeFETs) with low-k interfacial layer (IL) between ferroelectric and silicon channel suffers from high write voltage, limited write endurance and long read-after-write latency. This is due to early IL breakdown and mobile charge injection at the ferroelectric-IL interface. Here, we demon-strate low voltage, high speed memory operation with high write endurance using an IL-free back-end-of-line (BEOL) compatible FeFET. We fabricated IL-free FeFETs with 28nm channellength (Lg) and 126nmwidth undera thermal budget*** *<****4000C by integrating 5nm Hf0.5Zr0.5O2 (HZO) gate stack with amorphous Indium Tungsten Oxide (IWO) semicon-ductor channel. We report a voltage memory window of 1.6V with a read current window ILVT****/****IHVT of 105, write voltage of* ±*1.6V with 20ns pulses, instantaneousread-after-write latency*** *<****300ns and a record high write endurance exceeding 1011cycles. This establishes the IL-free BEOL FeFET as a promising candidate for logic-compatible high-performance last-level cache memory.***

***Index Terms— Ferroelectric memory, FeFET, interfacial layer (IL), BEOL, monolithic 3D, HZO, IWO, endurance.***

I. INTRODUCTION   
**H** ARNESSING polar orthorhombic phase Pca21 in thin films of doped Hafnium Oxide (HfO2*)*  such as

Zirconium-doped HfO2 (HZO), FeFET has emerged as one of the forerunners for embedded non-volatile memory. Recent

demonstrations have shown robust memory operation in

FeFETs built at relatively scaled CMOS technology nodes

Manuscript received December 29, 2021; revised January 23, 2022; accepted January 25, 2022. Date of publication February 1, 2022; date of current version February 24, 2022. This work was supported in part by the Applications and Systems Driven Center for Energy-Efficient Integrated NanoTechnologies (ASCENT), one of six centers in Joint University Microelectronics Program (JUMP), sponsored by Defense Advanced Research Projects Agency (DARPA) and the Semiconductor Research Corporation (SRC); and in part by the Innovative Materials and Processes for Accelerated Compute Technologies (IMPACT) Center in Nanoelectronic Computing Research (nCORE), sponsored by SRC. The review of this letter was arranged by Editor U. Schroeder. (Corresponding author: Sourav Dutta.)   
 Sourav Dutta, Huacheng Ye, Akif A. Khandker, Sharadindu Gopal Kirtania, Abhishek Khanna, and Suman Datta are with the Depart-ment of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556 USA (e-mail: sdutta4@nd.edu).

Kai Ni is with the Department of Microsystems Engineering, Rochester Institute of Technology, Rochester, NY 14623 USA.

Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LED.2022.3148669.

Digital Object Identifier 10.1109/LED.2022.3148669

Fig. 1. (a) Schematic of IL-free BEOL FeFET. (b) Top-view false colored SEM, (c) cross-sectional TEM and (d) EDS elemental mapping of an ultra-scaled FeFET with Lg = 28.3nm and width = 126nm.

(28nm planar bulk [1] and 22nm FD-SOI [2]). However, FeFET still needs to overcome several challenges before being considered as a high-performance memory candidate for applications such as on-chip weight-cell, buffer and last-level cache. Key technology challenges include high write voltage, limited write endurance, large read-after-write latency and BEOL-compatibility for monolithic 3D integration [3]–[7]. The limited write endurance in Si FeFET predominantly arises due to the presence of a low-k SiO2 IL between the ferroelectric (FE) gate stack and Si channel. During write operation, most of the voltage in the gate stack drops across the IL [8], [9]. The high electric-field stress across IL, along with continuous charge trapping and trap generation at the IL/Si and FE/IL interfaces limit the write endurance to 104-106 cycles [3]–[6]. Improving the write endurance requires us to either re-explore known techniques of IL engineering in HKMG technology such as reducing IL thickness through scavenging [10] and increasing dielectric constant of IL [11], or re-imagine novel ways to build an IL-free FeFET. The latter can be achieved by fabricating a back-gated, channel-last FeFET where a semiconductor channel material is grown directly on top of FE [12]–[17]. The absence of IL will allow lowering the write voltage, and significantly reduce the charge trapping, and trap generation at the FE/channel interface, thereby improving endurance.

0741-3106 © 2022 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: Georgia Institute of Technology. Downloaded on August 18,2022 at 03:40:30 UTC from IEEE Xplore. Restrictions apply.

DUTTA et al.: LOGIC COMPATIBLE HIGH-PERFORMANCE FERROELECTRIC TRANSISTOR MEMORY 383



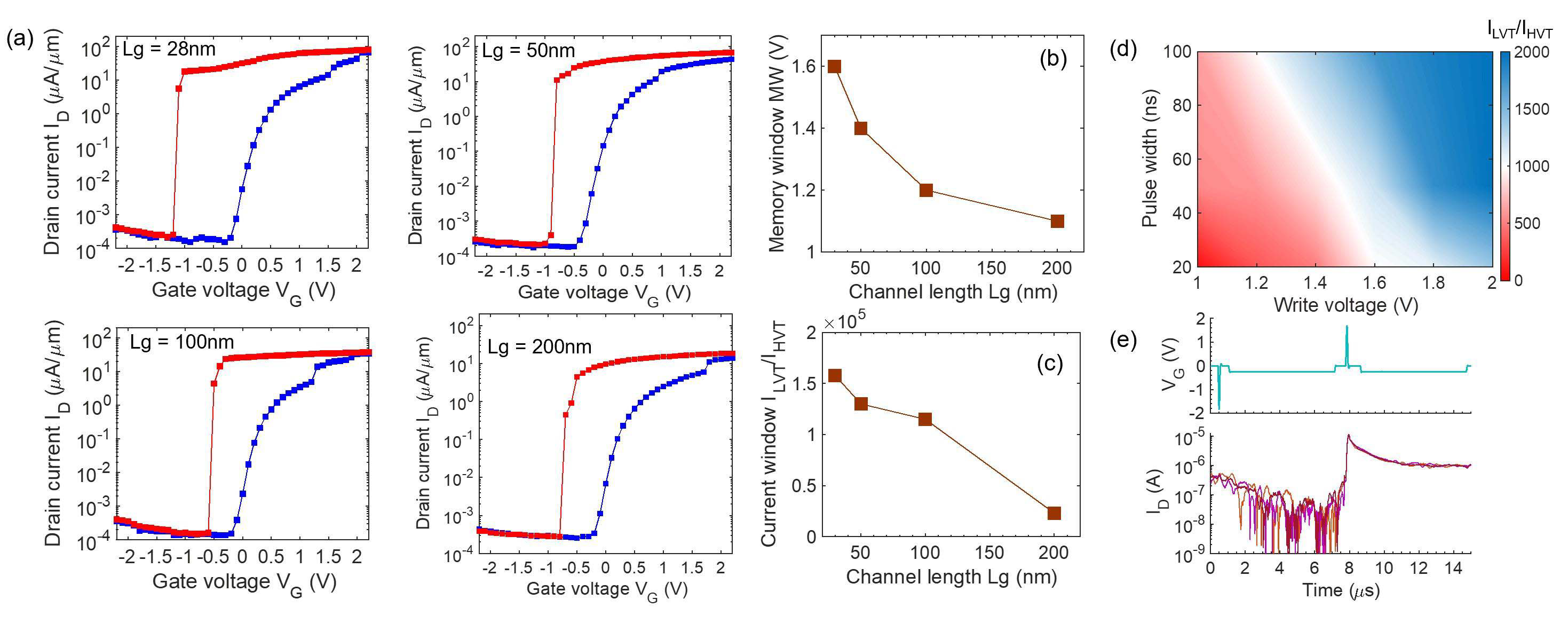


Fig. 2. (a) Dual-sweep DC Id-Vg characteristic measured for varying Lg from 28nm to 200nm and VDS = 0.2V. (b) Memory window and (c) current window ILVT*/*IHVT measured as a function of Lg. (d) Ultra-fast switching characteristics of the IL-free BEOL FeFET. (e) Transient measurements

show write operation with ±1.6V and 20ns pulses, and instantaneous read-after-write.

An IL-FeFET will also have a lower read-after-write latency compared to Si FeFET. The read delay is due to the electron and hole trapping at the FE/IL and IL/silicon interface, respec-tively, during the write operation. During programming with a positive gate voltage, electrons get trapped primarily at the FE/IL interface and the large read-after-write latency (around 10ms) is set by the time required to de-trap the electrons via tunneling through IL [3], [8]. Similarly, the erase operation with a negative gate voltage favors hole trapping primarily at the IL/Si interface, requiring around 100 *μ*s delay to de-trap [3], [8]. Thus, eliminating IL will allow faster de-trapping of charge, resulting in instantaneous read-after-write operation.

II. FABRICATION & CHARACTERIZATION OF IL-FREE FEFET

Fig. 1(a) shows the schematic of the fabricated IL-free FeFET. Plasma enhanced atomic layer deposition (PEALD) is used to deposit 5nm HZO on top of Tungsten (W) back gate. For strain-induced stabilization of the ferroelectricity in HZO, we sputter-deposit a W sacrificial capping layer (SCL) and perform rapid thermal anneal at 4000C for 300s in N2. Subsequently, W SCL is removed via etching. Next, 5nm of 1% by weight W-doped Indium Oxide (IWO) is sputtered in the presence of 0.02Pa excess O2 at room temperature. Finally, Pd source and drain electrodes are patterned and a post-metal anneal at 1500C N2 is done. The entire process temperature is kept within 4000C, making it BEOL com-patible. Fig. 1 (b) shows the top-view false-colored SEM of the fabricated FeFET, highlighting ultra-scaled dimensions of Lg = 28nm and width = 126nm. Figs. 1(c-d) show the cross-sectional TEM and EDS elemental mapping.

We perform dual-sweep DC Id-Vg as shown in Fig. 2(a) on FeFETs with Lg varying from 28nm to 200nm and a fixed

|  |
| --- |
| VDS = 0.2V. The voltage memory window (MW) at a constant current of 1*μA/μm.* The current window *ILV T /IHV T* is  measured as the ratio of currents in low Vt (ILVT*)* and high  Vt (IHVT*)* states at a read voltage *Vread* = −0*.*2V. We report a high MW = 1.6V for Lg = 28nm with a Vg sweep of  ± 2V. We also report a ILVT = 26*μA/μm* for program and IHVT = 0.0002*μA/μm* for erase operation, giving a |

high *ILV T /IHV T >* 105. Note that a steep slope of SS *<* 60mV/dec is measured during the reverse sweep owing to the ferroelectric switching kinetics [18]. Such a steep-slope, also known as transient negative capacitance (NC) effect, arises due to the lag between the temporal rate of change of polarization switching and rate of change of screening or compensating charge [19]–[21]. Fig. 2(b-c) shows both MW and *ILV T /IHV T* increasing with Lg scaling. To explain this, we use Synopsys TCAD simulations. Figs. 3(a-b) show the electric field distribution during the program and erase operation. While most of the electric field is concentrated underneath the overlap region between the source/drain and the back gate, there exists considerable fringing electric fields inside the channel region that assists the polarization switching in FE layer underneath the channel. Since the fringing field inside the channel increases with decreasing Lg, both MW and *ILV T /IHV T* monotonically increases with Lg scaling. The TCAD simulations also provide insights into the switching dynamics and the presence of large memory window even in the absence of holes in the IWO channel. During the programming operation, the positive polarization charge +PR inside HZO (pointing towards the IWO channel) is supported by the large electron charge density that accumulates inside the IWO channel (Fig. 3(c)). During erase, the negative polarization charge −PR (pointing away from the channel) is supported partly by the depletion charge inside the IWO channel and partly by the screening free charge provided by the source/drain electrodes in the overlap region (Fig. 3(d)).

We also performed TCAD simulations for FeFETs with different Lg. Fig. 3(e) shows the comparison in electric field distribution for Lg = 30nm and 100nm. As seen in Fig. 3(f), the average electric field inside the channel region of a shorter Lg device is much higher that assists in the polarization switching. This qualitatively explains our experimental results that both MW and *ILVT /IHV T* monotonically increases with Lg scaling.

Next, we characterized the fast write and read operation of the IL-free FeFET using a one-spot measurement scheme with fast read-out. Immediately after the write operation with a delay of around 300ns, we applied a short read pulse *Vread*

Authorized licensed use limited to: Georgia Institute of Technology. Downloaded on August 18,2022 at 03:40:30 UTC from IEEE Xplore. Restrictions apply.

384 IEEE ELECTRON DEVICE LETTERS, VOL. 43, NO. 3, MARCH 2022



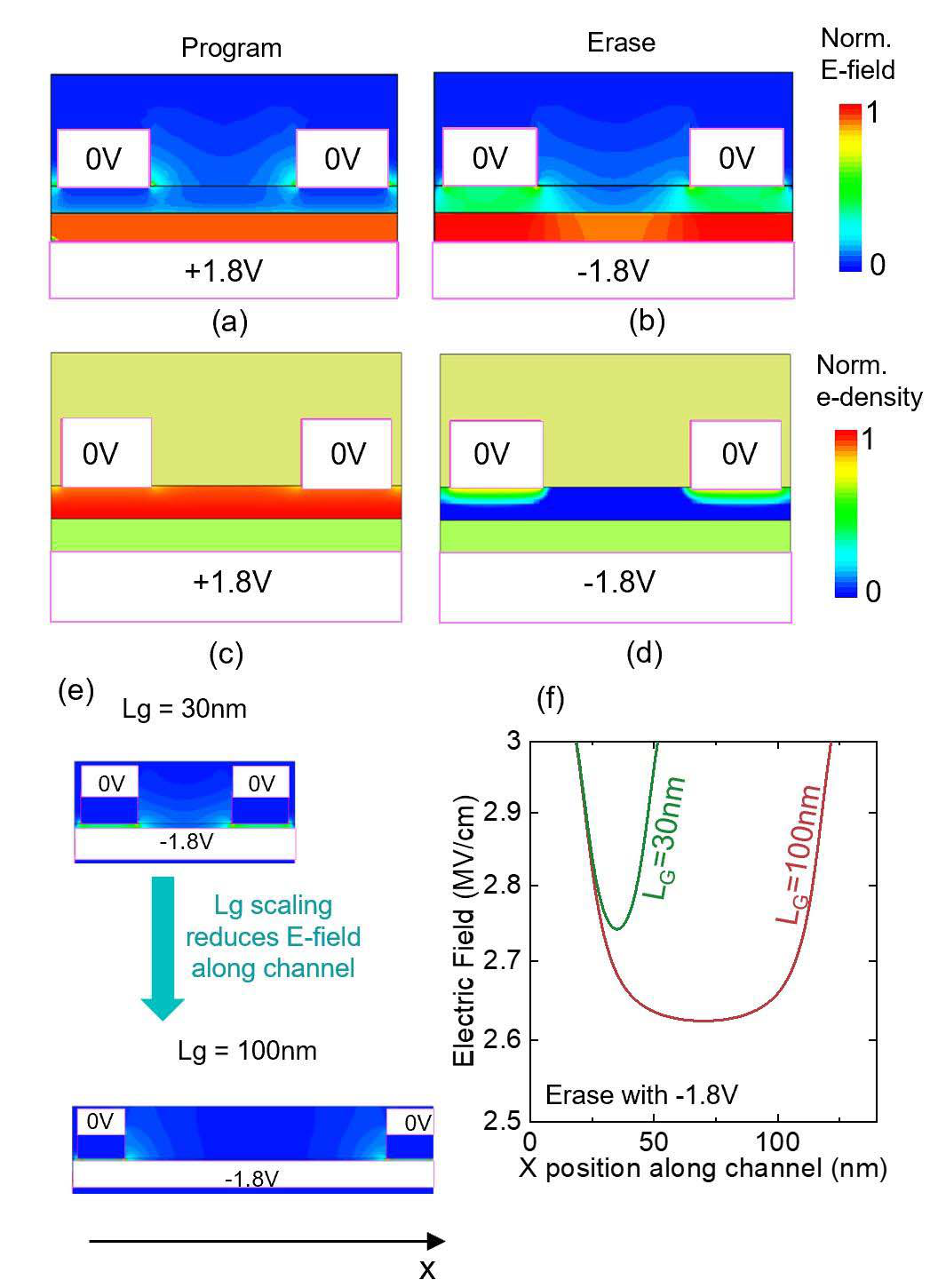


Fig. 3. field distribution and (c, d) electron density, during program and erase TCAD simulations for Lg = 30nm, showing (a-b) electric

operation. (e, f) Simulations for Lg = 30nm and 100nm, showing increase in fringing electric fields inside the channel region assisting polarization switching.

of around 5*μs* width to the gate of the FeFET to measure the drain current. Note that VDS = 0V is used during the write operation while VDS = 0.2V is applied only during the read operation. During the program and erase operation, we used different optimized current compliance settings for accurately capturing the ILVT and IHV. Finally, we calculated the current window as *ILV T /IHV T* . Fig. 2(d) shows the switching charac-teristics where a *ILV T /IHV T* ∼ 103is measured for write volt-age as low as ±1.6V and pulse width of 20ns. Fig. 2(e) shows a full transient measurement performed to demonstrate the absence of read latency. Note that here we used a continuous VDS applied throughout the measurement and a fixed current compliance of 10*μA*. This in turn increases the noise floor and limits the minimum current that can be measured as opposed to Fig. 2(d). We performed multiple transient measurements, 20ns pulses. We demonstrate instantaneous read-after-write showing high speed and low voltage operation with ±1.6V and operation with a measured read latency *<*300ns (limited by the setup), which is orders of magnitude improvement over conventional Si FeFET.

Next, we investigate the write endurance of the IL-free FeFET. Fig. 4(a) shows the bipolar pulse scheme with write pulses of ± 1.8V, 20ns with 100ns delay between the pulses. This is followed by periodic reading of the memory state using one-spot read-out scheme. Fig. 4(b) shows the dual-sweep DC Id-Vg of the FeFET pre- and post-1011cycling. We see an increase in the sub-threshold slope (SS) of the device post 1011endurance cycling. This can be associated with the generation of interface traps density (Nit) at the interface between HZO and IWO upon repeated switching of

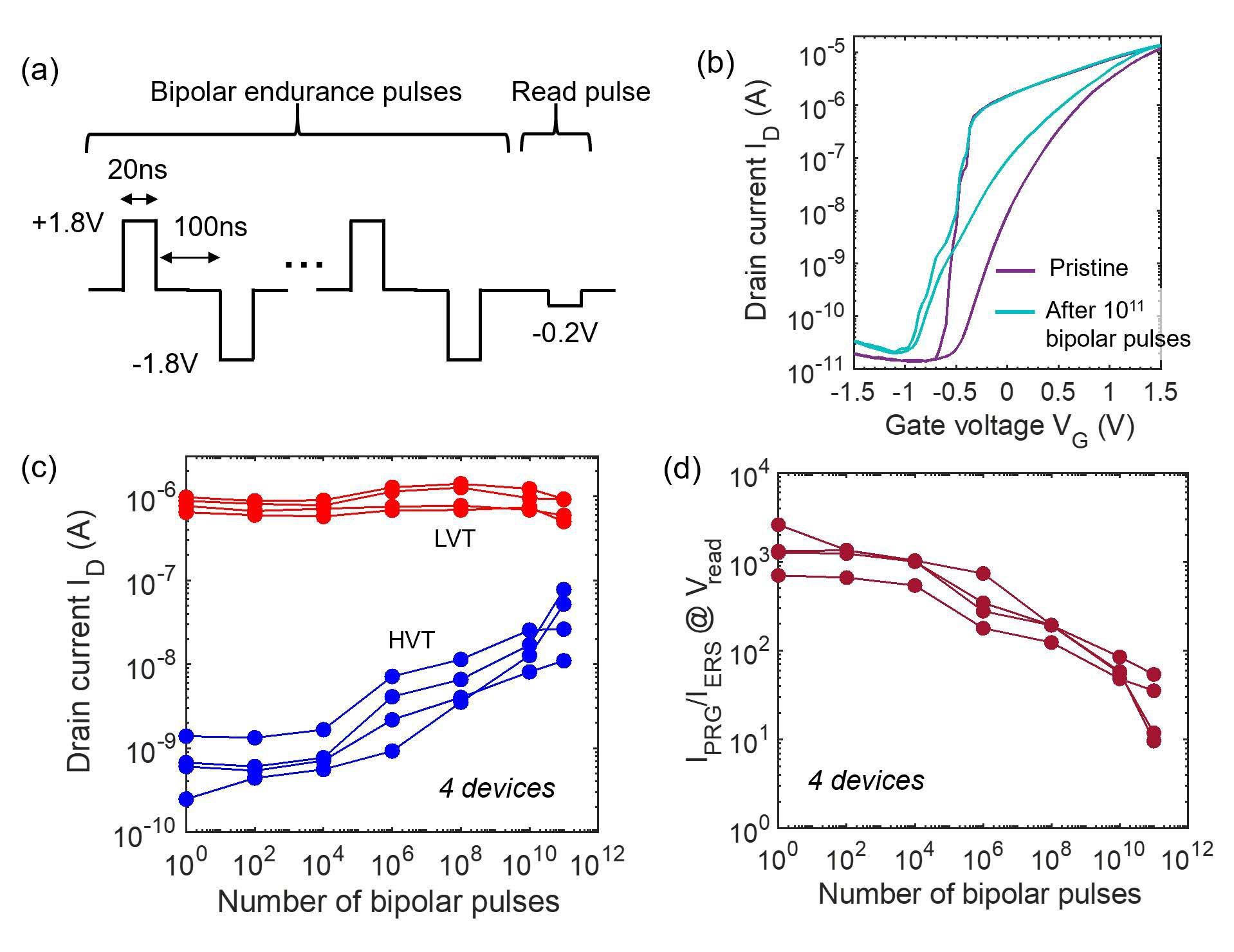


Fig. 4. (a) Bipolar pulse scheme for measuring write endurance.

(b) Dual-sweep DC Id-Vg characteristic measured pre and

post-1011cycling. (c) Read currents in the LVT and HVT states,

and (d) current window ILVT*/*IHVT measured on multiple devices as a

function of bipolar endurance pulses.

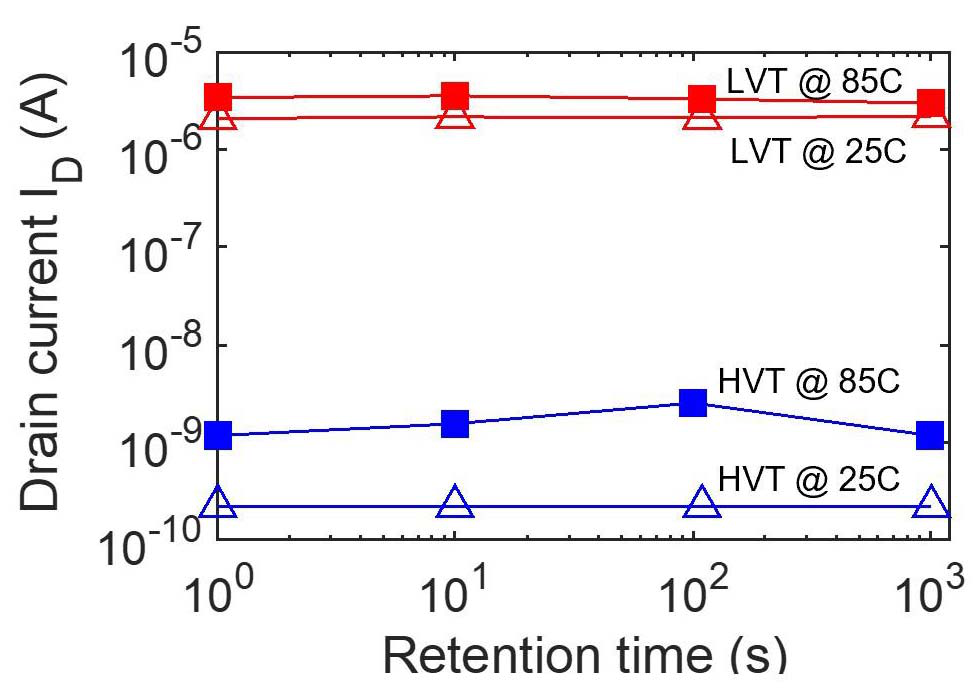


Fig. 5. Retention of IL-free FeFET, measured at room temperature (25C)

and at elevated temperature (85C).

polarization using bipolar endurance pulses. Similar effects

have been reported previously for Si FeFETs [7], [11]. How-

ever, in contrast to rapid degradation and permanent failure

exhibited by Si FeFETs after 104− 106cycles [3]–[7] due to catastrophic breakdown of the IL, we see a graceful degra-

dation. Note the presence of anti-clockwise hysteresis post

endurance cycling, denoting robust ferroelectricity in the 5nm

HZO with no sudden breakdown. Figs. 4(c) and (d) show the

measured ILVT and IHVT and current window *ILV T /IHV T* as a

function of endurance cycles, respectively. The measurements

were performed across four different devices. Even after 1011

bipolar pulses, *ILV T /IHV T* ∼ 50 is still maintained. We also characterize the retention of the FeFET at 250C and 850C,

showing no significant degradation as shown in Fig. 5.

III. CONCLUSION

The back-gated, channel last process for fabricating an

IL-free FeFET provides an effective pathway to realize a

logic-compatible, high-performance ferroelectric memory that

mitigates several challenges faced by conventional Si FeFETs.

In comparison to the state-of-the-art results reported on Si

FeFETs [2], [11], we report the best-in-class performance

with a lowest operating voltage of ±1.6V, high-speed write, instantaneous read-after-write operation and record high write

endurance exceeding 1011cycles. This makes IL-free BEOL

FeFET a strong candidate for embedded non-volatile memory.

Authorized licensed use limited to: Georgia Institute of Technology. Downloaded on August 18,2022 at 03:40:30 UTC from IEEE Xplore. Restrictions apply.

DUTTA et al.: LOGIC COMPATIBLE HIGH-PERFORMANCE FERROELECTRIC TRANSISTOR MEMORY 385



REFERENCES

[1] M. Trentzsch, S. Flachowsky, R. Richter, J. Paul, B. Reimer, D. Utess, S. Jansen, H. Mulaosmanovic, S. Müller, S. Slesazeck, and J. Ocker, “A 28 nm HKMG super low power embedded NVM technology based on ferroelectric FETs,” in *IEDM Tech. Dig.*, Dec. 2016, pp. 11.5.1–11.5.4, doi: [10.1109/IEDM.2016.7838397](http://dx.doi.org/10.1109/IEDM.2016.7838397).

[2] S. Dünkel, M. Trentzsch, R. Richter, P. Moll, C. Fuchs, O. Gehring, M. Majer, S. Wittek, B. Müller, T. Melde, and H. Mulaosmanovic,“A FeFET based super-low-power ultra-fast embedded NVM technology for 22 nm FDSOI and beyond,” in *IEDM Tech. Dig.*, Dec. 2017, pp. 19.7.1–19.7.4, doi: [10.1109/IEDM.2017.8268425](http://dx.doi.org/10.1109/IEDM.2017.8268425).

[3] E. Yurchuk, J. Müller, S. Müller, J. Paul, M. Peši´c, B. R. Van, U. Schroeder, and T. Mikolajick, “Charge-trapping phenomena in HfO2-based FeFET-type nonvolatile memories,” *IEEE Trans. Elec-* *tron*  *Devices*, vol. 63, no. 9, pp. 3501–3507, Sep. 2016, doi: [10.1109/TED.2016.2588439](http://dx.doi.org/10.1109/TED.2016.2588439).

[4] H. Mulaosmanovic, E. T. Breyer, T. Mikolajick, and S. Slesazeck,“Ferroelectric FETs with 20-nm-thick HfO2 layer for large mem-ory window and high performance,” *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 3828–3833, Sep. 2019, doi: [10.1109/TED.2019. 2930749](http://dx.doi.org/10.1109/TED.2019.2930749).

[5] T. Ali, P. Polakowski, S. Riedel, T. Büttner, T. Kämpfe, M. Rudolph, B. Pätzold, K. Seidel, D. Löhr, R. Hoffmann, M. Czernohorsky, K. Kühnel, P. Steinke, J. Calvo, K. Zimmermann, and J. Müller,“High endurance ferroelectric hafnium oxide-based FeFET memory without retention penalty,” *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3769–3774, Sep. 2018, doi: [10.1109/TED.2018.2856818](http://dx.doi.org/10.1109/TED.2018.2856818).

[6] A. J. Tan, M. Pe´sic, L. Larcher, Y. H. Liao, L. C. Wang, J. H. Bae, C. Hu, and S. Salahuddin, “Hot electrons as the dominant source of degradation for sub-5nm HZO FeFETs,” in *Proc. IEEE Symp. VLSI Tech-nol.*, May 2020, pp. 1–2, doi: [10.1109/VLSITechnology18217.2020. 9265067](http://dx.doi.org/10.1109/VLSITechnology18217.2020.9265067).

[7] N. Gong and T.-P. Ma, “A study of endurance issues in HfO2-based ferroelectric field effect transistors: Charge trapping and trap generation,”*IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 15–18, Jan. 2018, doi: [10.1109/LED.2017.2776263](http://dx.doi.org/10.1109/LED.2017.2776263).

[8] K. Ni, P. Sharma, J. Zhang, M. Jerry, J. A. Smith, K. Tapily, R. Clark, S. Mahapatra, and S. Datta, “Critical role of interlayer in Hf0*.*5Zr0*.*5O2 ferroelectric FET nonvolatile memory performance,” *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2461–2469, Jun. 2018, doi: [10.1109/TED.2018.2829122](http://dx.doi.org/10.1109/TED.2018.2829122).

[9] A. I. Khan, A. Keshavarzi, and S. Datta, “The future of ferroelectric field-effect transistor technology,” *Nature Electron.*, vol. 3, pp. 588–597, Oct. 2020, doi: [10.1038/s41928-020-00492-7](http://dx.doi.org/10.1038/s41928-020-00492-7).

[10] T. Ando, “Ultimate scaling of high-*κ* gate dielectrics: Higher-*κ* or interfacial layer scavenging?” *Materials*, vol. 5, no. 3, pp. 478–500, 2012, doi: [10.3390/ma5030478](http://dx.doi.org/10.3390/ma5030478).

[11] A. J. Tan, Y.-H. Liao, L.-C. Wang, N. Shanker, J.-H. Bae, C. Hu, and S. Salahuddin, “Ferroelectric HfO2 memory transistors with high-*κ* interfacial layer and write endurance exceeding 1010 cycles,” *IEEE Electron Device Lett.*, vol. 42, no. 7, pp. 994–997, Jul. 2021, doi: [10.1109/LED.2021.3083219](http://dx.doi.org/10.1109/LED.2021.3083219).

[12] A. A. Sharma, B. Doyle, H. J. Yoo, I. C. Tung, J. Kavalieros, M. V. Metz, M. Reshotko, P. Majhi, T. Brown-Heft, Y. J. Chen, and V. H. Le, “High speed memory operation in channel-last, back-gated fer-roelectric transistors,” in *IEDM Tech. Dig.*, Oct. 2020, pp. 18.5.1–18.5.4, doi: [10.1109/IEDM13553.2020.9371940](http://dx.doi.org/10.1109/IEDM13553.2020.9371940).

[13] F. Mo, Y. Tagawa, C. Jin, M. Ahn, T. Saraya, T. Hiramoto, and M. Kobayashi, “Experimental demonstration of ferroelectric HfO2 FET with ultrathin-body IGZO for high-density and low-power memory application,” in *Proc. Symp. VLSI Technol.*, 2019, pp. T42–T43, doi: [10.23919/VLSIT.2019.8776553](http://dx.doi.org/10.23919/VLSIT.2019.8776553).

|  |  |  |
| --- | --- | --- |
| [14] F. Mo, Y. Tagawa, | C. Jin, M. Ahn, T. Saraya, | T. Hiramoto, |

and M. Kobayashi, “Low-voltage operating ferroelectric FET with ultrathin IGZO channel for high-density memory application,” in *IEEE J. Electron Devices Soc.*, vol. 8, pp. 717–723, 2020, doi: [10.1109/JEDS.2020.3008789](http://dx.doi.org/10.1109/JEDS.2020.3008789).

[15] M. Halter, L. Bégon-Lours, V. Bragaglia, M. Sousa, B. J. Offrein, S. Abel, M. Luisier, and J. Fompeyrine, “Back-end, CMOS-compatible ferroelectric field-effect transistor for synaptic weights,” *ACS Appl.*

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| *Mater.* | *Interface*, | vol. | 12, | no. | 15, | pp. 17725–17732, 2020, | doi: |
| [10.1021/acsami.0c00877](http://dx.doi.org/10.1021/acsami.0c00877). | | |

[16] M. K. Kim and J. S. Lee, “Ferroelectric analog synaptic tran-sistors,” *Nano Lett.*, vol. 19, no. 3, pp. 2044–2050, 2019, doi: [10.1021/acs.nanolett.9b00180](http://dx.doi.org/10.1021/acs.nanolett.9b00180).

[17] S. Dutta, H. Ye, W. Chakraborty, Y. C. Luo, J. M. San, B. Grisafe, A. Khanna, I. S. S. Lightcap, S. Yu, and S. Datta, “Monolithic 3D integration of high endurance multi-bit ferroelectric FET for accelerating compute-in-memory,” in *IEDM Tech. Dig.*, Oct. 020, pp. 36.4.1–36.4.4, doi: [10.1109/IEDM13553.2020.9371974](http://dx.doi.org/10.1109/IEDM13553.2020.9371974).

[18] M. Jerry, J. A. Smith, K. Ni, A. Saha, S. Gupta, and S. Datta, “Insinhts on the DC characterization of ferroelectric field-effect- transistors,” in *Proc. 76th Device Res. Conf. (DRC)*, 2018, pp. 1–2, doi: [10.1109/DRC.2018.8442191](http://dx.doi.org/10.1109/DRC.2018.8442191).

[19] P. Sharma, J. Zhang, K. Ni, and S. Datta, “Time-resolved measurement of negative capacitance,” *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 272–275, Feb. 2018, doi: [10.1109/LED.2017.2782261](http://dx.doi.org/10.1109/LED.2017.2782261).

[20] J. Gomez, S. Dutta, K. Ni, S. Joshi, and S. Datta, “Steep slope

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ferroelectric | | field | effect | transistor,” | in | *Proc.* | *Electron* | *Devices* | |
| *Technol.* | *Manuf.* | | *Conf.* | *(EDTM)*, | Feb. | 2019, | pp. 59–61, | | doi: |

[10.1109/EDTM.2019.8731115](http://dx.doi.org/10.1109/EDTM.2019.8731115).

[21] J. Gomez, S. Dutta, K. Ni, J. A. Smith, B. Grisafe, A. Khan, and S. Datta,“Hysteresis-free negative capacitance in the multi-domain scenario for logic applications,” in *IEDM Tech. Dig.*, Oct. 2019, pp. 7.1.1–7.1.4, doi: [10.1109/IEDM19573.2019.8993638](http://dx.doi.org/10.1109/IEDM19573.2019.8993638).

Authorized licensed use limited to: Georgia Institute of Technology. Downloaded on August 18,2022 at 03:40:30 UTC from IEEE Xplore. Restrictions apply.