Origin of the Endurance Degradation in the Novel HfO2-based 1T Ferroelectric Non-Volatile Memories

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***Abstract*— Novel HfO2-based non-volatile ferroelectric field effect transistors (FeFETs) reveal integration and scaling properties superior to the devices utilizing perovskite-type ferroelectrics. However, until now the switching endurance of only 104 program/erase cycles could be proven. The mechanisms responsible for the cycling degradation have been scarcely studied so far. Therefore, the scope of this paper is to clarify the origin of the cycling degradation in HfO2-based FeFETs. Several possible degradation mechanisms – fatigue of the ferroelectric layer and degradation of the transistor gate stack – are proposed and investigated. The limited endurance properties were found to**

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| **be linked to the transistor gate stack reliability rather than to the** | | | | | | |
| **ferroelectric** | |  | | --- | | **material** | | **itself.** | **The** | **gate** | **leakage** | **current** |

**measurements and the trapping analyses presented in this paper identified a degradation of the interfacial layer in the gate stack, which in turn is strongly linked to a reduction of ferroelectric memory window.**

***KeywordsHfO2; ferroelectric; non-volatile memory; FeFET; MFIS-FET; endurance; degradation mechanisms***

I. INTRODUCTION

The ferroelectric field effect transistor (FeFET) is considered as a promising candidate for future non-volatile memory applications [1]. In the FeFET two stable polarization states of a ferroelectric material incorporated into a transistor gate stack are utilized for data storage. The concept of a non-volatile ferroelectric transistor was introduced in the late 50’s of the last century [2]. Its industrial implementation is, however, still missing primarily due to the integration [3] and scaling obstacles [4] associated with conventionally used perovskite-type ferroelectrics (PZT, SBT). The recently discovered ferroelectric properties of HfO2-based thin films [5] overcome these issues. By utilizing ferroelectric Si:HfO2, it is

possible to fabricate FeFET devices at a state-of-the-art 28 nm technology node [6]. Low operation voltages (4 – 6 V) and switching times in the range of a few nanoseconds could be demonstrated for these devices [6]. In the first HfO2-based FeFETs, however, the memory window (*MW*) closes after about 104 – 105 program/erase cycles [7]. FeFETs with conventional ferroelectrics, on the other hand, are reported to withstand up to 1012 program/erase cycles [8].

In order to identify the main cause of the limited endurance in Si:HfO2-based FeFETs we performed an extensive study of their endurance behavior using capacitor and transistor structures. The gate stack structure of the studied ferroelectric transistors is similar to an ordinary high-*k* metal gate stack, whereas a thicker and crystalline high-*k* layer exhibits additionally ferroelectric properties. Therefore, the observed endurance degradation can be explained in the context of either reliability aspects of the ferroelectric material or the entire high-*k* metal gate stack. In the present paper we will consider and explore both scenarios.

II. EXPERIMENTAL DETAILS

The metal-ferroelectric-insulator-semiconductor field effect transistors (MFIS-FETs) studied in this paper feature a poly-Si/TiN (8 nm)/Si:HfO2 (9 nm)/SiON (1.2 nm) gate stack. The devices were manufactured using a state-of-the-art 28 nm high-*k* metal-gate technology on 300 mm wafers [6]. Metal-ferroelectric-metal (MFM) capacitor structures consisting of a Pt (50 nm) /TiN (10 nm)/Si:HfO2 (9 nm)/TiN (10 nm) film stack were fabricated on 300 mm silicon substrates [9]. Both device types included 9 nm thick HfO2 films doped with 4.4 mol% SiO2, known to exhibite the best ferroelectric behavior as evaluated in [9].

978-1-4799-3317-4/14/$31.00 ©2014 IEEE 2E.5.1

Polarization-voltage characteristics of the MFM capacitors were recorded using the aixACCT TF Analyzer 3000 by applying triangular pulses at 1 kHz frequency and measuring transient current response, which is subsequently converted into a polarization hysteresis.

The trapping behavior of Si:HfO2 layer within the transistor gate stack was studied with the help of a single-pulse *ID-VG* technique [10], [11]. This method allows for a more accurate characterization of the amount of charge trapped during the stress time. Since the *ID-VG* characteristics are measured directly at the rising and falling edges of a stress pulse applied to the gate, the time delay between stressing and sensing is practically eliminated. The threshold voltage(*VTH*) shift induced by the stress pulse gives a quantitative estimation of the amount of trapped charges. The measurement setup used in this work allowed exploiting pulses with rise/fall transition times of 500 ns. The pulse width was varied between 500 ns and 100 μs. The drain voltage was set to 300 mV in order to maximize the signal-to-noise ratio. The *VTH* values were extracted using a constant drain current criterion.

The interface trap density was analyzed by means of variable base level charge pumping technique [12], [13]. The interfacial traps, located directly at the Si / SiON interface, as well as traps, located within the interfacial SiON layer close to the Si interface, are accessed. The charge-pumping current was induced by applying ac signal of 1 MHz and constant amplitude of 1.8 V to the gate. The base gate voltage (*VG BASE*) was varied between -2.5 and + 0.5 V, forcing the Si surface to transit from accumulation into inversion.

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| device into the “ON”- and “OFF”-state and reading out the | | | | | | | | | | | | | |
| corresponding *VTH* | | | | | values. | | A | more pronounced *MW* | | | | | |
| degradation | | | was | | detected | | for | the | | alternating | | | pulses |
| accompanied by continuous polarization switching, whereas for unipolar pulses only slight shifts in the *VTH*-values of both memory states were observed. From that we deduce, that the polarization switching itself or mechanisms coupled with alternating pulses aggravate the endurance degradation in Si:HfO2-based FeFETs. | | | | | | | | | | | | | |
| -1  10 | | | | 0 10 | 1  10 | | 2 10 | 3  10 | | | 4  10 | | 5  10 |
| 1.0 | | | **OFF state (- 6 V100 ns )** | | | | | (a) | | | | | |
| VTH (V) | | 0.5 | **VSENSE** | | **residual MW: 0.9 V** | | | | | | | | |
| 0.0 |
| -0.5 | | | **ON state ( + 4 V100 ns )** | | | | | | | | | | |
| MW (V) | 1.5 | | |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | |  |  |  |  |  |  |  | | | | | | | | | | | |
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| 2) | 20 | Voltage | / | Sense | Stress | Sense | 3 V | (a) | 0.8 | VC (V) | VTH (V) | 4 | **Initialization** | | **//** | **Trapping test** | (a) |
| **200 ns** | | **t PULSE**  **VTH1**  **VTH2** |
| 1 kHz | 1 MHz | Time | | | **+ 4 V 0 V**  **- 6 V**   |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | | |  |  | |  |  |  | | |   **200 ns** | | VTH 1 |
| 1 kHz | | | **1 s** |
| (b) | | |
| P | Stress cycles | |
| 10 |
| 0.4 |
| initial | 1E4 |
| VTH 2 |
| PR (μC/cm | PR+/PR- | +PR | V | | | 3 | 10 | 5E4 |
| 0 | 0.0 | 100 | 1E5 |
| / | VC+/VC- | – VC |
| 1000 | |
| -10 | +VC | | | -0.4 | 2 |
| – PR | | |

|  |  |  |  |
| --- | --- | --- | --- |
| -20  10-1 10 0 10 | 1 10 | 2 10 | -0.8 |
| 3 10 4 10 5 10 6 10 7 10 8 10 9 10 10 |

Number of stress cycles

Figure 3. Program/erase cycling characteristics of an MFM capacitor at a stress frequency of 1 MHz. (a) Experimental gate pulse sequence; (b) The remanent polarization (*PR*) and coercive voltage (*VC*) as functions of stress cycles.

Number of program/erase cycles:   
1E-3 initial   
 100

|  |  |  |
| --- | --- | --- |
| 2) | 3  10 | 3  5x10 |
| 1E-5  IG (A/cm | 3  2x10 |
| 1E-7 | 4  10 |

4  
 2x10

4  
 5x10

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| --- | --- | --- | --- |
| 0 | 1 | VG (V) | 2 |

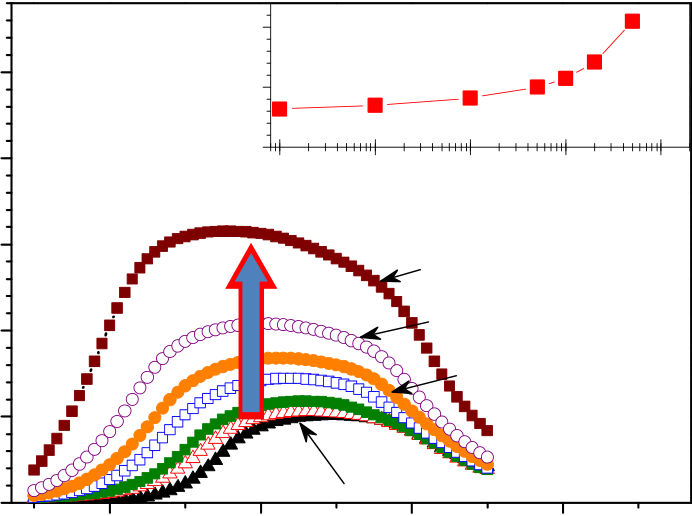
Figure 4. Evolution of gate leakage current characteristics (*IG-VG*) of MFIS-FETs with continuous program/erase cycling.

The endurance properties of the Si:HfO2 ferroelectric material were studied while decoupled from the high-*k* metal gate stack by using MFM capacitor structures. The development of the remanent polarization (*PR*) and the coercive voltage (*VC*) with cycling, inducing continuous polarization switching, was examined (Figure 3). The test frequency was set to 1 MHz, which provides a stress pulse length comparable to program/erase pulses used for transistor operation. The *PR* and *VC*  values were extracted from polarization-voltage characteristics recorded at different stages of cycling (inset Figure 3(b)). Fatigue-free behavior was detected up to 106 program/erase cycles. Thus, the endurance of the FeFET devices is not limited by the Si:HfO2 material itself.

We examined the possibility of the gate stack degradation by monitoring the gate leakage current of MFIS-FET devices during program/erase cycling (Figure 4). An increase in the gate current was detected after 103 cycles, which correlated well with the onset of the *MW* degradation (Figure 1). Gate leakage current induced during endurance stress was verified on devices with varying gate areas and lengths. The gate leakage was found to scale together with the gate area, which indicates a homogeneous degradation of the gate stack under cycling stress. In order to identify the degradation path within the gate stack, trap density was additionally characterized at different stages of the endurance testing.

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| 0 | | -7  10 | | -6 -5  10 10  trapping pulse width (s) | | | -4  10 | (b) |
| VTH2 - VTH1 (V) | 2.5 2.0 1.5 1.0 | | |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | |  |  |  |  |  |  |  | | | | | | |
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the Si:HfO2 traps was examined after different number of endurance stress cycles (Figure 5). The trapping characteristics were recorded using the pulse sequence schematically shown in Figure 5 (a). The *VTH* shift between the rising and the falling edges of the trapping pulse was measured as a function of pulse width for trapping voltage of 3.5 V. Before each trapping pulse an identical initial state was re-established with a combination of a negative (– 6 V/ 200 ns) and a positive (+ 4 V/ 200 ns) pulses followed by a delay of 1 s. The resulting trapping characteristics are depicted in Figure 5 (b). With increasing number of program/erase pulses no significant change in the trapping window (Δ*VTH*) was visible up to 104 cycles (Figure 5 (c)). For higher cycling numbers the trapping window even started to decrease. This was predominantly determined by the shift of the *VTH1* to higher positive voltages, reflecting the degradation of the “ON” memory state, whereas the *VTH2* remained almost unaffected by cycling. The slope of the trapping characteristic remained independent on the number of program/erase operations (Figure 5 (d)). Therefore, it can be deduced that only negligible generation of new bulk traps within the Si:HfO2 layer occurred during endurance stress. The decrease of the trapping window with cycling indicates a build-up of permanent negative charge within the dielectric stack. The possible origins are fixed charges generated during cycling or accumulation of electrons stuck on the deep traps. This permanent negative charge modifies the field distribution within the gate stack and reduces the injection current during trapping. Permanent negative charge should simultaneously deteriorate the ferroelectric switching during negative gate pulses. The contrary trend is, however, observed (Figure 1 and Figure 2). The degradation of the memory window with cycling is predominantly determined by the shift of the “ON” –state, written with positive gate pulses. Additional investigations are required to clarify this observation.

Furthermore, the interfacial trap density evolution with progressive cycling was monitored using variable base level charge pumping (CP) technique (Figure 6). An increase in the charge pumping current indicated a change in the trap density of the interfacial SiON layer by almost one order of magnitude. The strong increase in the interfacial trap density after 103 cycles goes along with an increase in the gate leakage current. Therefore, we conclude that the degradation of the gate leakage current is mainly related to the degradation of the interfacial SiON layer. The high density of generated traps impairs its insulating properties. A prevailing degradation of the interface layer in standard high-*k* transistor gate stacks exposed to positive or negative bias stress was ascertained by various research groups [20], [21], [22]. Moreover, alternating stress was reported to accelerate the degradation [23], [24], which was assigned to the wear-out of the interfacial layer due to continuous back and forth tunneling of charges [25]. In comparison to the standard high-*k* gate stacks the charge injection into the ferroelectric transistor is further enhanced. The ferroelectric polarization charge of the Si:HfO2 layer induces internal fields, which facilitate charge injection from the channel. Positive polarization established by positive gate voltages simultaneously assists the electron injection, while negative polarization induced by negative gate voltages facilitates hole injection. Therefore, steady transfer of charges through the interfacial layer is inevitable under alternating

program/erase pulses. The degradation of the insulating properties of the interfacial layer can have a strong impact on the memory operation of the FeFET. Free charges can be easily injected from the channel into the ferroelectric layer, compensating its polarization, which eventually degrades the ferroelectric memory window. Charge injection was one of the issues identified in the first peroskite-based FeFET devices [26], [27], for which the ferroelectric layer was fabricated directly on the semiconductor substrate. In order to improve the endurance properties, operation conditions or/and dielectric stack should be optimized in a way that enables to moderate the electric field across the interface layer and reduce the charge trapping.

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| 2) | 250 | NCP | 2**)** | 10 | 11 x 10 | 1  10 | 2  10 | 3  10 | 4  10 |
| **(**Traps/cm | 5 |
| 200 | 0 | 0  10 |
| ICP (mA/cm | 150 |
| Number of cycles | | | |
| after 5x10 3 cycles | | | |
| 100 | after 2x10 3 cycles | | | |
| after 10 3 cycles | | | |

50

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 0 | -2 | initial | | 1 |
| -1 | 0 |
| VG BASE (V) | |

Figure 6. Variable base level CP characteristics with increasing number of program/erase cycles. Insert shows the interface trap density, extracted from the CP characteristics, as a function of cycle number.

IV. CONCLUSIONS

In summary, the endurance behavior of Si:HfO2-based FeFET devices was studied in order to identify the root cause for its limited endurance capability of 104-105 program/erase cycles. The reliability of the transistor gate stack rather than of the ferroelectric layer itself was found to be responsible for the degradation of the ferroelectric memory window with cycling. Increase in the gate leakage current was detected with progressive endurance stress, correlating to a simultaneously appearing degradation of the ferroelectric memory window. Based on the charge trapping analyses the interfacial SiON layer was identified as the main reliability concern within the gate stack. The deteriorated insulating properties of the interfacial layer are held responsible for the decrease of the ferroelectric memory window with cycling. Optimization of the operation conditions or/and gate stack structure is required to improve the endurance properties.

ACKNOWLEDGMENT

This work was financially supported within the EFRE fund of the European Community and by the Free State of Saxony (Cool Memory/HEIKO).

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