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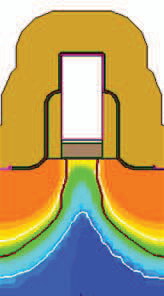
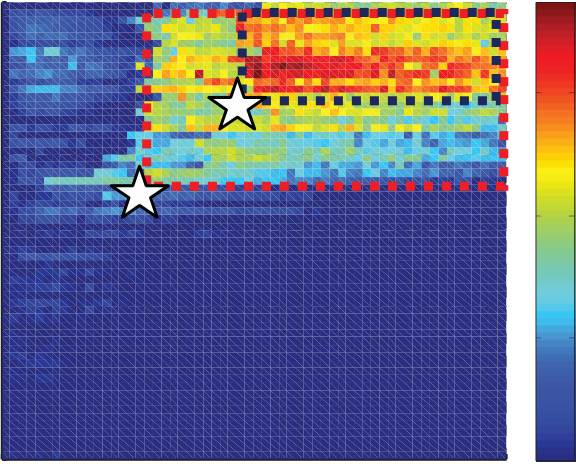
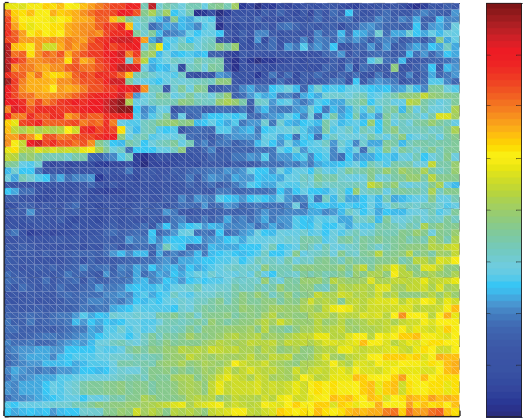
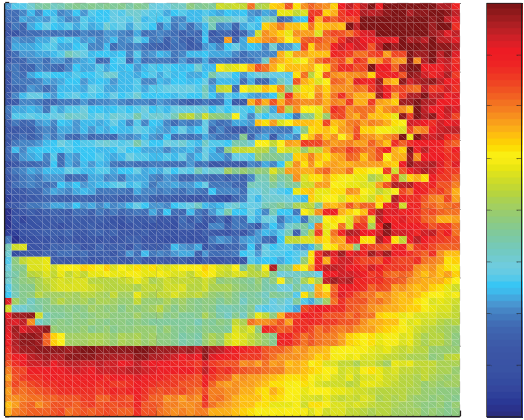
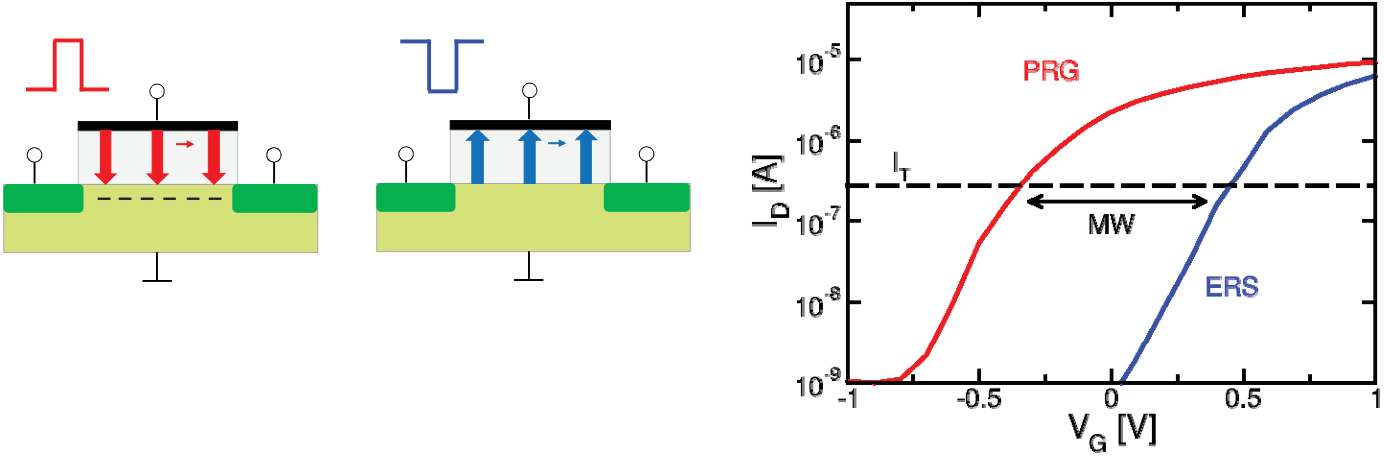
**Introduction**: Recent discovery of ferroelectricity in HfO2 thin films paved the way for demonstration of ultra-scaled 28 nm Ferroelectric FETs (FeFET) as non-volatile memory (NVM) cells [1]. However, such small devices are inevitably sensible to the granularity of the polycrystalline gate oxide film. Here we report for the first time the evidence of single ferroelectric (FE) domain switching in such scaled devices. These properties are sensed in terms of abrupt threshold voltage (*VT*) shifts leading to stable intermediate *VT* levels. We emphasize that this feature enables multi-level cell (MLC) FeFETs and gives a new perspective on steep subthreshold devices based on ferroelectric HfO2.

**Experimental**: Fig. 1 shows the TEM image of the Metal-Ferroelectric-Insulator-Silicon Field Effect Transistor (MFIS-FET) examined in this work. It features a poly-Si/TiN (8 nm)/HfO2 (10 nm)/SiON (1.2 nm) gate-stack and *W*=80 nm and *L*=30 nm are channel width and length respectively. Fig. 2 illustrates the memory operation of FeFETs: positive *VG* pulse sets the cell into the low *VT*state (Program), while negative *VG* pulse results in the high *VT* state (Erase) by the polarization switching of the FE layer. The difference of the two *VT*s defines the cell’s memory window (MW) as depicted in Fig. 3. In order to investigate the effect of FE polarization switching on *VT* and MW, the waveform of Fig. 4 is adopted for *VG*: after initial 100 bipolar cycles for device preconditioning [3], follows the sequence of Reference Erase pulse, defining the high reference *VT* state, and a variable Program pulse, increasing in 50 mV steps. **Evidence of single domain switching:** Fig. 5 shows exemplarily the evolution of the VT level for both PRG and ERS incremental gate pulse sweeps and fixed Reference levels: two clear discrete VT jumps are observed only at certain VG values. These steps indicate abrupt polarization switching of two distinct FE domains within the HfO2 film occurring at intrinsically different coercive fields (EC). Fig. 6 extends this analysis for different combinations of reference and incremental writing pulses for the same cell. Three significant traces for different reference pulses are highlighted in Fig. 6b) showing that the occurrence of *VT* jumps depend on the initial *VT* state determined by the reference pulse: if Ref ERS is large enough to back-switch both domains inducing the highest *VT* state, their switching into the low *VT* state will be visible during the incremental PRG sweep (upper trace); otherwise, when one or both domains are not back-switched (middle and lower trace, respectively), only one or no *VT* jumps will be observed. Fig. 7 depicts the resulting MW dependence on PRG and ERS voltage, which is calculated from Fig. 6c) by subtracting the reference erase *VT* value from each point along the program traces. Obviously, three distinct MW regions can be distinguished, corresponding to none (blue), one (light-blue) and both (red) domains switched. The two stars indicate the minimum PRG and ERS voltages, above which the individual domains can be switched. Further strengthening of our hypothesis is given by

TCAD simulations: Fig. 8 illustrates the implemented 2D-FeFET structure, the gate stack comprising two distinct FE domains with different *EC* in the adopted Preisach model. The *VT* vs. *VG* curve confirms *VT* jumps as observed experimentally.

**Multi-level cell capability**: Fig. 9a) shows the *VT* vs. *VG*curves for both ERS and PRG incremental pulse sweeps with distinct intermediate *VT* levels. The feasibility to set the cell into two separate *VT* levels is demonstrated by applying *VG* voltages as indicated by the vertical lines (-4.5V and -4.85V), starting always from the low *VT* state (PRG at +4V). The procedure is repeated 50 times. Fig.s 9 b) and c) show *ID*-*VG* curves and cumulative distributions, respectively, of the corresponding three *VT* states, indicating a very low cycle-to-cycle variability. Moreover, the cycling test with a pulse width of 500 ns shown in Fig. 10 reveals more than 10 5 endurance cycles with clearly separated three states. In addition, retention characterization was performed at room temperature and obviously no *VT* jumps are visible in Fig. 11, indicating that the polarization states of the single domains are stable and the slight gradual *VT* drift originates most probably from de-trapping of parasitic charges. The cumulative distribution of the first *VT* jump of 60 cells is represented in Fig. 12 for both ERS and PRG sweeps. It is clear that most of the domains can be switched below 4V and |-5V|. A similar distribution is obtained for *L*=90 nm FeFET as well, which however has more polycrystalline grains and hence more FE domains, and consequently more *VT* jumps, as shown in Fig. 13. **Film engineering:** The variability of switching voltages can be explained by a surface energy effect on the transition barrier for polarization reversal, which depends on the grain size [4], doping and furthermore on grain orientation. In the top-view TEM image of an 80nm x 30nm device in Fig. 14a) four HfO2 grains with varying sizes can be clearly distinguished. Fig. 14b) depicts the top-view SEM image of the HfO2 film, from which the grain size distribution is extracted. Correlating this distribution and the voltage jump distribution of Fig. 12 the relation in Fig. 15 is obtained. Therefore, the key for the MLC capability optimization of FeFET devices towards low switching voltages is the engineering of polycrystalline films. Various CMOS compatible processing conditions impact the MW as depicted in Fig. 16. **Conclusion**: The stable switching of single domains within one device opens the path of exploiting MLC FeFETs for non-volatile data storage. We believe the origin of single domain switching at different *VG*comes from the polycrystalline structure of the FE HfO2 film. These observations suggest that for future memory applications a multi-domain FE film might be preferable, enabling MLC capability, likewise for the realization of 3D architectures. Accurate material and grain engineering is of utmost importance. Further, these results indicate that for steep subthreshold devices based on single domain switching [5] mono-crystalline epitaxial grown FE films might be inevitable.

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| Fig. 1 – TEM image of 30-nm Si:HfO2-based MFIS-FET device. Ferroelectric layer is a thin polycrystalline film. | VG>0 | VG<0 | | | | | | | | | | |
| S | D | S | D | | | | | | | | |
| **P** | **P** | | | | | | | | | | |
| ����������� | ����������� | | | | | | | | | | |
| Fig. 2 – Schematic illustration of FeFET  operation. The polarization state of the FE | | | | | | | | | | | |
| film can be reversed by suitable *VG* pulses: for *VG* >0 (Program, PRG) FeFET is brought into inversion, while for *VG*<0 (Erase, ERS) into accumulation regime. | | | | Fig. 3 – *ID-VG*curves for programmed (red)  and erased (blue) state. MW extracted as  the *VT* difference evaluated with the  constant current criterion [2] as | | | | | | | |
| *IT*=0.1μA•*W/L*. | | | | | | | | | | | |
| Ref ERS -5V | | | | | Ref PRG 4V | | | | | | |
| a) | | | | |  |  |  |  |  |  | |
|  |  |
|  |  |  |
| b) | |



Fig. 4 – *VG* waveform scheme used in the measurement. Wake-up: 100 bipolar pulses. Reference ERS pulse sets the high *VT* state, while incrementally increasing PRG explores the switching

to the low *VT* state. Each write operation is followed by a read-out (R). The width of all pulses is 500 ns. Vice versa for ERS sweep.

Fig. 5 – *VT* shift due to incremental program (a) and erase (b) pulses. Abrupt *VT* jumps are present at two distinct *VG*, which correspond to two different coercive fields *EC.*

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| a) | **5** | **1)** | **3**  **|VERS| [V]** | **4** | VT [V] | b) |  | c) | **5** | **3** | **VPRG [V]** | **4** | VT [V] |
| **Reference VPRG [V]** | **0.4** | **1)** | **0.4** |
| **4.5** | **Reference |VERS| [V]** | **4.5** |
| **0.3** | **0.3** |
| **4** | **0.2** | **2)** | **4** | **0.2** |
| **3.5** | **3.5** |
| **0.1** | **0.1** |
| **3** | **2)** | **0** | **3)** | **3** | **0** |
| **-0.1** | **-0.1** |
| **2.5** | **2.5** |
| **-0.2** | **-0.2** |
| **3)** |
| **2**  **2** | **5** | **2**  **2** | **5** |

Fig. 6 – *VT* switching matrices for ERS (a) and PRG (c) sweep. *VT* degradation in bottom-right corners is due to parasitic charge trapping. Three significant regions of (a) are highlighted in (b), showing *VT* vs. *|VERS|* traces with two (1), one (2) and no (3) *VT* jumps.

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| --- | --- | --- | --- |
| **|VERS| [V]** | **5** | MW [V] |  |
| **4.5** | **0.6** |
| **4** | **0.4** |
| **3.5** |
| **3** | **0.2** |

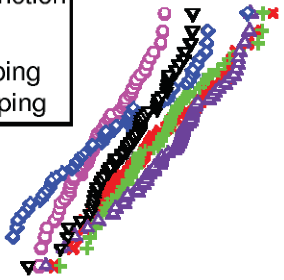
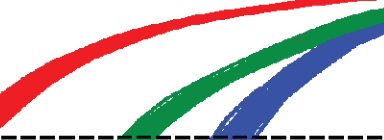
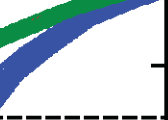
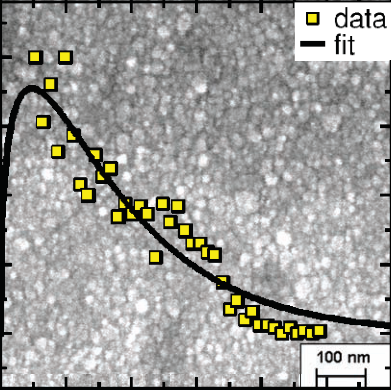
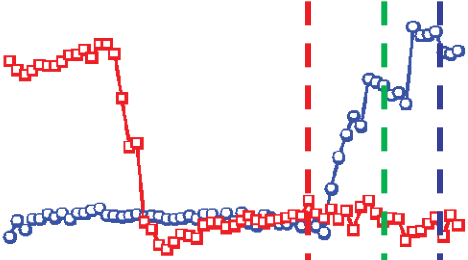
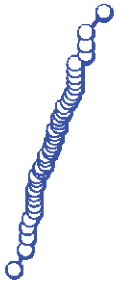
**2.5**

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| --- | --- | --- | --- | --- | --- |
| **2**  **2** | **3** | **VPRG [V]** | **4** | **5** | **0** |

Fig. 7 – MW switching matrix: two consecutively switching domains identified by dashed squares. Stars indicate the PRG and ERS limit values necessary for the domain switching.

Fig. 8 – FeFET structure implemented in TCAD: the two domain gate stack exhibits *VT* jumps similar to experimental observation in Fig. 5. More gradual switching events are due to the adopted Preisach model in the simulation.

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| a) | PRG |  |  | b) |  | c) |  |  |  |
|  |  |
|  |  |
| ERS |
|  |

Fig. 9 – a) Cell with three *VT* levels and b) their corresponding *ID-VG* curves sampled in 50 cycles of PRG operation at 4V and erase

operations at -4.5V and -4.85V (indicated by vertical lines in (a)). c) extracted *VT* levels show a very low cycle-to-cycle variability.



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5 Fig. 10 – Three *VT* states are separated and stable up to 10

program +4V/500ns and erase -4.85V/500ns cycles.

Fig. 11 – Retention of the three *VT* states measured up to 10 h at room temperature. No domain back-switching occurs. Initial

transient behavior is most probably due to the de-trapping of

parasitic charge.

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| ERS | PRG |  | | | | a) |  | b) | | | |
| Fig. 12 – Distribution of *VG* levels for PRG and ERS operation at which the | | Fig. 13 – *VT* vs. *VPRG* trace for a 80x90 nm² device exhibits an increased | | | | Fig. 14 – a) Top-view TEM image of | | | | |
| polycrystalline Si:HfO2 layer after removing the gate electrode and b) | | | | |
| first *VT* jump occurs. Data extracted from 60 devices. | | number of single domain switching | | | |
| events (shown by arrows) compared | | | | top-view SEM image of 10 nm FE | | | | |
|  | | to the 80x30 nm² device of Fig. 5. | | | | film, | the | extracted | grain | size |
| distribution and its Poisson fit. | | | | |
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| References: | | | | |
|  |  | | |
| [1] J. Müller *et al*., *VLSI*, 25-26, 2012. | | | | |
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| [2] JEDEC, JESD28A, 2012. | | | | |
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| [3] M. Kohli *et al*., *APL*, **72**, 1998. | | | | |
|  | | | | [4] Y. Tan *et al*., *Nat.Sci. Rep.* 5, | | | | |
| (2015) | | | | |
| [5] S. Salahuddin *et al*., *Nano Lett.*, | | | | |

8(2), 405-410, 2008

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| Fig. 15 – Switching voltage vs. grain | Fig. | 16 | – | Various | | processing | This work was supported in part by |
| radius for a 10nm thick FE HfO2 film derived from the grain size and | conditions can be used to tailor the | | | | | | the EFRE fund of the European |
| dependence | | of | | the | polarization | Commission within the scope of |
| voltage jump distributions shown in | reversal barrier on grain size, directly | | | | | | technology development and in part |
| Fig.s 14 and 12, respectively. | impacting MW. | | | | | | by the Free State of Saxony. |
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