IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 12, DECEMBER 2013 4199

From MFM Capacitors Toward Ferroelectric   
Transistors: Endurance and Disturb Characteristics of HfO2-Based FeFET Devices

Stefan Mueller, Johannes Müller, *Graduate Student Member, IEEE*, Raik Hoffmann, Ekaterina Yurchuk, Till Schlösser, Roman Boschke, Jan Paul, Matthias Goldbach, Tom Herrmann, Alban Zaka,   
Uwe Schröder, and Thomas Mikolajick, *Senior Member, IEEE*

***Abstract*—Ferroelectric Si:HfO2 has been investigated start-**

**ing**  **from**  **metal–ferroelectric–metal**  **(MFM)**  **capacitors**  **over**

**metal–ferroelectric–insulator–semiconductor (MFIS) and finally**

**ferroelectric field-effect-transistor (FeFET) devices. Endurance**

**characteristics and field cycling effects recognized for the mater-**

**ial itself are shown to also translate to highly scaled 30-nm FeFET**

**devices. Positive-up negative-down as well as pulsed *Id*–*Vg***

**measurements illustrate how ferroelectric material characteristics**

**of MFM capacitors can also be identified in more complex**

**MFIS and FeFET structures. Antiferroelectric-like characteris-**

**tics observed for relatively high Si dopant concentration reveal**

**significant trapping superimposed onto the ferroelectric memory**

**window limiting the general program/erase endurance of the**

**devices to 104cycles. In addition, worst case disturb scenarios**

**for a VDD/2 and VDD/3 scheme are evaluated to prove the**

**viability of one-transistor memory cell concepts. The ability**

**to tailor the ferroelectric properties by appropriate dopant**

**concentration reveals disturb resilience up to 106disturb cycles**

**while maintaining an ION to IOFF ratio of more than four orders**

**of magnitude.**

***Index***  ***Terms*—Disturb,**  **embedded**  **memory,**  **endurance,**

**ferroelectric field-effect-transistor (FeFET), V**DD**/3 scheme.**

I. INTRODUCTION

**T** HE ability to tailor HfO2 to become ferroelectric by using

appropriate dopant species and annealing conditions

[1]–[4] has finally enabled CMOS-compatible manufacturing

Manuscript received January 26, 2013; revised August 15, 2013; accepted

September 23, 2013. Date of publication October 7, 2013; date of current

version November 20, 2013. This work was supported in part by the

EFRE fund of the European Commission within the scope of technology

development and in part by the Free State of Saxony under Project HEIKO.

The review of this paper was arranged by Editor A. M. Ionescu.

S. Mueller, E. Yurchuk, and U. Schröder are with NaMLab gGmbH, Dresden

01187, Germany (e-mail: stefan.mueller@namlab.com; ekaterina.yurchuk@

namlab.com; uwe.schroeder@namlab.com).

J. Müller, R. Hoffmann, and J. Paul are with Fraunhofer CNT, Dresden

01099, Germany (e-mail: johannes.mueller@ieee.org; raik.hoffmann@

cnt.fraunhofer.de; jan.paul@cnt.fraunhofer.de).

T. Schlösser, R. Boschke, M. Goldbach, T. Herrmann, and

A. Zaka are with Globalfoundries Dresden Module One LLC & Co.

KG, Dresden 01109, Germany (e-mail: till.schloesser@infineon.com;

roman.boschke@ globalfoundries.com; matthias.goldbach@globalfoundries

.com; tom.herrmann@globalfoundries.com; alban.zaka@globalfoundries.com).

T. Mikolajick is with the NaMLab gGmbH, Dresden 01187, Ger-

many, and also with the Institute of Semiconductors and Microsystems

at Technische Universität Dresden, Dresden 01187, Germany (e-mail:

thomas.mikolajick@namlab.com).

Color versions of one or more of the figures in this paper are available

online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2013.2283465

of highly scaled ferroelectric field effect transistors (FeFETs) down to a 28-nm ground rule [5], [6]. Compared with classical ferroelectric materials used for FeFET devices [7], [8], HfO2 as novel ferroelectric is very promising for nonvolatile data storage especially because it is integratable into established high-*k* metal-gate (HKMG) process flows. Furthermore, the ferroelectric characteristics such as remanent polarization and coercive field but also the type of nonlinear polarization behavior (para-, anti-, or ferroelectric) can be influenced by various parameters, i.e., dopant species/concentration, film thickness, or annealing temperature [1]–[4], [9].

In this paper, it is shown that variations in ferroelectric properties using different dopant concentrations (various molar concentrations of SiO2 inside the HfO2 host lattice) are not limited only to standard MFM-capacitor structures but also translate to more complex structures such as MFIS capacitors or FeFET devices. The influence of varying material character-istics on important memory properties such as program/erase endurance and disturb resilience is investigated using predomi-nantly pulsed electrical characterization to additionally deepen the understanding of transient effects occurring in HfO2-based ferroelectric devices.

II. EXPERIMENTS

Electrical characterization was first carried out on MFM-capacitor structures, which were deposited on highly doped silicon substrates. A 10-nm TiN bottom electrode was man-ufactured by pulsed chemical vapor deposition (CVD) using the precursor TiCl4 and NH3 at a thermal budget of 450 °C for 3 h. Atomic layer deposition was then used for processing of the 10-nm Si-doped HfO2 layer possessing different molar concentrations of 5.7-, 4.5-, and 3.5-mol% SiO2 depending on the chosen pulse ratios of the precursors HfCl4 and SiCl4. Afterward, a covering TiN top electrode was deposited at the same processing conditions as previously mentioned for the bottom electrode. A postmetallization rapid thermal anneal step (1000 °C for 1 s) was used to emulate the conditions of source/drain junction anneals most appropriately. There-after, platinum dots (104*µ*m2*)* were evaporated through a shadow mask finally serving as a hard mask for etching the TiN top electrode and by that achieving proper MFM geometries. Precisely, the same Si:HfO2 layers were also integrated into a standard CMOS test chip using a 28-nm

0018-9383 © 2013 IEEE

4200 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 12, DECEMBER 2013

ground rule. This again shows the suitability of this approach for, e.g., embedded applications since no severe changes to an existing HKMG logic process need to be undertaken. The major difference between MFM and transistor test structures was that the functional layers of the transistor and MFIS devices were deposited onto nitrided SiO2 and that the top electrode was deposited at room temperature using physical vapor deposition (PVD) instead of CVD. The thermal budget during source/drain junction anneal was, however, comparable with the one used for MFM capacitors and in general has the most significant influence on the ferroelectric characteristics (leaving aside the right doping concentration, which had been chosen identical for all test structures). By shorting source and drain regions, transistors can be operated as MFIS capacitor structures (2·103*µ*m2*)* and serve as transition devices between MFM and FeFET structures.

Electrical characterization in general was carried out using a Keithley SCS-4200 semiconductor characterization system possessing a two-channel pulse-measurement unit. Hysteresis measurements were carried out using an aixACCT TF Ana-lyzer 3000 measurement system.

III. RESULTS AND DISCUSSION

To analyze the effect of different silicon content incorpo-rated in the HfO2 host lattice, hysteresis as well as endurance measurements up to 106cycles were performed on MFM-capacitor structures (Fig. 1).

As shown in this figure, increased amounts of silicon incor-poration led to clear antiferroelectric-like polarization [10] behavior with no remanent polarization after the removal of the electric field. For 4.5-mol% SiO2 content, it became obvious that the properties were right in between ferroelectric and antiferroelectric-like. The ferroelectric hysteresis with remanence was superimposed onto an antiferroelectric-like hysteresis without remanence. The most pronounced ferro-electric properties could be observed for the smallest dopant concentrations of 3.5-mol% silicon. This behavior is known to occur for the mentioned dopant concentrations and can be attributed to a gradual transition from the tetragonal to a proposed orthorhombic crystallographic phase of doped HfO2 [2].

When cycled at the measurement amplitude of 3 MV/cm using pulsewidths of 10 *µ*s (not parasitically affected by RC delay), the polarization characteristics of all samples showed a field cycling-induced transition toward increased remanent polarization and more pronounced ferroelectric properties in general. This conditioning effect, sometimes also called wake-up, has similarly been observed for classical ferro-electrics like PZT [11], [12].

Whereas the remanent polarizations of the 4.5- and 3.5-mol% samples are approximately the same after 106 endurance cycles, the values of the coercive fields clearly differ. Theoretically, this would directly correspond to an increased memory window of the FeFET since its magnitude the coercive field and *d* to the thickness of the ferroelectric can be approximated by ∼2·*Ec* · *d* whereas *Ec* corresponds to incorporated into the gate-stack [13]. This represents an impor-tant reference for memory window measurements, which had

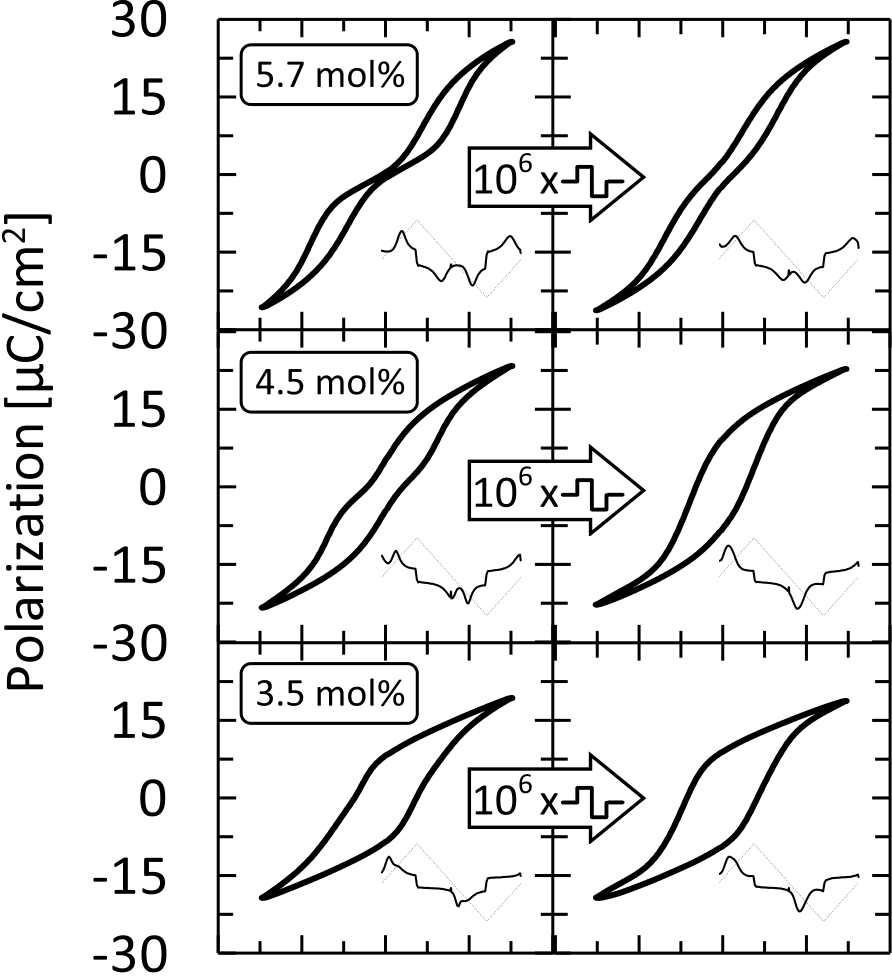






Fig. 1. Polarization hysteresis of 10-nm Si:HfO2 MFM capacitors depending on the amount of incorporated silicon dopant. A transition from antiferroelectric-like to clear ferroelectric hysteresis is visible for lower doping concentrations. Field cycling up to 106bipolar voltage cycles at 3 MV/cm improves the ferroelectric characteristics. Corresponding current versus time transients are shown as inset.

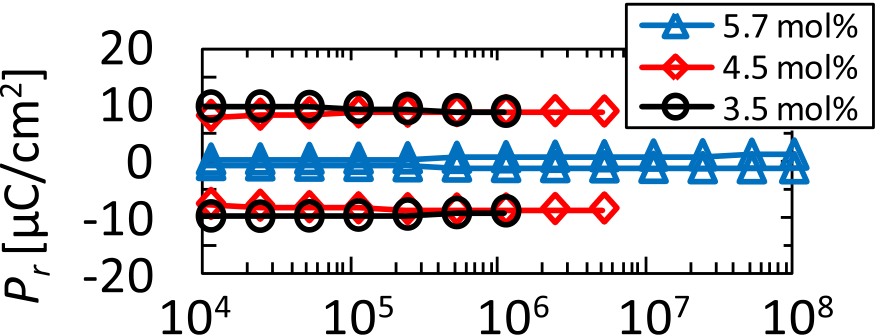




Fig. 2. MFM-endurance characteristics for the three respective dopant concentrations. For the 3.5- and 4.5-mol% samples, endurance is rather limited by hard dielectric breakdown than by typical ferroelectric fatigue. The 5.7-mol% sample shows no breakdown even after 108stress cycles.

been performed on long- and short-channel FeFET devices. Furthermore, the effect of nonvanishing remanence for the field cycled 5.7-mol% sample also served as an essential reference for the transistor characterization.

As shown by the field cycled hysteresis measurements, all samples were able to withstand 106bipolar voltage cycles at 3 MV/cm, which can generally be considered as a threshold for the capability of a material to serve as nonvolatile data storage layer. Hence, cycling was continued until 108cycles to analyze endurance properties until hard electrical breakdown (Fig. 2).

While capacitors with pronounced ferroelectric proper-ties (3.5- and 4.5-mol% SiO2*)* show breakdown after about

MUELLER *et al.*: FROM MFM CAPACITORS TOWARD FERROELECTRIC TRANSISTORS 4201

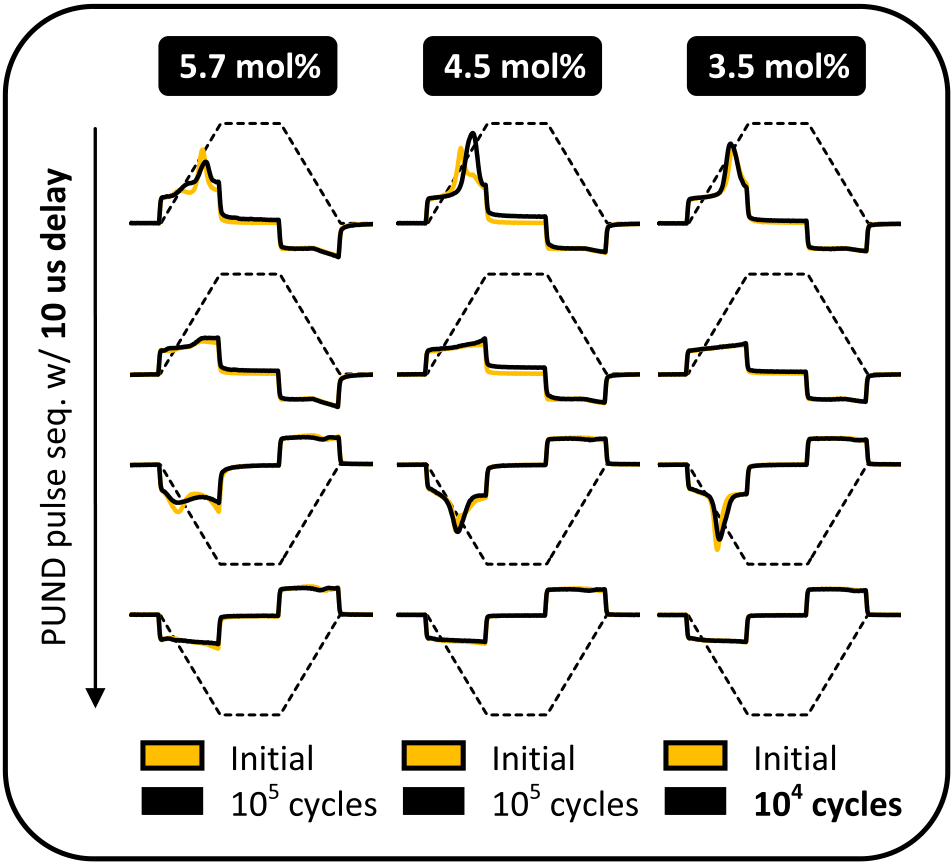


Fig. 3. PUND measurements for MFIS capacitors having the same ferroelec-tric layer incorporated, as shown for MFM capacitors in Fig. 1. The effects of field cycling are comparable with results obtained for MFM capacitors. Endurance however does not exceed 105cycles and is limited by breakdown of the gate-stack.

106cycles, higher dopant concentrations lead to improved endurance characteristics showing no breakdown even after 108stress cycles. This behavior is known from piezoelectric ceramics and can be attributed to increased mechanical stress accompanying a larger remanent polarization [14].

To analyze these endurance and field cycling properties on a fully integrated CMOS test chip, MFIS structures as described before were first chosen to be exposed to the same stress signal (10-*µ*s pulsewidth with 10-*µ*s rise and fall time). In the following, all considerations refer to n-FeFET transistors.

In general, hysteresis measurements on MFIS structures are not suitable to draw proper conclusions since accumulation and weak inversion would also be included in the integrated current response, i.e., the measured polarization. The best way to compare the switching characteristics of MFIS with MFM structures is by a pulsed measurement, more specifically a positive-up negative-down (PUND) test [15]. As shown by the name itself, two succeeding pairs of voltage pulses with oppos-ing polarity lead to current responses representing switching and nonswitching portions of the ferroelectric hysteresis.

Even though the MFIS capacitors shown in Fig. 3 do not possess a proper bottom electrode and will therefore show different current responses as compared with MFM capac-itors, various characteristics of the current response reflect previously observed field cycling characteristics. First of all, the current response is significantly more pronounced for the ferroelectric compositions (3.5- and 4.5-mol% SiO2*)* than for the antiferroelectric-like composition of 5.7-mol% SiO2. The most severe change of current response with respect to field

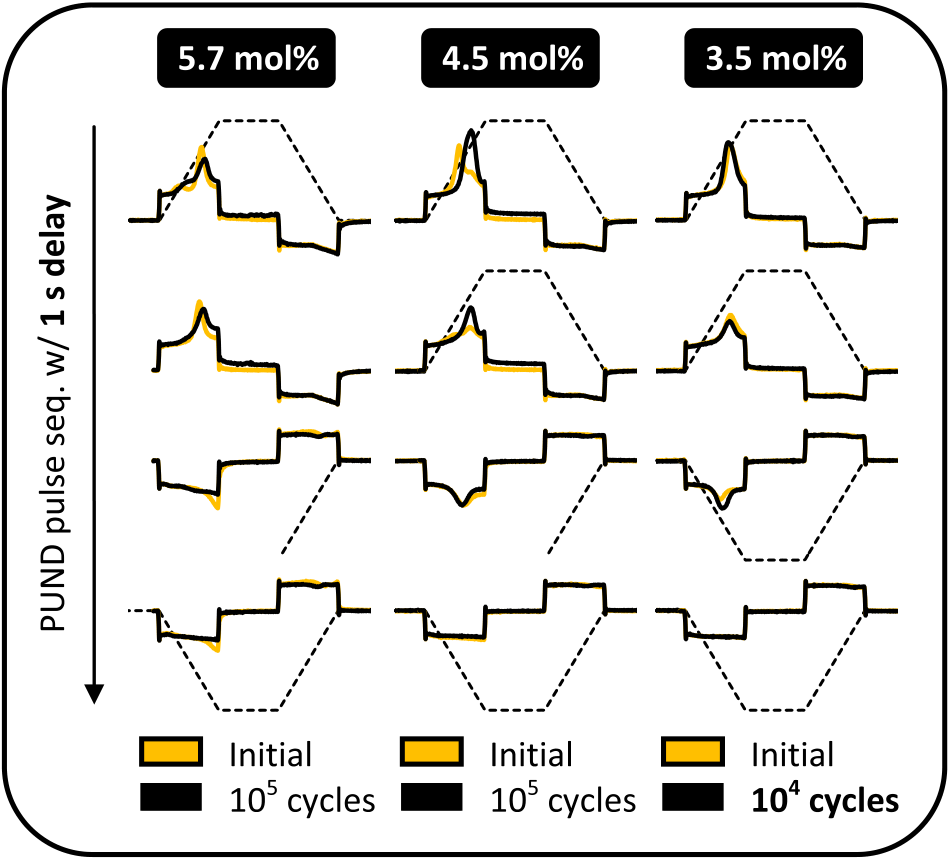


Fig. 4. PUND measurements for MFIS capacitors with increased delay times of 1 s. In general, significantly increased switching/detrapping currents can be observed for the up pulse. Accordingly, the down pulse is reduced in amplitude as compared with measurements performed with 10-*µ*s delay time.

105stress cycles. The tendency that compositions showing most pronounced ferroelectric properties are prone to early breakdown however remained since the 3.5-mol% composition could only endure 104bipolar voltage cycles. This degradation can be understood in terms of increased interfacial field stress for films possessing pronounced ferroelectric properties/large remanent polarizations [16].

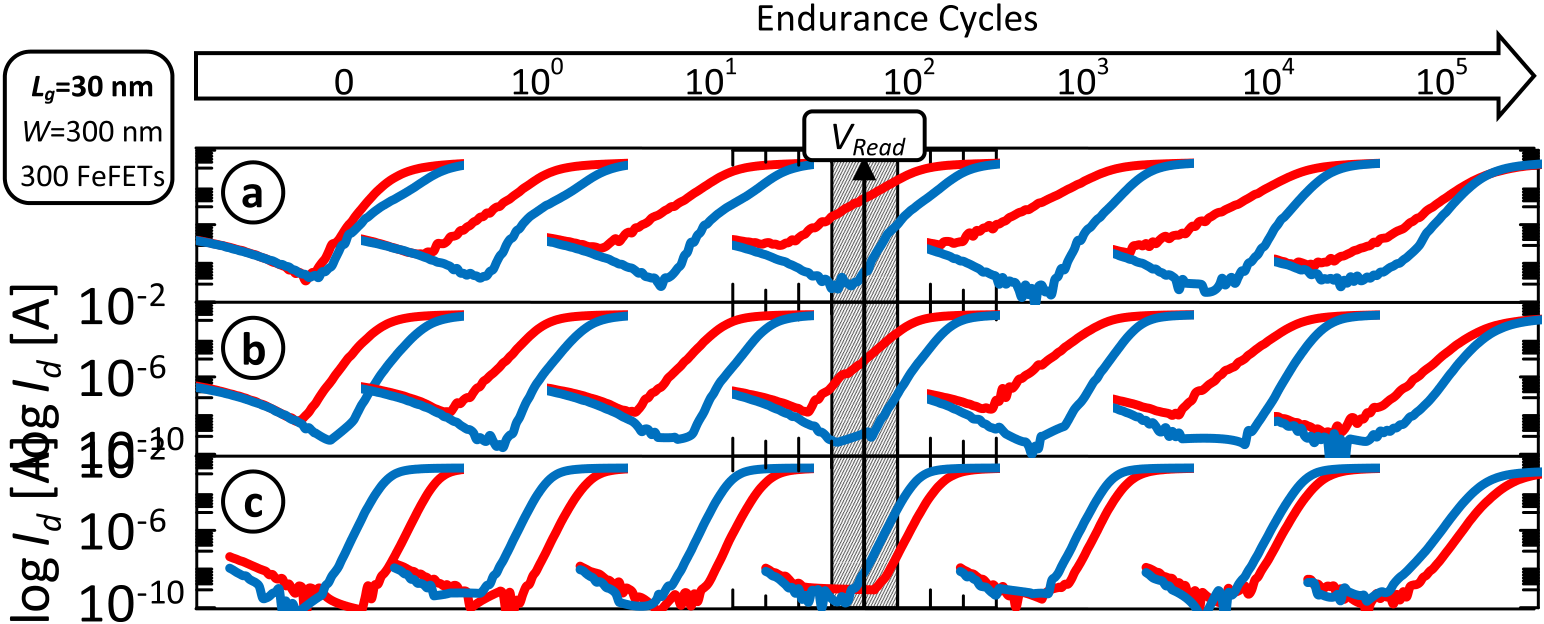
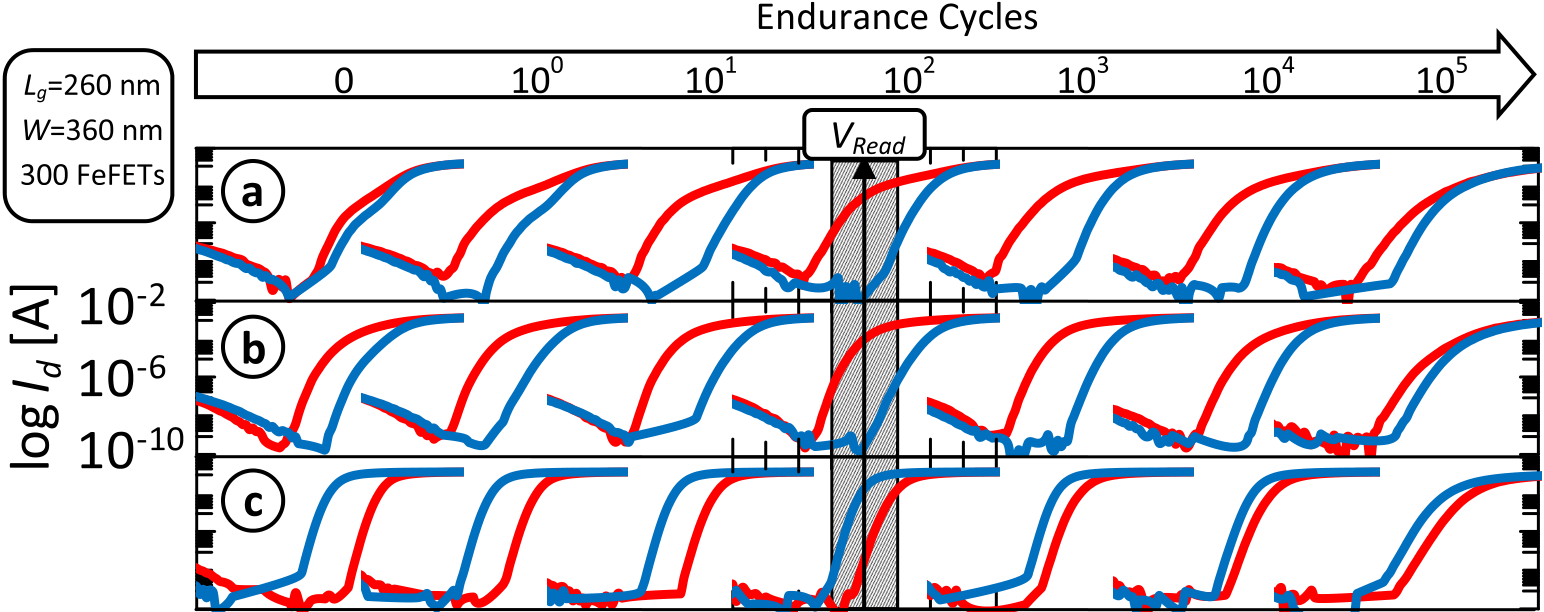
Furthermore, using pulsewidths/transition times of 10 *µ*s and a delay time of 10 *µ*s, it was not possible to identify the proper current response corresponding to the backswitching of the antiferroelectric-like composition (a current pulse should appear for the up pulse). Hence, effects of relaxation, both for ferroelectric and potentially antiferroelectric domains as well as detrapping of electrons were investigated by increasing delay times in between the pulse sequence (Fig. 4).

By increasing the delay times up to 1 s, the current response corresponding to the positive pulse remained almost con-stant whereas the one of the up pulses changed significantly, i.e., a significant current peak could be observed. Furthermore, the response current of the negative pulse was accordingly reduced in amplitude by the same amount. These effects can be attributed to the relaxation of the ferroelectric domains due to the internal depolarization fields occurring for this type of transistor eventually resulting in an initially fast retention loss [17], [18]. Even though this represents a major challenge for ferroelectric transistors, retention could still be extrapo-lated to 10 years if the devices were based on Si:HfO2 [6]. Moreover, retention characteristics for the Si:HfO2 ferroelec-tric itself were shown to be very stable even at elevated

cycling was detected for the intermediate composition of 4.5- temperatures [19].

mol% SiO2. This had also been the case for MFM capacitors as it was shown in Fig. 1. However, certain characteristics need to be investigated further. Independent of the doping composi-tion, all MFIS capacitors were not able to withstand more than

Furthermore, trapping and detrapping of charge carriers can also lead to similar effects. Increasing the delay times enables trap centers to release charge carriers, which can again be filled effectively resulting in a similar current peak to occur for the



4202 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 12, DECEMBER 2013





Fig. 5. Pulsed *Id*–*Vg* characterization for both long-channel and short-channel FeFETs. Doping concentrations of (a) 3.5 and (b) 4.5 mol% both show a

shift to more negative *Vt* values after the application of a positive programming pulse (red) and a shift toward more positive *Vt* values after the application

of a negative erase pulse (blue). (c) 5.7-mol% composition shows an inverted memory window showing only trapping related phenomena. For short-channel

devices, strong subthreshold-slope degradation is visible, especially after a programming pulse.

up pulse. Nevertheless, hole trapping or electron trapping from the gate side can be ruled out since the current response of the down pulse stays ideally dielectric (constant current during voltage change) independent of the delay time. In addition, it has to be mentioned that similar studies had also been performed for MFM capacitors. However, an identical change in delay time did not lead to any significant change of the respective current responses. Hence, it can be concluded that the relaxation characteristics are uniquely present only for devices based on FeFET architectures.

To investigate the significance of electron trapping superim-posed on the ferroelectric switching, the evolution of *Id*–*Vg* characteristics of FeFETs exposed to the same stress sequence

characteristics due to the oppositely oriented *Vt* shift caused by ferroelectricity as compared with *Vt* shifts caused by electron trapping. Because after a positive gate pulse, the remanent polarization of the ferroelectric causes the inversion layer to be maintained, a hysteretic *Id*–*Vg* sweep always runs counter clockwise for FeFETs as compared with clockwise for charge trapping devices. However, a superimposed existence of electron trapping is clearly visible for FeFET devices, which incorporate a silicon concentration in the HfO2 corresponding to the antiferroelectric-like composition of 5.7 mol%. Here, the *Vt* shift is identical to n-channel charge trapping devices, i.e., after applying a positive programming amplitude, the threshold voltage shifts to more positive values due to electron trapping.

was analyzed. Hence, if the ferroelectric switching would not be superim-

Both long-channel as well as short-channel transistors (*Lg* = 260 nm, *W* = 360 nm, and *Lg* = 30 nm, *W* = 300 nm, respectively) were characterized using a pulsed *Id*-*Vg* char-acterization capable of analyzing the respective importance of those overlapping effects. As shown in Fig. 5(a) and (b),

posed by a 1 V charge trapping window, the ferroelectric memory window would be close to the theoretically possible value of 2 × 1 MV/cm × 10 nm, i.e., 2 V. Interestingly, for both long-channel as well as short-channel FeFET devices of composition (c), the memory window van-

|  |  |  |
| --- | --- | --- |
| the ferroelectric switching clearly dominates the | *Id*–*Vg* | ishes, which can well be explained by the observations made |

MUELLER *et al.*: FROM MFM CAPACITORS TOWARD FERROELECTRIC TRANSISTORS 4203

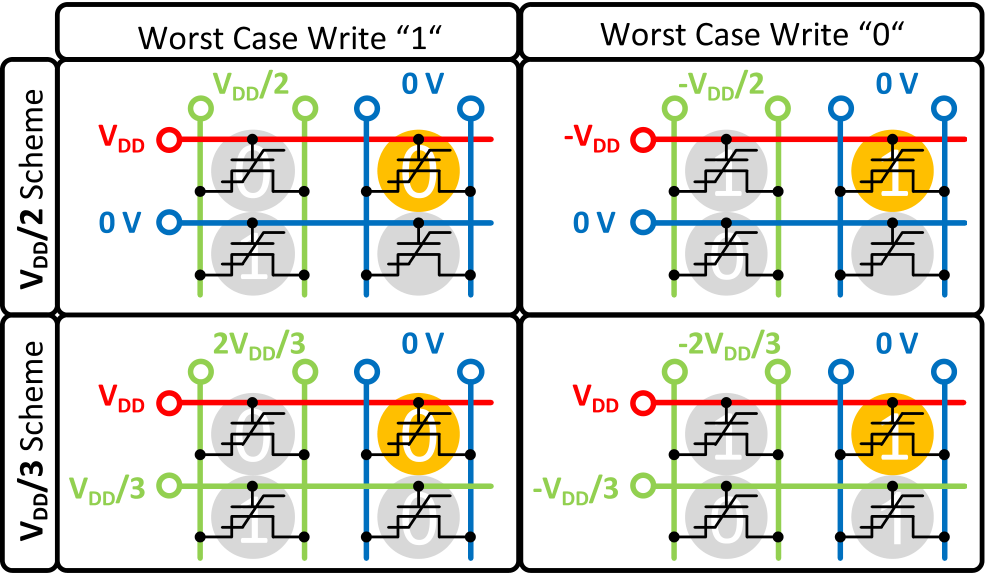


Fig. 6. Worst case scenarios for writing either 1 or 0 states to cell (1,2) in an AND architecture of FeFET devices. For a *V*DD/2 inhibit scheme, less neighboring signal lines have to be precharged. A *V*DD/3 scheme provides minimization of disturb voltages.

for MFM capacitors at the beginning. As mentioned, these antiferroelectric-like layers still show a minor amount of rema-nent polarization, i.e., a ferroelectric fraction with increasing cycling, which can explain the closure of the memory window due to the two competing effects of ferroelectricity and charge trapping. Referring also back to Fig. 4, taking a closer look at the switching currents after 105cycles reveals that fractions of the switching current corresponding to the positive pulse do not reappear for the up pulse, which further supports

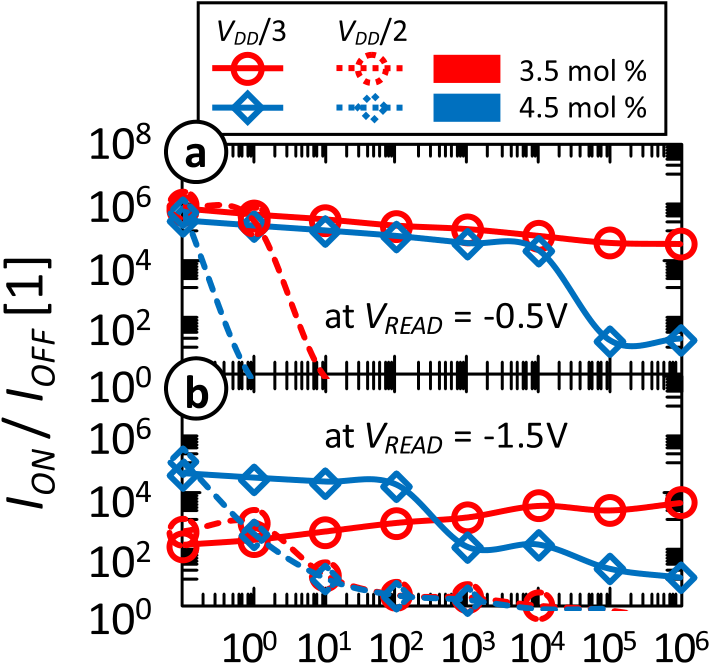




Fig. 7. Remaining *I*ON/*I*OFF ratios for (a) long-channel and (b) short-channel devices. FeFET devices having the smallest amount of silicon incorporated show the best resilience with respect to disturb. The *V*DD/2 scheme is not capable of inhibiting disturb for pulsewidths of 10 *µ*s.

previous publications [6]. These conditions were then used for analyzing the viability of 1T memory cell concepts. One major concern for, e.g., an AND-cell architecture is represented by program and erase disturb. Worst case scenarios are shown in

the hypothesis of increasing remanence with increasing field Fig. 6.

cycling for molar concentrations of 5.7 mol%. For the ferro-electric compositions (a) and (b) the memory window is rather similar in size and closes after 105endurance cycles. It has to be mentioned that the degradation occurs primarily for the programmed state, i.e., the threshold voltage cannot be shifted toward more negative values whereas the erased state stays almost constant. This represents an effect also observed during PUND measurements on MFIS capacitors. There, the onset of gate-stack degradation also took place due to increased current flow during positive constant voltage stress of the trapezoidal

Depending on the inhibit scheme, different voltages have to be applied to neighboring word-, bit- and sourcelines. If a *V*DD/2 scheme is used, neighboring source- and bitlines have to be exposed to half of the programming or erase voltage, respectively (first row in Fig. 6). The effective voltage disturbing the cells in a worst case scenario is half of the program/erase voltage. This can be improved if also neighbor-ing wordlines are precharged to 1/3 *V*DD effectively reducing the disturb voltage to one-third of the program/erase voltages (second row in Fig. 6). The drawback of this approach is that

voltage pulses. the precharge for inhibiting program/erase disturb increases

Furthermore, short-channel devices showed similar charac- power consumption.

teristics whereas the degradation of the subthreshold slope after a positive program pulse was much more severe (Fig. 5). Since all the devices were processed with strong source drain extension diffusion, short-channel devices were normally on. Hence, control over the channel region becomes significantly degraded especially when the channel is further enhanced as is the case after a program pulse.

Another goal of this paper was to extract the most appro-priate operating conditions with respect to one-transistor (1T) cell concepts. Therefore, the intervals of potential read volt-ages were determined from the pulsed *Id*–*Vg* characteristics, as shown in Fig. 5. For long-channel devices, the largest

0.5 V]. A 1 V interval was also assigned to the short-*I*ON/*I*OFF ratios were visible for the interval of [−0.5 V;

channel FeFETs however shifted by 1 V to more negative values due to the mentioned *Vt* rolloff. Program/erase voltages of ±5 V for long-channel and +4/−6 V for short-channel devices, respectively, show the largest memory windows and were determined by pulse matrix measurements analogous to

To estimate if such an architecture and inhibiting scheme would be applicable for FeFET transistors, either a 1 or a 0 state was written to long- and short-channel devices and respective *V*DD/2 and *V*DD/3 disturb signals of opposite polar-ity were applied up to 106times. After disturbing the states, the *I*ON and *I*OFF current were read out in the interval extracted from pulsed *Id*–*Vg* characterizations. To maintain consistency with all previously performed measurements, program/erase as well as disturb pulsewidths and rise times were set to 10 *µ*s. For FeFETs possessing a 3.5-mol% SiO2 composition, it could be shown that for long-channel devices, a *V*DD/3 scheme can maintain a proper *I*ON/ *I*OFF ratio of more than four orders of magnitude even after 106disturb cycles (Fig. 7). This observation can most likely be attributed to the increased coercive field of that specific material composition (compare Fig. 1).

The *V*DD/2 scheme in comparison is not capable of inhibit-ing disturb at pulsewidths of 10 *µ*s since states are lost almost instantaneously for long-channel and gradually for

4204 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 12, DECEMBER 2013

short-channel devices. It is further interesting to note that short-channel FeFET devices of 3.5-mol% composition seem to improve their resilience with respect to disturb with increas-ing amount of disturb cycles. Even though the devices have been treated with 100 cycles in advance to exclude condi-tioning effects, this behavior was nonetheless attributed to a widening of the memory window with cycling, as shown in Fig. 5. Especially, short-channel devices of that respective composition show conditioning effects up to 103cycles.

In the future, similar characteristics will have to be inves-tigated on integrated FeFET memory arrays. Due to reduced *RC* parasitic, disturb and endurance characteristics might then be analyzed for pulsewidths even in the nanosecond range.

IV. CONCLUSION

Ferroelectric Si:HfO2-based MFM and MFIS capacitors as well as FeFETs were investigated with focus on endurance and disturb characteristics relevant for memory arrays. Com-positional changes of the Si:HfO2 were shown to influence these characteristics significantly due to changes occurring in the ferroelectric properties themselves. Improved ferroelectric properties with field cycling were well transferrable from MFM toward MFIS capacitors and finally to FeFET devices. Electron trapping from the channel region was identified as the most probable reason for degraded endurance performance of MFIS capacitors and ferroelectric transistors as compared with MFM capacitors. Pulsed *Id*–*Vg* measurements could illustrate how the ferroelectric memory window evolves with cycling and that a significant trapping window is superim-posed on ferroelectric switching. Endurance characteristics are therewith limited to 104cycles. Hence, it can be concluded

[7] S. Sakai and R. Ilangovan, “Metal-ferroelectric-insulator-semiconductor memory FET with long retention and high endurance,” *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 369–371, Jun. 2004.

[8] X. Zhang, M. Takahashi, K. Takeuchi, and S. Sakai, “First 64 kb ferroelectric-NAND flash memory array with 7.5 V program, 108 endurance and long data retention,” in *Proc. Int. Conf. Solid State Devices Mater.*, 2011, pp. 975–976.

[9] E. Yurchuk, J. Müller, S. Knebel, J. Sundqvist, A. P. Graham, T. Melde, *et al.*, “Impact of layer thickness on the ferroelectric behaviour of silicon doped hafnium oxide thin films,” *Thin Solid Films*, vol. 533, pp. 88–92, Apr. 2013.

[10] C. Kittel, “Theory of antiferroelectric crystals,” *Phys. Rev.*, vol. 82, no. 5, pp. 729–732, Jun. 1951.

[11] M. Kohli and P. Muralt, “Poling of ferroelectric thin films,” *Ferro-* *electrics*, vol. 225, no. 1, pp. 155–162, 1999.

[12] M. Kohli, P. Muralt, and N. Setter, “Removal of 90° domain pinning in (100) Pb(Zr0*.*15Ti0*.*85)O3 thin films by pulsed operation,” *Appl. Phys. Lett.*, vol. 72, no. 24, pp. 3217–3219, Apr. 1998.

[13] M. Fitsilis, “Scaling of the ferroelectric field effect transistor and pro-gramming concepts for non-volatile memory applications (dissertation style),” Ph.D. dissertation, Faculty Electr. Eng. Inf. Technol., RWTH Aachen Univ., Aachen, Germany, 2005.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| [14] M. | A. | Ugryumova, | I. | P. | Golyamina, | G. | G. | Pisarenko, | and |

A. K. Gerikhanov, “Influence of polarization on the fatigue of a piezoceramic,” *Strength Mater.*, vol. 13, no. 7, pp. 925–927, Jul. 1981. [15] J. T. Evans, “Characterizing ferroelectric materials,” in *Proc. IEEE ISAF*, 2010, pp. 1–123.

[16] S. Mueller, J. Müller, E. Yurchuk, A. Zaka, T. Herrmann, S. Slesazeck, *et al.*, “Performance investigation and optimization of Si:HfO2 FeFETs on a 28 nm bulk technology,” in *Proc. ISAF*, to be published.

[17] T. P. Ma and J.-P. Han, “Why is nonvolatile ferroelectric memory field-effect transistor still elusive?” *IEEE Electron Device Lett.*, vol. 23, no. 7, pp. 386–388, Jul. 2002.

[18] J. Müller, T. S. Böscke, U. Schröder, R. Hoffmann, T. Mikolajick, and L. Frey, “Nanosecond polarization switching and long retention in a novel MFIS-FET based on ferroelectric HfO2,” *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 185–187, Feb. 2012.

[19] S. Mueller, J. Müller, U. Schröder, and T. Mikolajick, “Reliability char-acteristics of ferroelectric Si:HfO2 thin films for memory applications,”*IEEE Trans. Device Mater. Rel.*, vol. 13, no. 1, pp. 93–97, Mar. 2012.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| that Si:HfO2-based FeFET endurance is currently limited by | | | | | | | | | | | | | | | | |  | **Stefan Mueller** received the joint master’s degree in |
| device architecture and not by ferroelectric material properties | | | | | | | | | | | | | | | | |
| microelectronics from Technical University Munich, |
| itself. Furthermore, it was shown that FeFET devices can | | | | | | | | | | | | | | | | | Munich, Germany, and Nanyang Technological Uni- |
| withstand *V*DD/3 disturb up to the tested 106disturb cycles | | | | | | | | | | | | | | | | | versity, Singapore, in 2011. |
| He joined NaMLab gGmbH, Dresden, Germany, in |
| while maintaining a sufficiently large *I*ON/*I*OFF ratio. | | | | | | | | | | | | | | | | |
| 2011, as a Ph.D. Student, on ferroelectric devices. |
| Due to this basic disturb resilience of Si:HfO2 FeFETs, | | | | | | | | | | | | | | | | |
| efforts | aiming | | at | very | | dense | | 1T-architectures | | | | | such | | | as |
| NAND | or | NOR | | arrays | | might | | enable | | | embedded | | | high- | | |
| density ferroelectric memories at state-of-the-art technology | | | | | | | | | | | | | | | | |
| nodes. | | | | | | | | | | | | | | | | |  | **Johannes Müller** (GSM’11) received the Diploma |
| REFERENCES | | | | | | | | | | | | | | | | | degree in applied natural science from Technical |
| University Freiberg, Freiberg, Germany. |
| He is currently leading the ferroelectric material |
| and device activities with Fraunhofer IPMS-CNT, |
| [1] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, | | | | | | | | | | | | | | | | |
| Dresden, Germany. |
| “Ferroelectricity in hafnium oxide thin films,” *Appl. Phys. Lett.*, vol. 99, | | | | | | | | | | | | | | | | |
| no. 10, pp. 102903-1–102903-3, Sep. 2011. | | | | | | | | | | | | | | | | |
| [2] T. S. Böscke, S. Teichert, D. Bräuhaus, J. Müller, U. Schröder, | | | | | | | | | | | | | | | | |
| U. | Böttger, | | *et* | *al.*, | “Phase | | transitions | | | in | ferroelectric | | | silicon | | |
| doped | | hafnium | | oxide,” | | *Appl.* | | *Phys.* | *Lett.*, | | vol. | 99, | | no. | 11, | |

pp. 112904-1–112904-3, Sep. 2011.

[3] J. Müller, U. Schroder, T. S. Boscke, I. Muller, U. Bottger, L. Wilde, *et al.*, “Ferroelectricity in yttrium-doped hafnium oxide,” *J. Appl. Phys.*, vol. 110, no. 11, pp. 114113-1–114113-5, Dec. 2011.

[4] S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, *et al.*, “Incipient ferroelectricity in Al-doped HfO2 thin films,” *Adv. Funct. Mater.*, vol. 22, no. 11, pp. 2412–2417, Jun. 2012.

[5] T. S. Böscke, J. Muller, D. Brauhaus, U. Schroder, and U. Bottger,“Ferroelectricity in hafnium oxide: CMOS compatible ferroelectric field effect transistors,” in *Proc. IEEE IEDM*, Dec. 2011, pp. 1–4.

[6] J. Müller, E. Yurchuk, T. Schlosser, J. Paul, R. Hoffmann, S. Muller, *et al.*, “Ferroelectricity in HfO2 enables nonvolatile data storage in 28 nm HKMG,” in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2012, pp. 25–26.

**Raik Hoffmann**, photograph and biography not available at the time of publication.

**Ekaterina Yurchuk**, photograph and biography not available at the time of publication.

**Till Schlösser**, photograph and biography not available at the time of publication.

**Roman Boschke**, photograph and biography not available at the time of publication.

|  |  |  |  |
| --- | --- | --- | --- |
| MUELLER *et al.*: FROM MFM CAPACITORS TOWARD FERROELECTRIC TRANSISTORS | | | 4205  **Uwe Schröeder** received the Doctoral degree from the University of Bonn, Bonn, Germany.  He joined Infineon formerly Siemens Semicon-ductor for DRAM capacitor development in the DRAM development alliance with IBM and Toshiba, Hopewell Jct., NY, USA, in 1997. |
|  | **Jan Paul** is currently pursuing the Ph.D. degree in |  |
| electrical engineering with the Dresden University |
| of Technology, Dresden, Germany. |
| His current research interests include the plasma |
| etch processing of new materials, especially for |
| scalable memory and transistor devices. |

**Matthias Goldbach**, photograph and biography not available at the time of

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| publication. |  | **Thomas Mikolajick** (SM’09) received the Ph.D. | | | | | | |
| **Tom Herrmann**, photograph and biography not available at the time of | degree from University Erlangen-Nuremberg, Erlan- | | | | | | |
| gen, Germany, in 1996. | | | | | | |
| He | is | the | Scientific | Director | with | NaMLab |
| gGmbH, Dresden, Germany. | | | | | | |
| publication. |
| **Alban Zaka**, photograph and biography not available at the time of publica- |
| tion. |