

Next-Generation Ferroelectric Memories Based on FE-HfO2

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***Abstract*—In recent years, and with the discovery of ferroelectricity in hafnium oxide, it was possible to scale down ferroelectric memory cells in both transistor and capacitor configurations. This study reports the latest advances for FE-HfO2-based memory cells and arrays. For the 1T FeFET memory approach, retention in the range of 10 μs up to 104 seconds was measured both after 102 and 104 endurance cycles. At room temperature, memory windows of 0.8 V and 0.7 V were extrapolated to ten years respectively. Moreover, a novel operating scheme for a 1T FeFET AND architecture is presented allowing for true random access operation of the array. With respect to capacitor-based memory cells, high aspect ratio ferroelectric trench capacitors are demonstrated which show proper memory characteristics up to 105 cells in parallel. In order to bring these concepts closer to commercialization, device statistics of larger amounts of memory cells have to be provided. For the first time, the functionality of small FeFET memory arrays is shown and the statistical distribution of memory characteristics is analyzed. We provide evidence that with the proper choice of material composition, device size and operating conditions, the realization of memory products utilizing HfO2-based FeFET arrays seems viable in the future.**

***Index Terms*—FE-HfO2, FeFET, FRAM, HKMG, memory array.**

I.INTRODUCTION

In 2011, ferroelectric behavior in doped hafnium oxide (FE-HfO2) was published for the first time [1]. Due to the fact that hafnium oxide was also introduced as gate oxide replacement back at that time, first publications could verify the functionality of FE-HfO2-based ferroelectric field effect transistors (FeFETs) [2]. In this transistor configuration, a binary state is encoded in a non-volatile fashion by use of the polarization state of the ferroelectric. That is, if the polarization is pointing towards the channel region, an inversion channel is created whereas accumulation is induced in case the polarization is pointing into the opposite direction (Fig. 1a).

Since the introduction of HfO2 at the 45 nm technology node, most of the succeeding technology generations today are utilizing hafnium oxide as gate dielectric. Due to this, in 2013 it was possible to demonstrate the world’s first 28 nm FeFET

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based on a high-k metal-gate process flow of semiconductor manufacturer Globalfoundries [3].

Besides the very appealing concept of a one-transistor (1T) based memory application like the FeFET, ferroelectric memories are nowadays actually commercialized as one-transistor one-capacitor (1T-1C) architectures. In this capacitor configuration, the binary state is again encoded in the polarization state of the ferroelectric, however, the read-out operation is destructive and based on the switching response of the capacitor (Fig. 1b).

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| a | *VG* | | | | | | b | *VPL* | | | | | **P** |
| 0 V | *VRead* | FE | **P** | or |
| 0 V | FE | Gate | | **P** | 0.1 V |
| **P** | or |
| Gate | | | | |
| Insulator | | | | | | Insulator | | | | |
| Source | Drain | | | | | Source | Drain | | | |
| Log Drain Current | | | | | | |Plateline Current| | | | | |

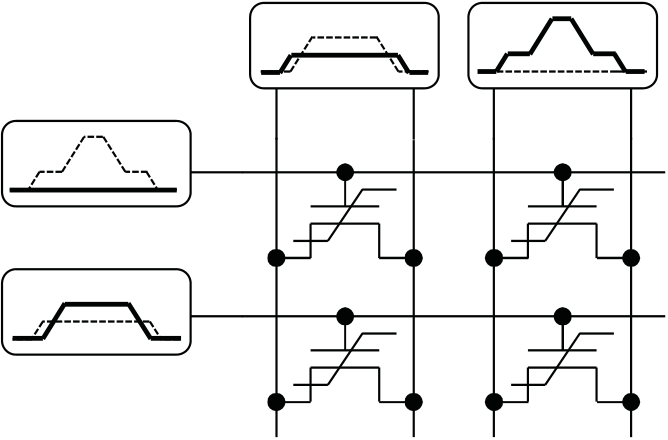
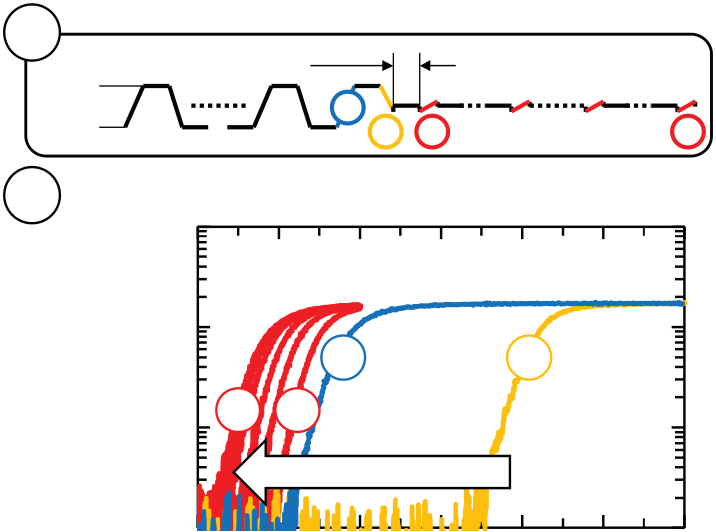
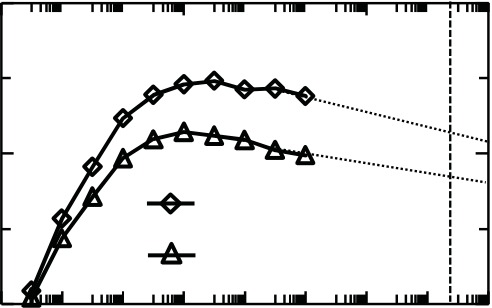
**P**

|  |  |  |
| --- | --- | --- |
| **P** | **P** | **P**  Plateline Voltage *VPL* |
| Gate Voltage *VG* | |

Fig. 1: Memory operation of 1T and 1T-1C FRAM. (a) In a 1T FeFET, the threshold voltage of the transistor depends on the polarization state of the ferroelectric. (b) For the 1T-1C architecture, the binary state is encoded in the magnitude of the switching current.

In the following paragraphs, the latest findings on both FeFET and capacitor memory cells will be presented. Finally, memory characteristics of small FeFET arrays are shown for the first time and shall support the commercialization of FE-HfO2-based memory applications.

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II.28 NM FEFET FOR 1TFRAM

28 nm FeFETs could be realized in the past by increasing the thickness and by doping of the HfO2 of standard high-k metal-gate (HKMG) logic transistors. Two of the most important memory characteristics, i.e. cycling endurance and data retention, were appropriately demonstrated [3]. However, for real memory applications it is essential to also ensure proper data retention after the device has endured a significant amount of stress cycles.

In order to set up a so called retention after endurance test, a special measurement procedure was implemented utilizing a Keithley SCS-4200 semiconductor analyzer equipped with one pulse-measurement-unit (PMU). A pulse train was created that was first stressing the device by continuous polarization reversal applying a ± 5 V / 10 μs bipolar gate voltage for 102 or 104 times while keeping the drain, source and bulk terminals grounded. The stress sequence ended with a negative gate voltage thereby inducing the high-*VT* state for the FeFET. This state was measured immediately after 10 μs using an *Id*-*Vg* sweep from -5 V up to 5 V gate bias (*Vd* = 100 mV) that lasted for 10 μs as well. After holding the gate voltage at 5 V for 10 μs, which should in principle induce the low-*VT* state, an *Id*-*Vg* sweep was again performed back to -1 V gate bias. Subsequently, the gate was grounded and an *Id*-*Vg* sweep from -1 V to 1 V gate bias was performed once per time decade in order to cause the least possible state disturb (Fig. 2a).

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| a | **102x /** | **10 μs** | | **3** | **100 μs** | **104s** |
| **+5V** | **104x** | **1** | **2** |
| **12** |
| **-5V** |

The results of the characterization showed that the high-*VT* state could be induced appropriately. However, the low-*VT* state which should follow on the falling edge (number 2 in Fig. 1a) was superimposed by severe electron trapping due to a shift to a significantly high threshold voltage of around 3 V (Fig. 2b). This is in accordance to previous publications where strong electron trapping for HfO2-based FeFET devices was reported [4]. Already the succeeding *Id*-*Vg* sweep could recover a positive memory window which was growing up to a retention time of one second (Fig. 2c). This can be explained by continuous detrapping of electrons from the gate stack, partially accelerated by the negative starting voltage of the intermediate *Id*-*Vg* sweeps. After one second retention time, the memory window decreased in a logarithmic manner as would be expected for classical FeFETs as well. By logarithmic extrapolation a 0.8 V and a 0.7 V memory window for 102 and 104 previously applied stress cycles can be estimated after ten year data retention at room temperature. These results verify that even after a certain amount of stress cycles, data retention in HfO2-based FeFET devices is possible.

Besides FeFET device characteristics, the operation of memory cells in an 1T AND array configuration had also been analyzed in the past [5]. These studies led to the discovery of a novel operating scheme called the “Positive-Source-Drain-Erase-Scheme” (PSDES) that shall be presented in the following. The scheme is specifically targeted at bit-wise writing of the high-*VT* state (erased state) within a FeFET AND array. It therefore differs from traditional block wise / Flash-type erase and allows for true random program / erase operations (Fig. 3).

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| b | 10-2 |  |  | 1 | | | 2 | |  |  | Program via *VDD*/3 | SL / BL (n) | SL / BL (n+1) |
| [A] |  |  |  |  |  |  |  |
| Erase via PSDES |
| Drain Current | 10-3 | -1 | 12 | 4 | 5 |  |  |
| 10-4 | 3 | | | | | WL (m) |
| 10-5 | retention time | | | | | WL (m+1) |
| c | 0 | 1 | 2 | | 3 |
| Gate Voltage [V] | | | | |

|  |  |  |  |
| --- | --- | --- | --- |
| Mem. Window [V] | 1.25 | 102x ±5V  104x ±5V | 10 y |
| 1 |
| 0.75 |
| 0.5 |
| 0.25 | 10-6 100 104 1010 | |

Retention Time [s]

Fig. 2: Retention after endurance test for FeFET structures (300 DUTs in parallel). (a) Utilized pulse train with measurement segments indicated by color coding and numbers. (b) Extracted *Id*-*Vg* characteristics at points corresponding to numbering given in (a). (c) Memory window as a function of retention time after 102 and 104 applied stress cycles.

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The scheme has been verified both experimentally as well as by TCAD simulation and the results will be shown elsewhere. The major advantage of the scheme is its bit-selectiveness and that it holds promise to be applicable also to advanced silicon-on-insulator (SOI) technology nodes.

III.3DTRENCH CAPACITORS FOR 1T-1CFRAM

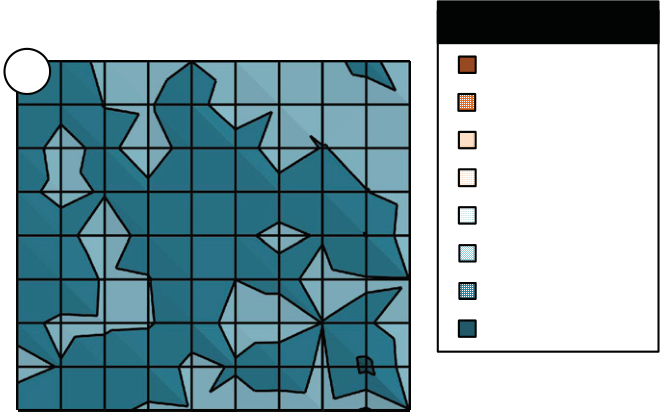
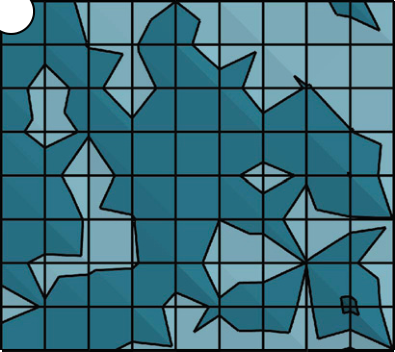
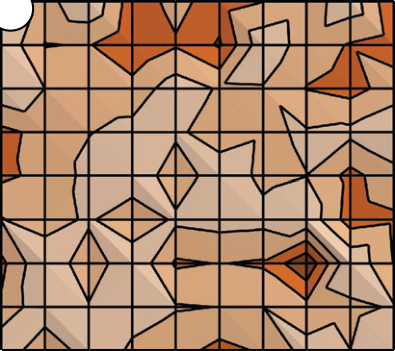
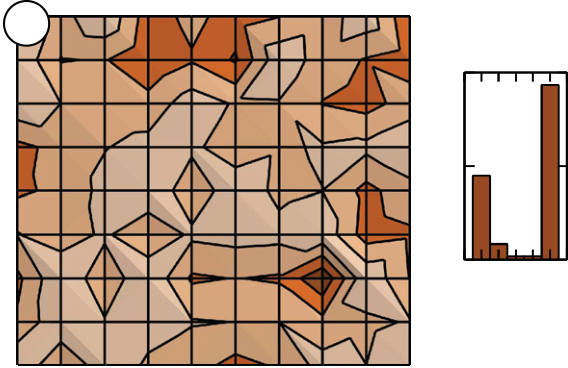
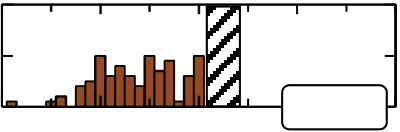
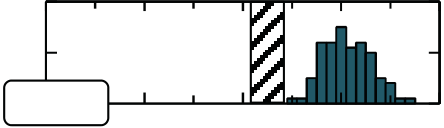
In the last two decades the challenging scaling of dynamic random access memory (DRAM) has proven to be one of the biggest drivers for material and process innovation in the semiconductor industry. Especially the vertical integration of the storage capacitor in the commonly adapted one-transistor one-capacitor configuration has led to numerous advances in etch and thin film technology. However, despite these tremendous advances in DRAM scaling, which is currently being produced at the 2X nm technology node, one-transistor one-capacitor based FRAM is still lacking far behind. Even though from a technology point of view FRAM can be understood as a non-volatile analogue of DRAM, their integration and material challenges are markedly different.

In order to follow the pathway of the highly scaled DRAM, a three-dimensional integration of the ferroelectric capacitor in FRAM will eventually be required. Besides numerous issues related to the conformal deposition of the commonly used material stacks, a simple steric problem induced by the inadequate thickness scaling of the ferroelectrics manifests as the most fundamental issue. Naturally, the minimum diameter of a trench capacitor or cylindrical stack capacitor, as well as the lateral spacing of a simple stack capacitor is linked to the total thickness of the metal-ferroelectric-metal stack being integrated. Considering the difficulties in scaling ferroelectric film thickness of the commonly used PZT below 30 nm [6] the lateral foot print of the capacitor remains rather large and comparable to the planar approach. Therewith the advantages of a three-dimensional integration become obsolete and are not simply linked to a maturity issue of thin film technology.

With the ability to sustain ferroelectric properties in the single digit nanometer range, HfO2- or ZrO2-based thin films in combination with simple nitride based electrodes appear ideally suited for the three-dimensional integration of CMOS-compatible ferroelectric capacitors. Considering the similar choice of material in state of the art DRAM, a comparison of FRAM to DRAM is now truly valid. With the purpose of volatile data storage these material stacks have been integrated into high aspect structures and have proven high volume manufacturability.

A first proof of concept concerning the sustainability of the ferroelectric properties in high aspect structures is presented in Fig. 4 [7]. The area enhancement achieved by the extension of the Al:HfO2 based ferroelectric capacitor into multiple silicon trenches (Fig 4a) is almost fully reflected in the corresponding polarization-voltage characteristics normalized to the capacitor area (Fig. 4b). Based on these first results it can be concluded that the loss of remanent polarization related to three-dimensional processing is minimal and ferroelectric phase stability is maintained along the entire depth of the trenches. Atomic layer deposition of the ferroelectric HfO2 and the TiN-

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IV.PROOF-OF-CONCEPT:28 NM FEFETARRAYS

Beyond the characteristics of multiple memory cells connected in parallel in order to move closer towards a proof-of-concept demonstration, several memory cells have to be connected in a matrix architecture. This allows on the one hand to test if each memory shows proper memory operation but also to test the parasitic influences of neighboring cells when a selected cell is written or read out. In the course of this work, smaller amounts of FeFET devices were connected in different architectures whereas results for the NAND architecture shall be presented in the following. The cell array consisted only of 90 cells in total since no integration scheme of FeFET cells besides logic transistors was available, hence, no peripheral decoders could be implemented. The 90 cells were distributed across nine wordlines and 10 bitlines whereas two additional signal lines needed to be provided for the NAND specific bitline-select and sourceline-select transistors. The cells had a channel length of 34 nm and a width of 210 nm each.

In a first measurement, the high-*VT* state of each cell was extracted after a negative wordline bias of -7V / 1us was utilized to set the state wordline-wise. Afterwards, a cell wise program operation to the low-VT state was performed utilizing an incremental-step-pulse-programming (ISPP) scheme known from Flash memories [9]. The target threshold voltage was set to -0.5 V and the maximum programming operation was limited to 6 V / 1 μs (Fig. 5).

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| BL1 | | BL2 | BL3 | BL4 | BL5 | BL6 | BL7 | BL8 | BL9 | BL10 | ***VT* [V]** | | |
| WL1  WL2 | a | | | | | | -1.5 - -1.25 | | |
| -1.25 - -1 | | |
| WL3 | | | | | | | 0 | 0 | | | -1 - -0.75 | | |
| -0.75 - -0.5 | | |
| WL4 | | | | | | |
| -0.5 - -0.25 | | |
| WL5 | | | | | | |
| -0.25 - 0 | | |
| WL6 | | | | | | |
| 0 - 0.25 | | |
| WL7 | | | | | | |
| 0.25 - 0.5 | | |
| WL8 | | | | | | |
| 20  0 | # Devices [1] | |
| WL9 | | | | | | |
| -7V / 1 us | | | | | | |
| *VT* [V] | | | -1 | -0.5 | | |
| WL1  WL2 | b | | | | | | # Devices [1] | | |
| 60 | | |
| WL3 | | | | | | |
| WL4 | | | | | | | 30 | | |
| WL5 | | | | | | |
| WL6 | | | | | | | 1 5  Amp [V] | | 0 |
| *VT* [V] | | |
| WL7 | | | | | | |
| WL8 | | | | | | |
| WL9 | | | | | | | 20  0 | # Devices [1] | |
| ISPP at 1 us | | | | | | |
| -1 | | | | -0.5 | | |

Fig. 5: Spatial and statistical threshold voltage distributions of 90 bit NAND array. (a) Threshold voltage distribution for the erased state (wordline-wise erase with -7 V / 1 μs pulses). (b) Threshold voltage distribution for the programmed state utilizing an ISPP scheme. The required program amplitudes for reaching the low-*VT* target of -0.5 V are shown on the right.

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