Ferroelectric Hafnium Oxide A Game Changer to FRAM?

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***Abstract*— In this paper the potential of hafnium oxide as a CMOS-compatible ferroelectric for future memory applications is assessed. The high coercive field strength of ferroelectric hafnium oxide is identified as a key parameter being crucial to device performance. It provides the unique thickness and lateral scaling potential of this novel ferroelectric, while at the same time compromises its endurance properties due to large switching fields. Considering the ambivalent nature of this parameter as well as the emerging trade-off between retention and endurance, voltage controlled operation modes and different device concepts**

the exceptionally high coercive field strength Ec of FE-HfO2, preserving the memory window at reduced thickness (Figure 1b). Moreover, in the case of the capacitor based solution, the thickness scalability of ferroelectric HfO2 and the availability of mature thin film technologies allow for an area enhancement to the third dimension (Figure 1d). In this paper we critically review the current status of this disruptive technology and assess its future potential by exercising general scaling considerations and device simulations.

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| **for ferroelectric hafnium oxide are discussed.** | II. | FERROELECTRICITY IN HAFNIUM OXIDE |

***hafnium oxide; ferroelectric; FRAM; FeFET, NVM***

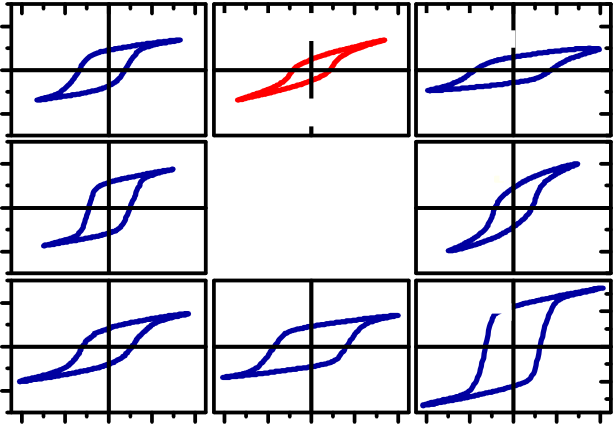
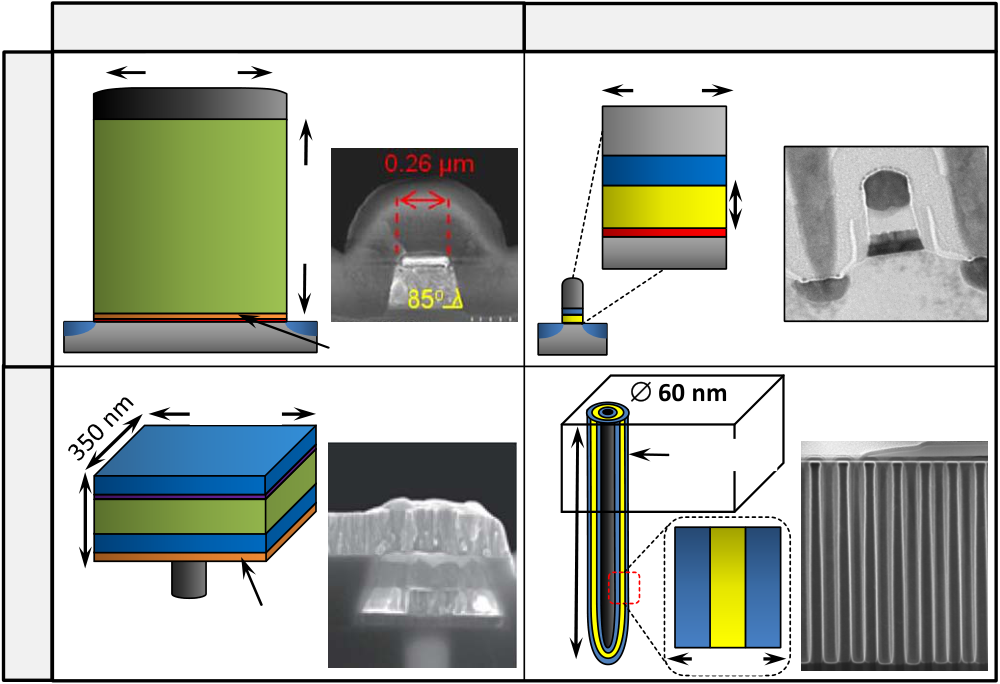
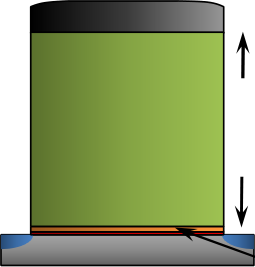
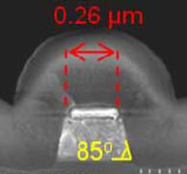
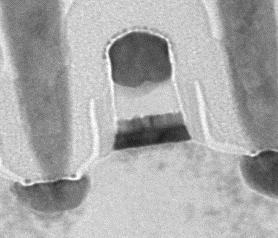
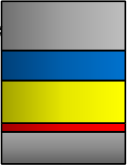
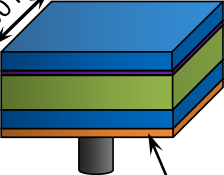
I. INTRODUCTION

The first research and development efforts focusing on ferroelectric random access memory (FRAM) were started more than 60 years ago [1]. Even though new and promising nonvolatile device concepts have emerged since then, the right to exist for FRAM is still provided by its excellent energy efficiency, fast rewrite speed and low voltage operation capability. Compared to the heat induced switching in PCRAM, spin transfer in STTRAM, ion conduction in RRAM or hot electron injection in NOR-FLASH, the electron efficiency of the polarization induced displacement current in FRAM remains unchallenged. Nevertheless, besides some temporary upturns and the launch of a few niche products, the focus of attention has notably shifted away from FRAM. This is mainly due to the challenging integration and limited scalability of capacitor-based (1T-1C) as well as transistor-based (1T) ferroelectric memory cells [2, 3]. These issues are decisive upon the future of FRAM and can be traced back to the choice of the ferroelectric itself. The commonly utilized perovskites, e.g. PZT or SBT, do not provide the thickness scalability and CMOS-compatibility required for cost efficient, high density 1T-1C or 1T memory solutions (Figure 1 a and c).

However, utilizing ferroelectric hafnium oxide (FE-HfO2) based memory devices, this scaling and integration dilemma can be overcome [4 and references therein]. Highly scaled 1T FRAM at the 2X nm node, as well as the possibility of a DRAM-like 3D-integration of 1T-1C FRAM has been demonstrated. In the case of 1T FRAM this renewed scaling potential compared to its perovskite contenders is provided by

The experimental observation of polarization hysteresis in hafnium oxide based thin films is believed to be due to the appearance of a ferroelectric phase in this system. However, in order to fulfill the criteria for genuine structural ferroelectricity a deviation from the well-known centrosymmetric polymorphism (monoclinic-tetragonal-cubic) of crystalline hafnium oxide is required. It is argued that this deviation is the stabilization of an orthorhombic and non-centrosymmetric phase in hafnium oxide thin films. Due to the displacement of oxygen anions against the cation sub lattice a spontaneous and switchable polarization evolves. Structurally this phase has already been identified in ZrO2-based ceramics in 1989, but was never tested electrically [5]. The rediscovery of this phase in hafnium oxide thin films in 2011 revealed the potential of these CMOS-compatible transition metal oxides as a novel class of ferroelectrics. A summary of electrical, electromechanical, as well as structural evidence for this hypothesis is given in [4, 6].

As shown in Figure 2, multiple dopants facilitating the stabilization of this ferroelectric phase have been identified [4]. Other parameters, such as e.g. grain size, can additionally be utilized to partially stabilize a ferroelectric phase in pure HfO2 as well (to be published elsewhere). Depending on how well the doping level and/or process is optimized a large ferroelectric phase fraction and therewith a large remanent polarization Pr can be obtained. Values as high as 45 µC/cm2 for e.g. the La doped system have already been demonstrated. However, switching the polarization to the opposite polarity requires comparably large fields. The coercive field of all hafnium oxide based system investigated so far ranges between 1 and 2 MV/cm. For comparison, the extrinsic Ec of most perovskites is below 100 kV/cm.



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| --- | --- | --- | --- | --- | --- | --- | --- |
| **1T FRAM** | (a) | **state of the art (perovskites)** | | (b) | **FE-HfO2 based** | | Ref. [B] |
| 260 nm | |
| 28 nm | |
| **Pt** | Ref. [A] |
| **Poly-Si** | |
| **SBT** | 200 nm | **TiN**  **FE-HfO2** | 8 nm |
| **Si** | |
| **1T-1C FRAM** | (c) | **Si** | High-k buffer | (d) | ∅ **60 nm** | | Ref. [D] |
| 350 nm | Ref. [C] |
| **0.12 µm2** | |
| **0.12 µm2** | |
| 150 nm | **SrRuO3 / Ir** | | 0.5 µm |
| **PZT** | |
| **Ir** | |
| **W** | |

TiAlN

20 nm

Figure 1. Drawn to scale schematics of state of the art perovskite based 1T (a, Ref. A [3]) and 1T-1C (c, Ref. C [2]) ferroelectric memories compared to corresponding FE-HfO2 based devices (b) and (d). For comparison the FE-HfO2 based 1T cell is normalized to a theoretical memory window of about 1.5 V given in [3], whereas the FE-HfO2 based 1T-1C cell is normalized to the capacitor area of 0.12 µm2 given in [2] (at scaled thickness Pr PZT ≈ Pr FE-HfO2).

The feasibility of these FE-HfO2 based approaches (meeting specifications even beyond these requirements) has been demonstrated in Ref B [7] and D [8].

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 40 | **HfZrO4** | **pure HfO2** | **Gd:HfO2** | *A.Capacitor Based Ferroelectric Memory (1T-1C FRAM)* |

0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| polarization (μC/cm2) | -40 | **Si:HfO2** | **engineered** | **Al:HfO2** |
| 40 |
| 0 | **Y:HfO2** | **FE-HfO2** | **La:HfO2** |
| -40 |
| **Sr:HfO2** |
| 50 |
| 0 |

-50

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| -4 -2 0 | 2 | 4 | -4 -2 0 | 2 | 4 | -4 -2 0 | 2 | 4 |

electric field (MV/cm)

Figure 2. P-E-hystereses of HfO2 based metal-insulator-metal capacitors reveal FE-properties for various dopants X (<10 mol%) in HfO2, for the HfO2-ZrO2 solid solution as well as for undoped HfO2 processed under suitable conditions. The Pr of the ferroelectric films ranges from 10 - 45 µC/cm2.

III. RENEWED SCALING POTENTIAL FOR FRAM

Capacitor-based FRAM has successfully claimed a niche market, where extremely low write and read power in combination with a fast and random access based NVM concept is required. However, due to the limited scalability and challenging integration of perovskite based 1T-1C FRAM these niches must tolerate its rather large cost per bit.

The FeFET concept based on perovskites faces similar issues in terms of manufacturability and scalability. However, despite numerous attempts and some clear advantages compared to capacitor-based FRAM (e.g. nondestructive read and smaller cell size) a FeFET memory has until now not been commercialized. This is mainly due to the persistent retention issues evolving from the metal-ferroelectric-insulator-semiconductor (MFIS) structure of this 1T FRAM as compared to the metal-ferroelectric-metal (MFM) capacitor of the 1T-1C solution [9].

In this section the superior scaling perspective of FE-HfO2 compared to perovskite systems will be elucidated for both memory concepts. Ultimate scaling limits based on voltage, material and simple geometrical considerations will be given.

Scaling the lateral footprint of the MFM capacitor, while at the same time maintaining a sufficiently large sensing margin between the switching and non-switching state, remains a major challenge for high density 1T-1C FRAM. Following the pathway of the closely related DRAM by extending the capacitor into the third dimension either in a classical horizontal [10] or a vertical [11] manner has been proven to be extremely difficult. This is mainly due to an insufficient thin film technology and the large physical thickness and complicated crystal structure of perovskites severely restricting the diameter of a trench or stack capacitor. Film thickness in perovskites does not easily scale due to degrading ferroelectric properties and a strong increase in leakage current.

Considering these scaling issues of the MFM capacitor in the context of FE-HfO2, four distinct advantages of this novel ferroelectric can be identified:

|  |  |
| --- | --- |
| •  •  •  • | ALD technologies for hafnium and zirconium oxide based systems and related metal nitride electrodes in high aspect ratio structures have proven maturity on a manufacturing level.  Stable ferroelectric properties of FE-HfO2 have been proven for physical thicknesses down to 5 nm [6]  The high band gap of FE-HfO2 and its high conduction band offset to nitride-based electrodes allows for low leakage current operation at strongly reduced thickness  The atypical combination of a rather large remanent polarization and a low dielectric constant in FE-HfO2 further improves the non-switching to switching polarization sensing margin. |

The proof of concept for a 3D integrated FE-HfO2 has most recently been demonstrated in [8]. It was shown that the planar Pr of FE-HfO2 is largely preserved when integrated into deep trench capacitors with an aspect ratio of 13:1 (see also Figure 1d). This minimal polarization penalty for 3D integration

suggests that by conformal ALD coating the ferroelectric phase stability of FE-HfO2 can be maintained even at the sidewall of deep trench structures. With this feasibility demonstration scaling of the FRAM capacitor alongside advanced standalone and embedded DRAM storage nodes seems possible. Depending on the plate line technology used, a cell size that is very close to that of state of the art DRAM appears realizable for 1T-1C FRAM for the first time.

However, when considering the stringent voltage scaling requirements of the extremely low power FRAM technology, the rather high Ec of FE-HfO2 needs to be compensated by a very thin physical thickness of the ferroelectric layer. A ferroelectric film thickness dFE of 5 nm shall be regarded as a lower limit in the following considerations. Even though the ferroelectric properties of FE-HfO2 appear to be stable below this limit, leakage currents and contributions of film and electrode roughness become significantly enhanced when scaling beyond. Assuming a switching field ESW of at least 3 x Ec for saturated and retention stable polarization reversal, an operating voltage of about 1.5 V appears to be the lower limit for FE-HfO2 based 1T-1C FRAM (Figure 3). Due to the very low Ec of perovskites, switching voltage of classical 1T-1C FRAM technology is likely to scale even below 1 V. However, considering the frequently observed increase in Ec with decreasing dFE and the difficulty to scale polycrystalline perovskites below 30 nm this has yet to be demonstrated. As Figure 3 illustrates once more, scaling of dFE is a requirement not only for voltage reduction but also for obtaining a reasonable lateral dimension of a 3D capacitor structure. Only then the steric boundary conditions are given to vertically integrate the MFM layer stack into small feature sizes.

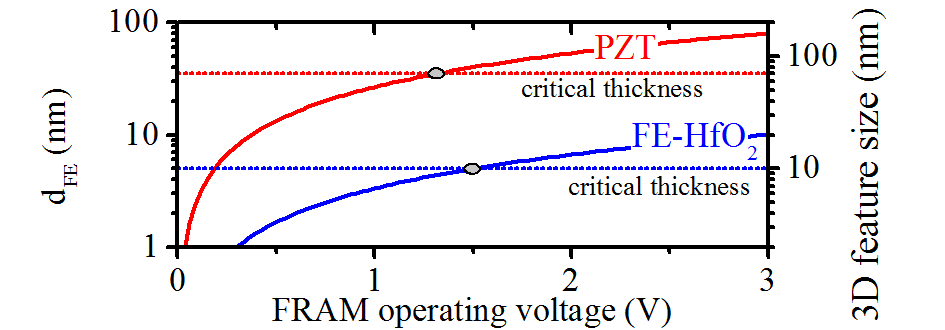


Figure 3. Simplified comparison of minimum switching voltage and 3D feature size achievable with polycrystalline PZT or FE-HfO2. The following assumptions are made: saturated switching voltage equals 3\*Ec\*dFE; critical dFE of PZT is reached at about 35 nm at which EC equals 125 kV/cm ([12]); critical dFE of FE-HfO2 is reached at about 5 nm at which EC equals 1 MV/cm [6]; minimum diameter of cylindrical stack capacitors or minimum spacing betwenn pillar shaped capacitors >2\*dFE (for simplicity electrode system, plug and storage node contribution to overall layer stack thickness are neglected).

It is interesting to note that when considering dead layer effects or non-ideal interfaces the high depolarization resilience of a large Ec might even be required to scale dFE of polycrystalline ferroelectrics to the single digit nanometer range [6]. The authors believe that in order to meet the demanding thickness requirements for 3D integration, a high band gap, high Ec ferroelectric with a simple electrode system, such as TiN/FE-HfO2, appears to be the only viable solution.

*B.Ferroelectric Field Effect Transistor*

To keep up with the CMOS and memory scaling trend, a gate length LG reduction of the ferroelectric field effect

transistor is required. However, due to the relationships among dFE, Ec, memory window and depolarization field, the FeFET is faced with a complex scaling dilemma. At reduced LG, fringing fields, short channel effect as well as manufacturability are becoming severe issues for perovskite based gate stacks as thick as 200 nm. However, a simple reduction of dFE leads to several issues that can only be solved by the introduction of a suitable ferroelectric:

|  |  |
| --- | --- |
| • | The memory window is directly proportional to dFE and Ec. Loss of memory window with decreasing dFE can only be compensated with increasing Ec. |

Solution: The exceptionally high Ec of FE-HfO2 allows for a reduction of dFE to the single digit nanometer range (e.g. Figure 1b).

|  |  |
| --- | --- |
| • | Depolarization field increases with decreasing dFE. Retention loss can only be compensated by increasing either EC, interface capacitance or substrate doping. |

Solution: The CMOS compatibility of FE-HfO2 allows for a thin, high capacitance interfacial layer, which together with the high Ec reduces retention loss at scaled dFE.

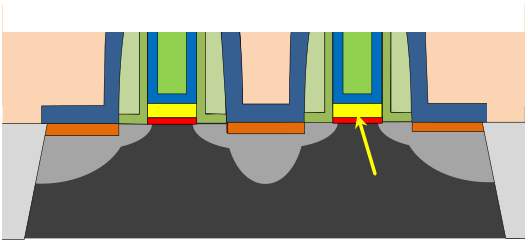
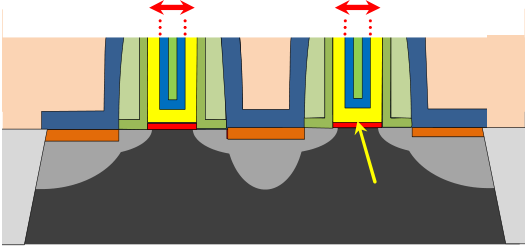
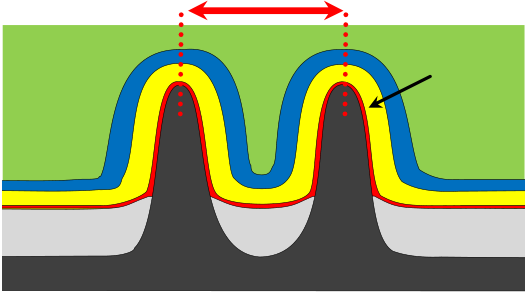
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| • | Ferroelectric | properties | of | the | polycrystalline |
| perovskites were found to degrade with decreasing dFE. A ferroelectric, stable with respect to thickness reduction needs to be implemented. | | | | |

Solution: The ferroelectric properties of FE-HfO2 have proven stable down to film thicknesses of 5 nm.

Utilizing these clear advantages, FE-HfO2 based FeFETs have been successfully implemented at the 28 nm node ([7], Figure 1b). This demonstration of highly scaled FeFETs has closed the two orders of magnitude scaling gap between FeFET and CMOS that has prevailed ever since the introduction of this memory concept. This memory technology is now capable of scaling alongside CMOS, and can be considered a promising candidate for embedded memory applications in future HKMG technologies.

However, for scaling beyond the 28 nm technology node, several aspects, such as memory window requirements and transistor technology have to be considered. Especially in the case of an embedded memory it is most desirable to adopt the transistor technology of the corresponding CMOS platform. The scaling considerations depicted in Figure 4 (not drawn to scale) assume a memory window of 1 V, which leads to a ferroelectric film thickness of at least 5 nm. Short channel effects and the actual availability of the platforms are excluded from these considerations.

Given the feasibility of a gate length to stack height ratio of LG 28 nm / dFE 10 nm demonstrated in [7], a reduction to LG 14 nm / dFE 5 nm in high-k first / metal last technology (half replacement gate) seems possible (Figure 4a). However, considering the spacer sidewall coverage in high-k last / metal last technology (full replacement gate), a similar reduction of gate length is not possible (see critical dimension illustrated in Figure 4b). Without the suppression or recess of this sidewall coverage the gate fill is no longer possible, and the full



replacement gate FeFET does not fully scale beyond the 2X nm node. A similar limitation with a different critical dimension appears when assessing FinFET technology as a host for the FE-HfO2-based FeFETs (the 3D capability of FE-HfO2 required for FinFET integration has already been summarized in the previous section). Due to the introduction of 5 nm FE-HfO2 to the HKMG layer stack, the space between the fins is narrowed down by 10 nm. Assuming a triangular fin shape this limits fin pitch to about 4X nm and therewith complicates scaling beyond 1X nm FinFET technology.

statistical variation of gate areas as small as e.g. (1X)2 nm2 cannot be drawn.















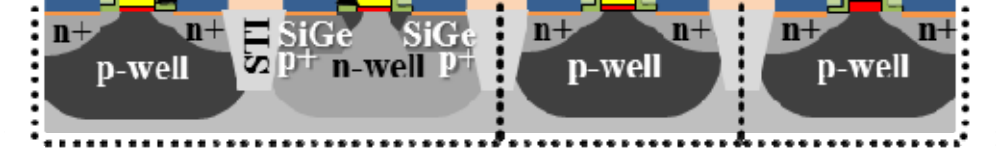


Figure 5. Exemplified schematic of an FeFET based embedded memory

|  |  |  |  |
| --- | --- | --- | --- |
| (a) |  |  | solution for advanced HKMG. In this flavor the FE-HfO2 based FeFET is |
| **scales with replacement gate** | | implemented as high-k first / metal last providing scalability, whereas the |

logic and periphery is realized as a contemporary full replacement gate.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| (b) | **n+** | **n+** | **n+** | IV. | DEVICE PERFORMANCE |
| As a direct consequence of the disruptive scaling potential | |
| **p-Well** | **FE-HfO2** | |
| **scaling limitation at 2X nm LG** | | | demonstrated in section III, FE-HfO2 is facing challenging | |
| reliability issues that, to some extent, are intrinsic in nature. In | |
| this section these reliability concerns are critically examined | |
| (c) | **n+** | **n+** | **n+** | and are being set into perspective with its perovskite | |
| contenders. Optimizing the design of the memory device as | |
| well as enhancing memory performance on a system level is | |
| **p-Well** | **FE-HfO2** | | further discussed to broaden the scope of application for FE- | |
| **scaling limitation at 4X nm fin pitch** | | | HfO2 at its current stage of development. | |
| *A.Capacitor Based Ferroelectric Memory (1T-1C FRAM)* | |
| **FE-HfO2** | | |

**oxide**  **Si-fin**

Figure 4. Scaling perspective of FE-HfO2 based FeFETs assuming a memory window of 1V, a dFE of 5 nm and the standard metal gate stack of HKMG technology. The red arrows denote the critical scaling dimensions. (a) high-k first / metal last – half replacement gate. (b) high-k last / metal last – full replacement gate. (c) FinFET

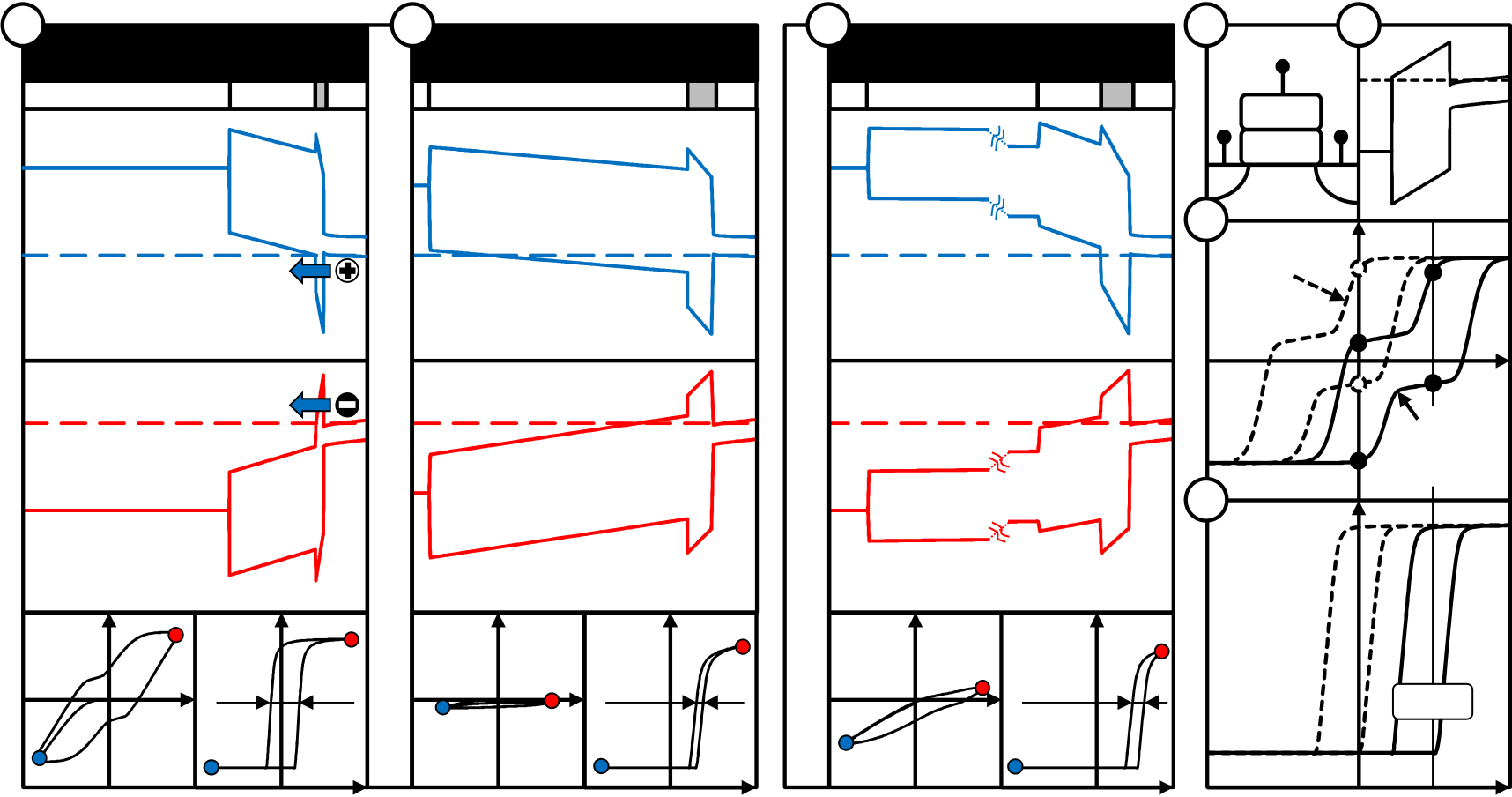
The implementation of FE-HfO2 based FeFETs as an embedded memory for HKMG CMOS technology is especially appealing due to the large similarities of the memory and logic transistors. Due to the high flexibility of FE-HfO2 with respect to electrode material and thermal budget (gate first/gate last), the only requirement for the memory transistor is a thicker and crystalline HfO2. Every other material or gate stack design aspect of HKMG may remain unchanged. Several combinations of CMOS and memory transistor integration flows requiring only 1-2 additional lithographic masks are thinkable. As an example, Figure 5 shows a combination of a FeFET first (half replacement gate) and CMOS last (full replacement gate) integration.

As concluding remarks to this section, it should be noted that a 1X nm planar or fin-shaped RAM transistor can hardly be reached with any other technology, and could readily be applied at the 1X nm as well as, at a relaxed pitch, in the succeeding CMOS technology nodes. However, due to the lack of experimental data on large array statistics, the feasibility of the scaling approaches suggested here cannot be fully judged. Even though the piezoresponse force microscopy data presented in [4] and [13] show a homogenous distribution of FE-properties on the mesoscopic scale, final conclusions on the

The failure mechanism fatigue, imprint and intrinsic depolarization are decisive upon the potential use of a ferroelectric in NVM technologies. Since the discovery of FE-HfO2 in 2011 several of these endurance and retention relevant parameters have been investigated using MFM capacitors. Even though these results were gathered on a single cell level and need to be confirmed on a larger statistical basis, the following performance characteristics can be summarized ([14, 15]):

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| •  •  • | For | saturated | polarization | | | hysteresis | | minimal |
| degradation of the memory state was demonstrated after 1000 h bake at 125°C, corresponding to 10 year retention at 85°C. However, polarization sub loops at reduced switching voltage were found to be prone to depolarization and therewith retention loss within the bake period.  Opposite state retention and therewith imprint characteristics were found to be comparable to PZT after 1000 h bake at 125°C. About 75% of the initial polarization was still achievable for the inverse state after testing.  At the current development stage the endurance of saturated polarization states was found to be limited to about 109 switching cycles. Hard breakdown (HBD) of the ferroelectric was identified as the failure mechanism limiting endurance. For unsaturated polarization loops about two orders of magnitude | | | | | | | |
| higher | endurance | | and | the | onset | of | classical |
| ferroelectric fatigue was observed. | | | | | | | |

Since in order to achieve sufficient retention saturated polarization loops are required, the endurance of FE-HfO2 at high switching fields needs to be improved. Due to the



destructive read operation of classical 1T-1C FRAM this is a requirement for achieving read endurance beyond the currently possible 109 switching cycles. Having identified HBD as the failure mechanism, the comparison of switching field to breakdown field in Table I further illustrates the severe challenge FE-HfO2 is faced with compared to its perovskite contenders.

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TABLE I | PROXIMITY | OF | | FERROELECTRIC | | | OPERATING | REGIME | TO |
| DIELECTRIC BREAKDOWN STRENGTH | | | | | | | |
| **SBT** | | | | | **PZT** | | | **FE-HfO2** |  |
| **(25 nm)** | | | | | **(35 nm)** | | |
| **(10 nm)** |
| **[16]** | | | | | **[12, 17]** | | |
| **switching field ESW** | | | | | | | | ~ 3 MV/cm |  |
| (saturated ESW ~ 3\*Ec) | | | ~ 300 kV/cm | | ~ 375 kV/cm | | |
| **break down field EBD** | | ~ 1.4 MV/cm | | | | ~ 1.2 MV/cm | | ~ 5 MV/cm |
| **percentage of EBD** | | | | | | | | ~ 60% |
| **reached during ESW** | | ~ 21% | | | ~ 31% | | |

Considering this close to HBD operation mode as well as the already largely optimized leakage current of state of the art hafnium and zirconium oxide based thin films, there are only limited options for improvement left. However, reducing trap assisted tunneling by passivation of defects and improving the

TiN/FE-HfO2 interface quality is believed to immediately improve endurance, whereas high work function or oxidic electrodes, responsible for solving classical fatigue issues in perovskites, are unlikely to ease the major reliability concerns of FE-HfO2. Due to the TDDB related nature of the failure mechanism, a simple reduction of switching time and capacitor area, possible in a fully integrated memory array, is believed to further increase endurance.

One possible way to improve the memory performance of a FE-HfO2 capacitor based memory on a system level is to make use of its striking resemblance to dielectric material and electrode systems of state of the art DRAM. As describe in [6] this might yield the opportunity to operate FRAM architecture in a volatile DRAM-like mode during power on, while accessing non-volatile FRAM mode on a store and recall basis only when needed. In the low voltage DRAM-like mode of this 1T-1C NV-DRAM the FE-HfO2 acts as a fairly linear capacitor yielding unlimited read/write endurance and fast speed, whereas polarization reversal at high voltage in FRAM mode provides non-volatility on demand with reduced endurance requirements.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| a | FE-HfO2-NVM-Type | | | b | FE-HfO2-VM-Type | | Si | c *WFPt*=5.66 eV;χ*SBT*=3.4eV;*EG,SBT*=4eV;*PS*=5µC/cm2;*Pr*=4µC/cm2;*EC*=50kV/cm;ε*SBT*=180;ε*HfO2*=20 | SBT-NVM-Type | | | Si | d | G | | e | | HfO2 | Si |
| *WFTiN*=4.2 eV;χ*HfO2*=2.05eV;*EG,HfO2*=5.9eV;*PS*=10µC/cm2;*Pr*=9.5µC/cm2;*EC*=1MV/cm;ε*FE*=30 |
| D | TiN |
| TiN | Si:HfO2 | Si | Zr:HfO2 | | Pt | SBT | HAO | S | M |
| F | |
| Prg at *VG* = -5V | | | Prg at *VG* = -4V | | *VG* | Prg at *VG* = -5V | | | *VG* | f | S | | *P* | | *VG* = 3V | |
| NDRO- | |
| Type | |
| WF=4eV | | *VG* | |
| g |
| *ID* | |
| DRO-Type | |
| WF=5.5eV | |
| Ers at *VG* = +5V | | | Ers at *VG* = +4V | | Ers at *VG* = +5V | | |
| *VRead* | |
| *ID* | | | *P* | *ID* | *Px2* | *ID* | |
| ∼1.5V | | | ∼0.3V | | ∼0.7V | | |
| *VG* | | | *VG* | | *VG* | | |
| *VG* | |
| *VG* | | |

Figure 6. Simulated program / erase characteristics of experimentally demonstrated FeFETs. Band diagrams (top), polarization- and drain current-gate voltage characteristics (bottom) are illustrated (a-c). (a) The stack of the Si:HfO2-based FeFET of [7] was based on a TiN metal gate, 10 nm Si:HfO2 ferroelectric and a 1 nm SiO2 interfacial layer (grey shaded). Program / erase at ±5V leads to a memory window of ∼1.5V. (b) The DRAM-type FeFET published in [18] consists of a TaN-gate electrode, 30 nm Zr:HfO2 ferroelectric and a 3 nm SiO2 interface. Program / erase at ±5V leads to a memory window of ∼0.3V. (c) SBT-FeFETs [19] possess a platinum gate electrode, 200 nm SBT ferroelectric, a 7 nm Al:HfO2 dielectric buffer layer and a 3.5 nm SiO2 interface. Material parameters that were used for simulation are shown in between/left to the illustrations (for SBT: see [17, 20]). (d) Optimized FeFET stack of MFS type. (e) Band diagram for MFS type at 3.3V gate bias and 5.5 eV metal gate workfunction. (f) Polarization-gate voltage characteristics depending on the metal gate workfunction (ferroelectric material parameters were chosen according to (a)). (g) Corresponding drain current-gate voltage characteristics with read voltage for DRO-type indicated (fine solid line, for NDRO-type Vread=0V).

*B.Ferroelectric Field Effect Transistor (1T FRAM)*

Utilizing the recently discovered ferroelectric properties of FE-HfO2, both non-volatile and volatile memory operation of FeFETs could experimentally be verified [7, 18]. For the non-volatile memory approach, scaling of the FeFET to HKMG technology nodes could finally be achieved. However, endurance characteristics were limited to 104 program / erase

cycles which was explained by the degradation of the interfacial layer [21]. Considering the band diagram for the respective gate stack and program / erase conditions at a gate voltage of ±5V (see Figure 6a), severe charge injection can be anticipated from Fowler-Nordheim or direct tunneling alone. Moreover and compared to classical ferroelectrics, simulations show that even though the FE-HfO2 is much more resilient towards depolarization [6], still a significant reduction of

spontaneous polarization *PS* occurs when the gate voltage *VG* returns to zero (see Fig. 6a bottom left).

Recently it was demonstrated that the endurance characteristics of FE-HfO2-based FeFETs can indeed be improved by implementation of different gate stack geometries and operating conditions [18]. By increasing the ferroelectric and interfacial layer thickness to 30 nm and 3 nm respectively and operating the devices at ±4V *VG*, endurance characteristics of up to 1012 cycles could be demonstrated. Assuming similar ferroelectric properties of the utilized Zr:HfO2 composition [22] and Si:HfO2, simulations reveal that charge injection is quite unlikely, which is, however, caused by the fact that the FeFET is polarized in a severe subloop state (see Figure 6b). This is also reflected in a small memory window of approximately 300 mV which coincides well with experimental observations [18].

For classical SBT-based FeFETs [19], the ferroelectric film is much thicker but can be operated at similar gate voltages due to the low SBT coercive field of approximately 50 kV/cm at 200 nm dFE [20]. However, also for these types of FeFETs, depolarization has always been [9] and remains a challenge as seen by the suploop operation in Figure 6c. Consequently, data retention characteristics could be proven up to a maximum of 30 days for SBT-based FeFETs [23].

In order to give an estimate regarding the reliability characteristics of the presented FeFET approaches (Figure 6a-c), electron tunneling currents during erase operation were calculated based on equations from [24] (see Figure 7). As can be seen from Figure 6a-c, Fowler-Nordheim tunneling applies for NVM FE-HfO2 FeFET cell, whereas for both other FeFET stacks modified Fowler-Nordheim tunneling occurs.

Comparing the non-volatile to the volatile FE-HfO2- or to the SBT-FeFET clearly reveals severe differences: The NVM-FeFET suffers from severe charge injection due to the very thin SiO2 interface of 1 nm and an order of magnitude higher electric field. This charge injection can be seen as the most likely cause for accelerated endurance degradation. Since the band bending in Figure 6a shows that charge injection is close to the Fowler-Nordheim regime, increasing the interfacial layer thickness alone is unlikely to improve cycling characteristics (see also [25]). Although charge trapping seems to be detrimental for FeFET endurance, it brings benefit in data

|  |
| --- |
| retention. The higher amount of trapped charge at higher program/erase amplitudes compensates the polarization charge, which results in a decreased depolarization field and improves the retention properties (to be published elsewhere). The |

presence of charge trapping most likely explains the better retention properties of NVM FE-HfO2 FeFET stack [7], for which 10 years data retention is expected even at 200 °C [4], in contrast to both other FeFET types with a retention capability limited to several minutes [18] and days [23]. Therefore, an MFIS-FeFET memory cell exhibits a trade-off between endurance and retention behavior, where charge trapping is playing the key role.

A way to improve the endurance characteristics of MFIS-type FeFETs and at the same time preserve good retention properties was presented in [26]: By lowering *PS* of the

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| ferroelectric, both the interfacial field stress as well as the |

depolarization field can be reduced. However, since the *PS* actually represents an intrinsic material property, it remains to be verified if such a low polarization might not detrimentally affect device statistics [27].

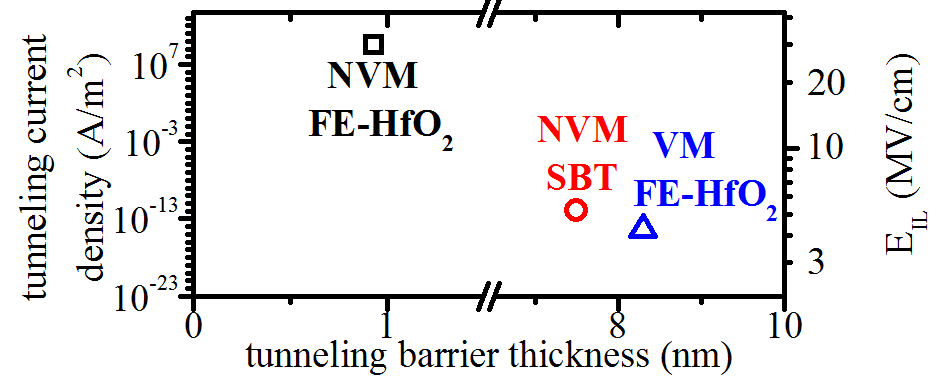


Figure 7. Electron tunneling current density and electric field in the interfacial layer EIL versus tunneling barrier thickness for three types of FeFET cells under their typical erase conditions: non-volatile FE-HfO2 FeFET [7], DRAM-type volatile FE-HfO2 FeFET [18] and SBT-FeFET [19].

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| In order to improve FeFET memory characteristics without engineering the ferroelectric itself, it might be possible to create MFS-type FeFETs in the future, i.e. eliminating the insulator between HfO2 and the silicon bulk altogether (Figure 6d). Significant progress in the field of epitactically grown HfO2 by ALD and appropriate post annealing steps has been made in the past [28]. If such approaches prove viable in the future, electron injection during erase operations might be reduced due to the different band alignment of the FeFET gate stack (Figure 6e). Moreover, in order to improve the retention characteristics of high *PS* FeFETs, creating an artificial imprint by workfunction engineering can be envisioned (Figure 6f). By this approach, different FeFET types possessing either | | | | | | | |
| destructive- | or | non-destructive-read | | | | out | ((N)DRO) |
| characteristics can be created. Due to the imprint created by an adjusted metal gate workfunction, a saturated and a fully depolarized state can be stabilized which could improve the overall FeFET retention characteristics. However, from a memory architecture viewpoint also for these types of FeFETs, write disturbs have to be eliminated by e.g. 2T cell concepts. | | | | | | | |
| V. | | | CONCLUSION | | | | |
| Hafnium | oxide | emerges | | as | a | CMOS-compatible | |
| ferroelectric providing unique three-dimensional and lateral scaling potential to capacitor as well as transistor based FRAM. Due to the large Ec of FE-HfO2 and its stable ferroelectric properties at reduced thickness, scaling of 1T FRAM alongside HKMG and 1T-1C FRAM alongside DRAM appears possible, yielding the potential to establish the first high density ferroelectric memory technology. However, considering the necessity of a large Ec to enable this drastic size reduction an intrinsic dilemma between scaling and device performance of ferroelectric memories evolves. As a consequence, the close to breakdown field operation of FE-HfO2 based MFM capacitors as well as severe charge injection in comparable MFIS-FETs are posing severe endurance constraints on the FE-HfO2 technology in its current development stage. Nevertheless, the   |  | | --- | | possibility to drastically increase endurance at the cost of | | | | | | | | |
| retention and vice versa as well as to switch between these | | | | | | | |
| modes on a system level needs to be considered when assessing | | | | | | | |

this memory technology. Even before further device improvements are established, this flexibility of performance parameters already opens a broad window of potential applications reaching from NOR-FLASH to low refresh rate 1T DRAM.

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