**Ferroelectricity in Hafnium Oxide:**   
**CMOS compatible Ferroelectric Field Effect Transistors**

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**Abstract**  crystallized in presence of a cap. We investigated the influence of mechanical encapsulation on HfSiO thin films at lower Si

We report the discovery of ferroelectricity in crystalline hafnium silicon oxide. If HfO2 based thin films, at a

content, where the complete stabilization of the tetragonal phase does not yet occur, in metal-insulator-metal capacitors.

composition where the tetragonal phase is not yet stable, are

crystallized in presence of a cap, the formation of an orthorhombic phase is observed. o-HfO2 shows a piezoelectric response, while a polarization measurements exhibit a remanent polarization above 10 µC/cm² at a coercive field of 1

**Ferroelectricity in Silicon doped HfO2**   
HfSiO was deposited by a metal organic atomic layer deposition process based on Tetrakis-(ethylmethylamino)-

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| MV/cm, confirming this phase to be ferroelectric. Transistors | hafnium | (TEMA-Hf), | Tetrakis-dimethylamino-silane |

fabricated with this material exhibit a permanent and switchable shift of the threshold voltage, allowing the realization of CMOS-compatible ferroelectric field effect transistors (FeFET) with sub 10 nm gate insulators for the first time.

**Introduction**

(4DMAS). metalorganic precursors and ozone. The silicon content was defined by varying the cycle ratio of the precursors and monitored by secondary ion mass spectrometry and elastic recoil detection analysis on samples without thermal treatment.

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| The crystallization temperature of all films in the used |

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| thickness (7-12 nm) and composition range (2.5-6 mol% SiO2) |

was above 500°C. Titanium nitride electrodes were deposited by a chemical vapor deposition process based on TiCl4 and

The FeFET is a long-term contender for a fast, low power NH3.

and nonvolatile memory technology [1]. In these devices, information is permanently stored as polarization state of the gate insulator and can be read non-destructively as a shift of the threshold voltage. The FeFET concept was experimentally demonstrated decades ago [2], but the practical implementation has remained elusive. This is due to a thermodynamic incompatibility of known ferroelectrics, such as lead zirconate titanate (PZT), strontium bismuth tantalate (SBT), and strained strontium titanate (STO) to silicon. Furthermore, due to low band offsets to silicon [4], thick films and noble metal electrode are required for low leakage devices. Numerous attempts have been made to improve the stability of ferroelectrics in contact with silicon by the introduction of buffer layers [3]. However, these approaches diminish the scalability of these devices as low EOT values are required for channel control in submicron devices. Furthermore, the introduction of an electrically thick buffer layer leads to a

By lowering the deposition temperature of the titanium nitride (TiN) top electrode below the crystallization temperature of the HfSiO dielectric, it was possible to encapsulate amorphous films and induce the crystallization in a subsequent thermal treatment step above the crystallization temperature. We found that capacitors manufactured with this scheme exhibited non-linearities in their capacitance-voltage behavior, which did not occur if crystallization was induced prior to capping (Fig. 1). A comprehensive characterization was made by electrical polarization measurements on capped HfSiO films at different compositions. A gradual transition from ferroelectric to antiferroelectric polarization curves is observed with increasing silicon content (Fig. 2), which is also reflected in small signal capacitance-voltage measurements. Further evidence for ferroelectric and antiferroelectric behavior was obtained by measurement of the mechanic displacement (Fig. 3). The ferroelectric sample shows clear evidence of

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| degradation of data retention due to a high depolarization field | piezoelectric | behavior, | which | is | a | prerequisite | for |

[5]. It becomes clear that a silicon compatible ferroelectric is a requirement for a reliable FeFET.

As known from the search for high-k gate dielectrics, only very few metal oxides are stable in contact to silicon and exhibit a sufficient band offset at the same time [6]. One of them is the well known high-k dielectric HfO2, which has so far been only regarded as a paraelectric material.

It has been reported [7,8], that the properties of HfO2, and consequently HfSiO, thin films can be influenced, if

ferroelectricity [9]. A symmetric, electrostrictive, response is observed for the antiferroelectric sample. This confirms that the observed polarization loops are not caused by parasitic electronic effects, but are of microstructural origin.

Since ferroelectricity is related to the crystal structure, a previously undetected crystalline phase must be present in the devices as prepared here. X-ray diffraction measurements (Fig. 4) of uncapped films show good agreement to a tetragonal/monoclinic-HfO2 mixture, as it is commonly

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observed for crystalline thin films. Capped samples, however, show a difraction pattern indicating a significant fraction of orthorhombic-HfO2. The known forms of o-HfO2 (Space groups Pbca and Pbcm) are centrosymmetric and therefore not ferroelectric. Furthermore, they are usually only observed at

programming bias for further evidence. Fig. 9 shows the programming behavior of devices at different compositions. A clear crossover from dipole switching for FE to charge trapping for AFE insulators is evident.

The threshold voltage shift in FE devices was retained in

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| extremely high pressure. However, a similar diffraction pattern | unbiased | state, | allowing | the | non-volatile | storage | of |

has been reported [10] for a rare orthorhombic phase with space group Pbc21 in Mg-doped ZrO2, which emerged when the t→m transformation was inhibited by external stress in nano-scale crystallites. Similar conditions may arise in capped thin films of HfSiO (Fig. 5). Since the chemistry of ZrO2 is almost identical to that of HfO2, the same phases occur in both oxides. The Pbc21 space group is not centrosymmetric and does therefore not exclude ferroelectricity. A fuller account of our investigations of ferroelectric HfO2 has been published in the meantime [11,12,13,14].

information. Extrapolation to 10 years yields a memory window of 650 mV (Fig. 10), which suggests the viability of long-term data storage. We note that this is an exceptionally long retention time for a FEFET which usually suffer from retention time loss due to imperfect interfaces to silicon.

To test the lateral scalability limits of this technology, we also manufactured short channel devices. Functional devices were observed down to 80 nm x 150 nm (WxL), the smallest structure on the mask set (Fig. 11, Fig. 7).

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| **Ferroelectric Field Effect Transistors** | **Conclusions** |

The high bond strength of ferroelectric HfO2 sets it apart from common ferroelectrics in several aspects: The high band gap and bad offsets allow for low leakage current even for very thin films below 10 nm. The excellent thermodynamic stability allows a direct contact to silicon and silicon dioxide. No noble metal electrodes or buffer layers are required as in earlier concepts [3].

Transistors were manufactured in a gate first scheme with a gate stack consisting of 1.2 nm thermal SiO2 interface, 5-9 nm

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| ferroelectric | HfSiO | insulator, | and | a | TiN | electrode. |

Crystallization of the HfSiO thin films was induced by a 1000 °C/20 s anneal in nitrogen after top electrode deposition. Both long and short channel devices were manufactured.

Fig. 6 compares the behavior of devices with ferroelectric and with antiferroelectric gate insulators during gate voltage sweeps and separate program and sense steps. The

We reported the formation of ferroelectric o-HfO2 in thin films and manufactured functional nano-scale FeFETs with promising electrical characteristics. Both lateral dimensions and dielectric thickness are at least an order of magnitude smaller than previously reported devices with conventional ferroelectrics (Fig. 12).

Both the extraordinary reduction in size and the improvement in device characteristics are driven by the vastly superior material properties in this application and suggest the viability of nano-scale FeFET memory based on FE-HfO2.

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| *experimental* | *work* | *was* | *performed.* | *S.* | *Jakschik* | *is* |

*acknowledged for processing the short channel device.*

antiferroelectric device is dominated by charge trapping, as **References**

evident from a clockwise hysteresis and a threshold voltage (Vt) shift in direction of the programming bias. This behavior can be ascribed to trapping of electrons from the channel region, a well-known behavior for devices with crystalline HfSiO based gate dielectrics [15]. The device with the ferroelectric gate insulator exhibits anticlockwise hysteresis and a Vt shift opposed to the threshold voltage. This behavior is evidence for a switchable dipole in the gate insulator (Fig. 7) and in agreement with the observation of ferroelectricity in MIM capacitors. Ferrolectric switching was observed in devices with gate dielectrics as thin as 5.5 nm. Fig. 8 shows the threshold voltage shift of such in a devices in dependence of polarity and bias for 1s pulses. At high negative programming bias, charge trapping from the channel overcompensates the Vt shift from the dipole. Therefore, -3V and 4V were chosen as

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| Uncapped | Capped | Capacitance [µF/cm²] | 4 | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | | | | |  |  |  |  |  |
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| Id [A]@Vd=25mV | Double Sweep 2V Double Sweep 4V    Gate Bias  Hysteresis | | | | | | | Gate Bias | Program | Sense | Program Sense | | Time |
| +4V | -3V | |
| Program + Sweep | | | | | |
| 25µ | 5.6mol% SiO2 | | | | | |
| 5.6mol% SiO2 | | | | '1' | |
| 20µ | AFE | | | | | | Initial Vt | | | | | |
| Program '1' -3V | | | | | |
| 15µ | | | | | | | Program '0' +4V | | | | '0' | |
| 10µ | | | | | | |
| 5µ | Hysteresis 2V | | | | | |
| Id [A]@Vd=25mV | 0 | Hysteresis 4V | | | | | | 3.1mol% SiO2 | | | | | |
| 25µ | 3.1mol% SiO2 | | | | | |
| 20µ | FE | | | | | | Initial Vt  Program '1' -3V | | | | '0' | |
| 15µ | | | | | | | Program '0' +4V | | | | | |
| 10µ | | | | | | | '1' | | | | | |
| 5µ | Hysteresis 2V | | | | | |
| 0 | Hysteresis 4V | | | | | | -1 | | 0 | | 1 | 2 |
| -1 | | 0 | 1 | 2 | 3 | 4 |
| Vg [V] | | | | | | | Vg [V] | | | | | |

Figure 6 Characterization of transistors with gate dielectrics that showed antiferroelectric (top row) and ferroelectric (bottom row) behavior in capacitors. The left column shows the drain current for a double sweep of the gate voltage. The right column shows gate-voltage sweeps for devices that were programmed with discrete pulses of 1s (limited by prober).

Figure 7 Top: transmission electron microscopy cross section of a short-channel transistor with FE-HfSiO. Bottom: schematic representation of charge carrier trap-ping and dipole switching leading to opposed Vt shifts.

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