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**Integration Challenges of Ferroelectric Hafnium Oxide Based Embedded Memory**

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One of the key challenges in the development of embedded memory solutions is to ensure their compatibility to CMOS processing and to reduce the added complexity to a minimum. Especially, the parallel implementation of charge based one-transistor memories in the FEoL, such as e.g. floating gate devices, together with advanced transistor technologies proves rather challenging. In contrast to that, an alternative one-transistor memory concept based on ferroelectric hafnium oxide closely resembles state of the art high-k metal gate devices and therewith promises a greatly simplified integration. Here, we investigate the impact of strain, thermal budget and work function engineering, usually applied to high-k metal gate technologies, on material properties as well as on the memory performance of hafnium oxide based ferroelectric field effect transistors. Key challenges related to a modified gate etch and the integration of different hafnium oxide thicknesses will be discussed.

**Introduction**

System on chip (SoC) embedded memory solutions promise small form factors and high operating speed, as well as a high energy and cost efficiency [1–3]. Single cell scalability and basic memory parameters such as data retention, cycling endurance and disturb characteristics on array level are important aspects in stand-alone memory development and can serve as a guideline for embedded solutions. However, one of the key aspects in embedded memory development is compatibility of the memory technology to its underlying complementary metal oxide semiconductor (CMOS) platform. This includes the voltage requirements for logic and memory operation, the need for additional lithographic steps and minimally CMOS invasive integration efforts, as well as the introduction of new materials and related contamination concerns. Especially, in state of the art high-k metal gate (HKMG) CMOS technologies at minimum feature size (F) these aspects prove rather challenging when searching for a suitable embedded memory solution. As a consequence, most emerging memory approaches result in large memory cells of multiple F2 or leave a back end of line (BEoL) integration of the memory cell as the only viable option [4].

With the introduction of ferroelectric hafnium oxide (FE-HfO2), however, a scalable one-transistor (1T) memory solution derived from the conventional HKMG transistor was presented for the 2X nm node [5]. The therewith close resemblance of the memory and logic transistor appears ideally suited for combining nonvolatile data storage and logic

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circuitry on the same chip. Nevertheless, in order to fulfill these expectations and to ease manufacturing issues this resemblance has to be as close as possible. In the context of a minimally invasive memory integration strategy this means that ideally the FE-HfO2 based memory transistor has to adapt to the HKMG transistor in terms of thermal budget and post treatments, vertical and lateral dimensions, the use of stress engineering, as well as metal gate and work function engineering. Based on experimental gate first ferroelectric field effect transistor and metal-insulator-metal capacitor data these aspects and embedded memory requirements are being analyzed and critically discussed.

**Experimental**

Hafnium oxide based ferroelectric field effect transistors were manufactured on 300 mm Si-substrates using a state of the art 28 nm gate first HKMG technology. The SiO(N) interfacial layer separating the FE-HfO2 layer from the Si-channel has a physical thickness of about 1.2 nm. The 10 nm FE-HfO2 layer consists of a thin undoped HfO2 layer stacked with a thicker silicon doped hafnium oxide (Si:HfO2) layer grown by atomic layer deposition (ALD) utilizing a metal halide based precursor system (HfCl4, SiCl4, water). The subsequent deposition of TiN, Poly-Si and the hard mask system for gate patterning completed the high-k metal gate stack. The dry etching of the gate stack was performed using a temperature adjustable susceptor.

Further material studies were performed on TiN-based metal-insulator-metal (MIM) capacitors. For the ALD of lanthanum doped hafnium oxide (La:HfO2) the metal organic precursor La(thd)3 in combination with the metal halide precursor HfCl4 was utilized. The deposition of hafnium zirconium oxide (HZO) and aluminium doped hafnium oxide (Al:HfO2) as well as Al2O3-laminated HZO was realized using the metal organic precursors TEMAHf, TEMAZr and TMA in combination with ozone.

**Results and Discussion**

The material and integratibility requirements an embedded hafnium oxide based FeFET has to fulfill are defined by the underlying CMOS platform. The stability within the thermal budget during CMOS processing as well as a feasible gate patterning are the most important among these requirements since they cannot be circumvented. However, when considering the simplification and cost benefit of processing logic and memory transistor in parallel for as many steps as possible, additional requirements such as compatibility to stress and work function engineering as well as a combined ALD of logic and memory dielectric are highly desired. Due to FeFET scalability considerations [6], the presented results are primarily aimed for an implementation in a gate first environment.

Thermal Budget Requirements

The thermal stress the FE-HfO2 has to endure depends on the HKMG technology used for CMOS processing. This requires ferroelectric phase stability and therewith remanent polarization (Pr) in hafnium oxide to be independent of annealing temperature and thermal stress during gate formation and implant activation anneals. Even though in a first approximation the threshold voltage shift of a FeFET is only defined by the thickness of the ferroelectric dFE and the coercive field strength Ec, the remanent polarization plays a crucial role in the formation of a ferroelectric memory window

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(MW). Figure 1 shows numerical simulations of the hafnium oxide based FeFET based

on the formalism described by Miller and McWhorter [7].

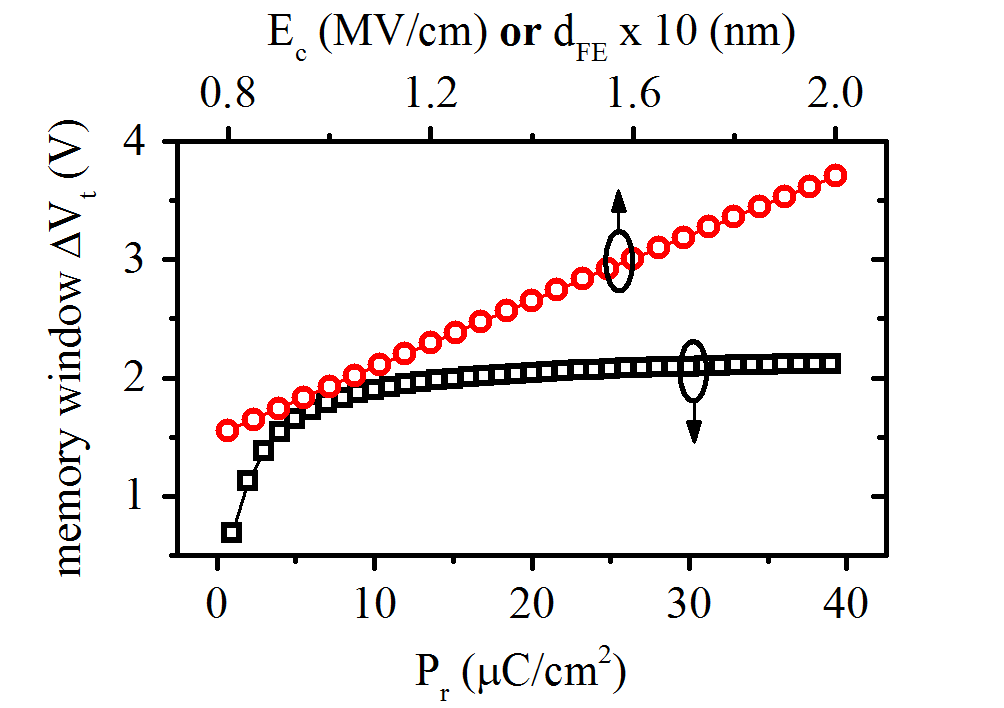


Figure 1**.** Numeric simulation of FeFET memory window dependence on coercive field strength Ec, ferroelectric film thickness dFE and remanent polarization Pr. Simulation input parameters are derived from the actual FE-HfO2 based FeFET described in the experimental section.

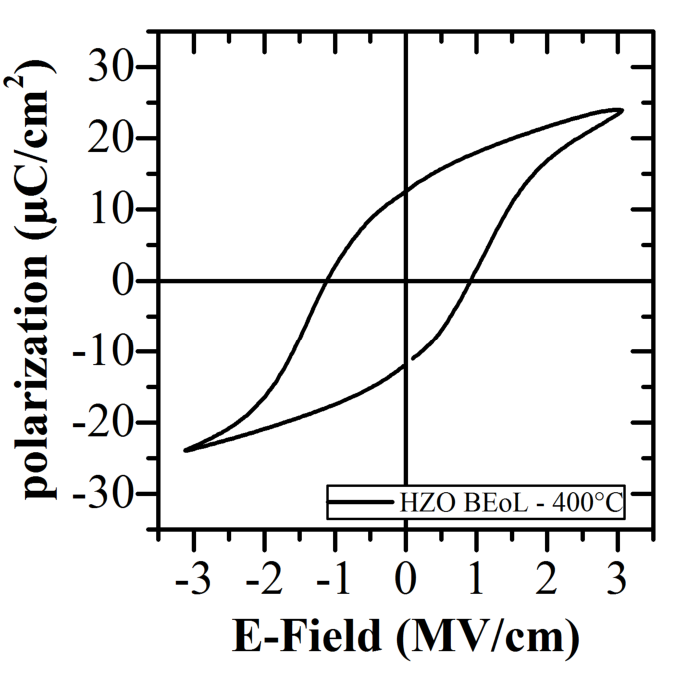


Figure 2**.** Polarization-voltage hysteresis

of a TiN-based BEoL MIM capacitor

containing a 8 nm thin HZO layer

crystallized during standard thermal

processing of a Cu back end.

The proportional dependence of the memory window on dFE and Ec is clearly observed in Figure 1. However, as Figure 1 further shows, this simple and exclusive relation is only valid if Pr does not fall below a certain threshold. Above this threshold the memory window becomes independent of Pr, whereas below this threshold the memory window rapidly decreases. Evolution of the memory window with switching cycles showed that this effect is critical within the first 100-1000 switching cycles of a pristine device [8]. Overall, this motivates the search for a material with reasonable Pr stability despite high or low annealing conditions.

For a gate last based transistor technology a FE-HfO2 based system has to be identified that crystallizes within the limited thermal budget of BEoL (~ 400-500 °C) processing, whereas in the case of a gate first approach the material optimization has to be focused on high temperature stability (>1000 °C). In the former case the comparably low crystallization temperature of the HZO solid solution [9] and the gadolinium doped hafnium oxide system [10] emerges as a viable solution. In this context Figure 2 demonstrates a ferroelectric polarization hysteresis obtained for a HZO layer crystallized within the thermal budget of BEoL processing without further annealing.

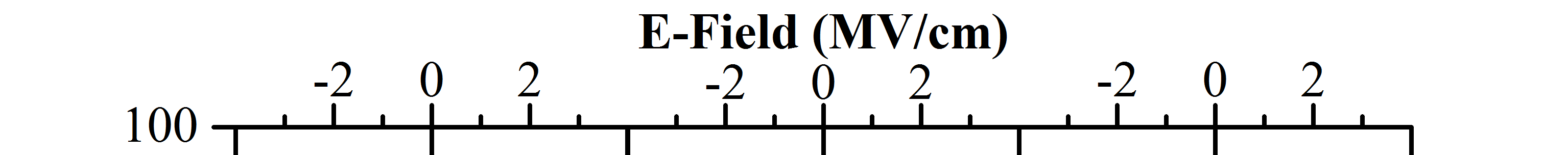
In the latter case of a gate first processing the crystallization temperature is no longer a decisive factor, so that in general, the utilization of all known FE-HfO2 based systems should be possible [11]. The applicability of alternative hafnium oxide based ferroelectrics at high annealing conditions will be discussed in the following.

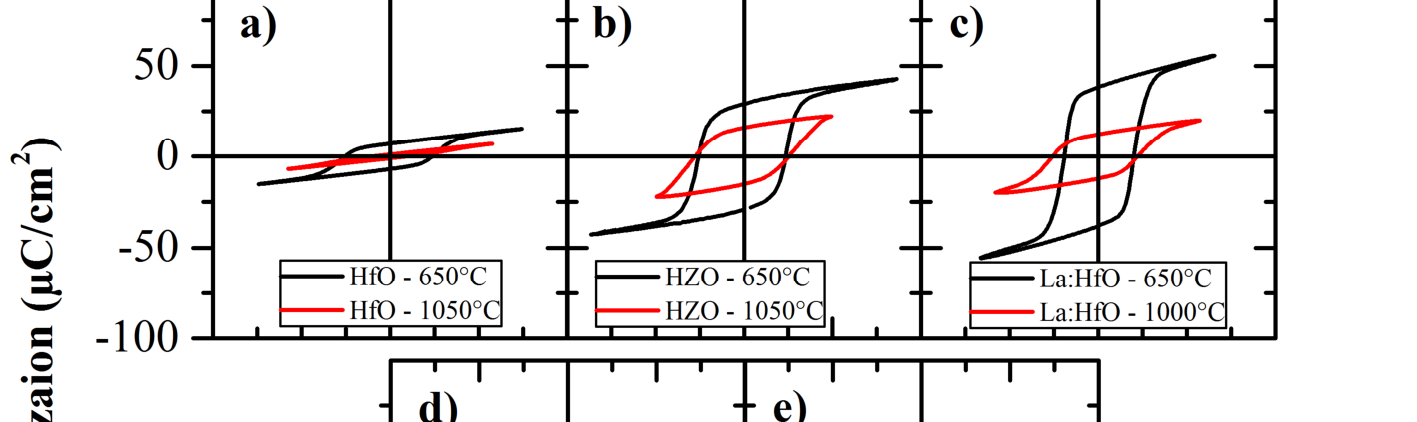
Si:HfO2 was the first hafnium oxide based ferroelectric being discovered [12] and therewith the natural choice for a first implementation into a gate first FeFET technology [13]. The observed ferroelectric threshold voltage shift as well as the fast switching kinetic in the nanosecond range provided the proof of concept for this technology and suggested the high thermal stability of the Si:HfO2 in a gate first environment. Additional

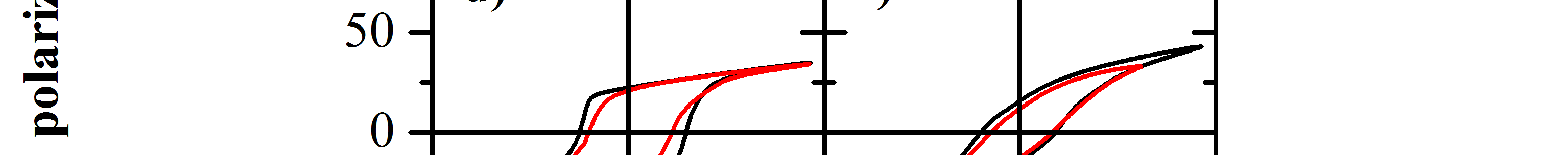
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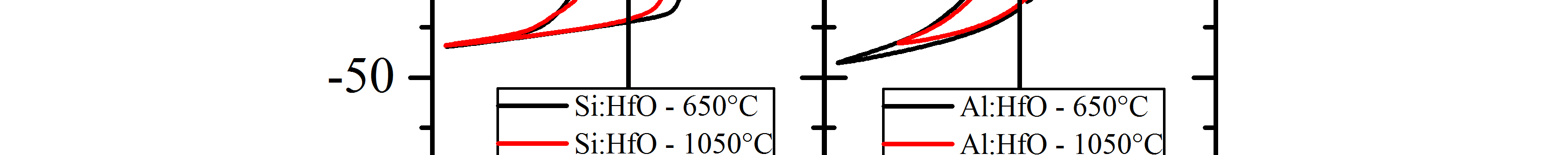
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proof for the high ferroelectric phase stability in Si:HfO2 is provided by MIM capacitor results in Figure 3d. Here the electrical polarization-voltage results extracted from a 10 nm Si:HfO2 film exposed to a post metallization anneal at 650 °C for 1 s and a gate first like anneal at 1050 °C for 1 s are shown. It becomes apparent that despite these markedly different annealing conditions no significant change in the polarization voltage hysteresis can be detected.









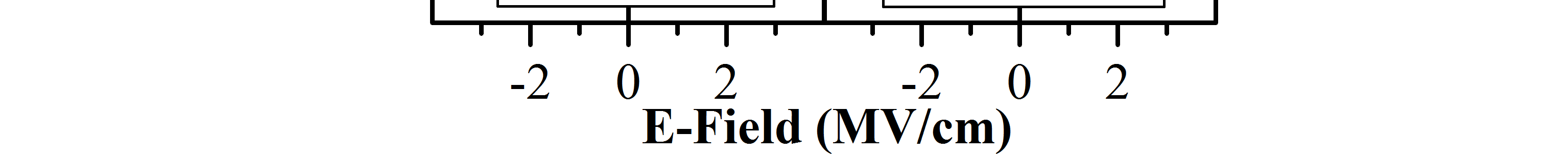


Figure 3**.** Polarization-voltage hysteresis of TiN-based MIM capacitors for different annealing conditions containing 10 nm thin (a) undoped HfO2 (b) HZO (c) La:HfO2 (d) Si:HfO2 and (e) Al:HfO2.

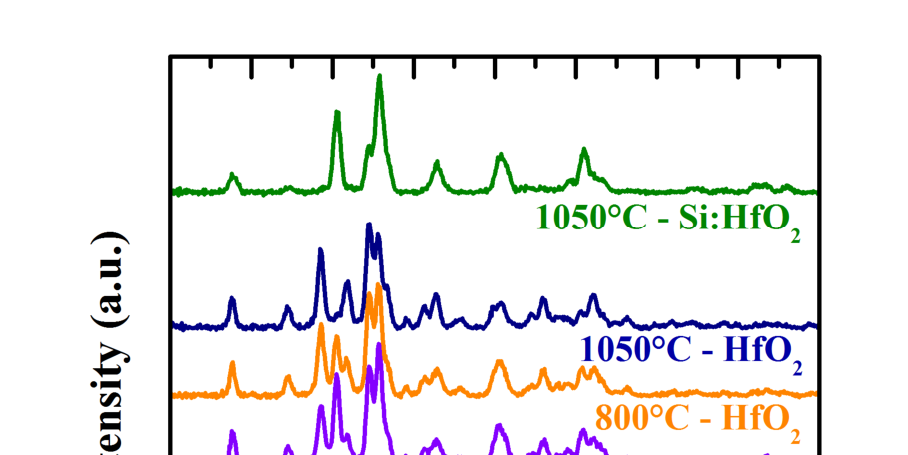
Nevertheless, considering the large and still increasing number of FE-HfO2 based systems available today, the question arises if Si:HfO2 is still the ideal choice for FeFET implementation. Especially the large Pr reported for La:HfO2 suggests a high ferroelectric phase fraction and therewith promises improved cell to cell variability for aggressively scaled FeFETs at the nanoscale [11]. Furthermore, utilizing undoped HfO2, which was recently confirmed to be ferroelectric within certain boundary conditions [14], promises a facilitation of the manufacturing process by eliminating the need for a dopant ALD precursor and the elimination of the accompanying device variability as a result of macroscopic dopant fluctuations across the wafer. A similar advantage is expected for the HZO system, which in contrast to Si:HfO2 shows a broad compositional range of ferroelectric phase stability [9].

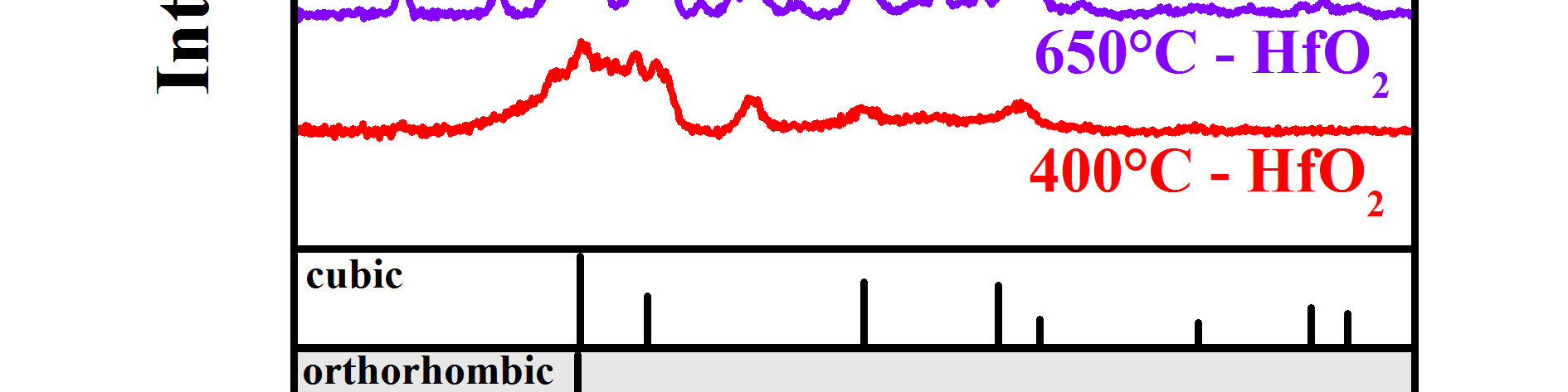
However, despite these clear advantages the MIM capacitor results of all three systems depicted in Figure 3a-c reveal their limited applicability to gate first FeFET technology. While at a medium annealing temperature of 650 °C the clear advantage of La:HfO2 in terms of remanent polarization is still visible, a sever degradation of Pr at an annealing

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temperature of 1050 °C has to be accounted for. In the case of the undoped HfO2, the already at 650 °C annealing temperature lowered Pr almost completely vanishes when increasing the annealing temperature to 1050 °C. This electrical degradation of undoped HfO2 is clearly reflected in a structural transformation to the monoclinic phase with increasing annealing temperature (Figure 4). The stable orthorhombic phase structure of silicon doped hafnium oxide at 1050 °C is shown for comparison.





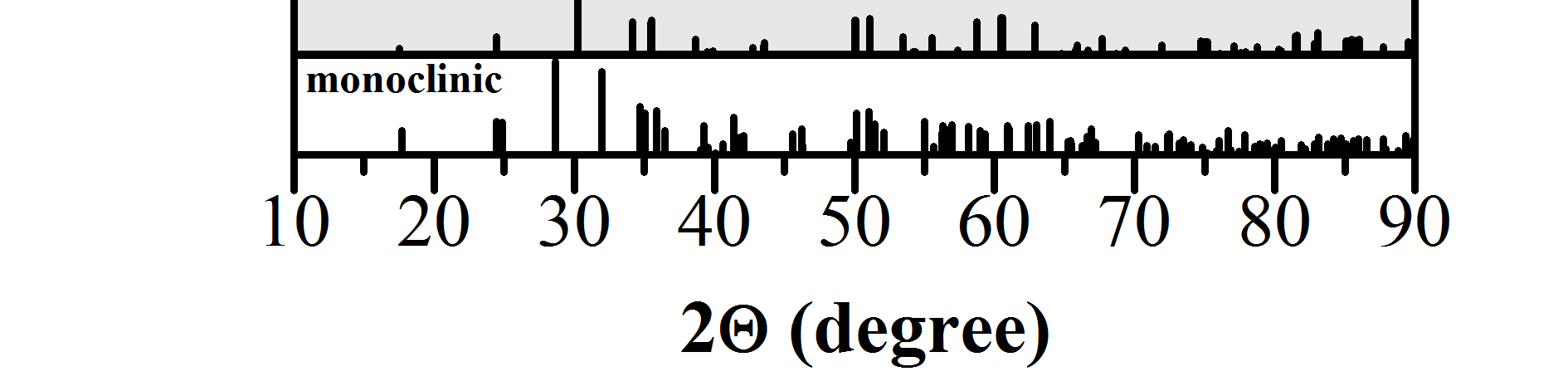


Figure 4**.** GIXRD analyses of 10 nm thin undoped HfO2 thin films for different annealing conditions. For the highest annealing condition the diffraction pattern of Si:HfO2 is included for reference. Database powder diffraction patterns are given for orientation and to assist phase identification.

A comparable degradation of polarization is observed for HZO (Figure 3b). This system has the lowest crystallization temperature of all materials investigated here and was dominated by a severely increased leakage current when annealed at 1050 °C. A leakage compensation technique described in [15] was utilized to extract a reliable polarization hysteresis.

Al:HfO2 on the other hand has a high crystallization temperature, which is comparable to that of Si:HfO2 [16]. The electrical results of this material system with respect to the aforementioned annealing conditions are also depicted in Figure 3e. No significant degradation of Pr can be detected when exposed to a gate first like thermal budget. These results suggest Al:HfO2 as a viable alternative for Si:HfO2. However, even though the TMA precursor used for in-situ doping of aluminum is clearly superior to any available silicon precursor in terms of ALD capability, no clear advantage is expected. The reason for that is the high growth rate of TMA, which does not allow fine tuning of doping concentration by the commonly applied ALD super cycle methodology. Especially in the case of the aluminum and silicon doped hafnium oxide this precise control of doping

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concentration was found to be crucial to achieve adequate ferroelectric phase stability [16] [12].

An alternative approach to preserve electrical quality in dielectrics despite thermal treatments is laminating the ferroelectric thin film as illustrated in Figure 5. Following up on the approach developed during the reliability optimization of ZrO2 based DRAM dielectrics [17] a laminated structure is introduced to stabilize the system in terms of preventing extensive grain growth and leakage path formation during high temperature annealing. Here we show electrical results of 10 and 15 nm HZO thin films interrupted by one and two layers of Al2O3, respectively. In accordance with [18] it is clearly observed that in spite of this interlayering, ferroelectric phase stability can be preserved. In addition to that, superior robustness in terms of Pr preservation at gate first like thermal conditions can be demonstrated for the laminated systems. Transferring this stabilization approach to other hafnium oxide based ferroelectrics might broaden the range of materials available for gate first FeFET implementation.

Figure 5**.** Polarization-voltage hysteresis and TEM micrographs of TiN-based MIM capacitors containing (a) 10 nm HZO, (b) 2x5 nm HZO laminated with a single layer of Al2O3 and (c) 3x5 nm HZO separated by two layers of Al2O3.

Gate Patterning

The integration of the FeFET gate oxide is challenging the transistor patterning due to the high physical thickness of the ferroelectric layer. Compared to hafnium oxide with less than 4 nm thickness, as usually applied for CMOS transistors, the ferroelectric Si:HfO2 requires several optimizations of the etch process, while compatibility to standard metal gate etch processing has to be secured. This includes the hard mask stack and patterning, the etching of Poly and TiN layers as well as the impact of dopants in hafnium. The patterning concept may be setup using the standard hard mask stack and etch processes for metal gates. However, the hafnium oxide etch process has to be adjusted to a higher thickness by providing higher selectivity to the interfacial oxide and hard mask material.

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Based on a BCl3 chemistry an optimized process was found capable of dealing with the silicon dopant in hafnium oxide and the higher stack thickness, while the profile geometry was optimized for steep sidewall angles.

Figure 6 shows the influence of the silicon dopant in hafnium oxide during etching of amorphous and crystalline samples. The hafnium oxide etch rate shows a strong dependency with increasing concentration of silicon and approaches the etch rate of thermally grown SiO2 at a Si content above 50%. By carefully choosing the etch gas composition and increasing the etching temperature, the etch rate could be maximized for relatively small silicon contents, like they are applied to stabilize the ferroelectric HfO2 phase. This resulted in an improved selectivity to the hard mask and the SiO(N) interface, which is necessary to stop the gate etch process at the bulk silicon. The etch temperature is a sensitive parameter to improve the total etch rate while isotropic etch rate is significantly increased in order to optimize the gate profile. As shown in Figure 6, the etch rate of crystalline Si:HfO2 is significantly smaller compared to amorphous Si:HfO2 under otherwise identical conditions. If an integration scheme is applied which involves a crystallization of the HfO2 before the gate etching, as it is usually the case for most gate first integration schemes, increasing the etching temperature enlarges the process window in terms of selectivity and etch rate.

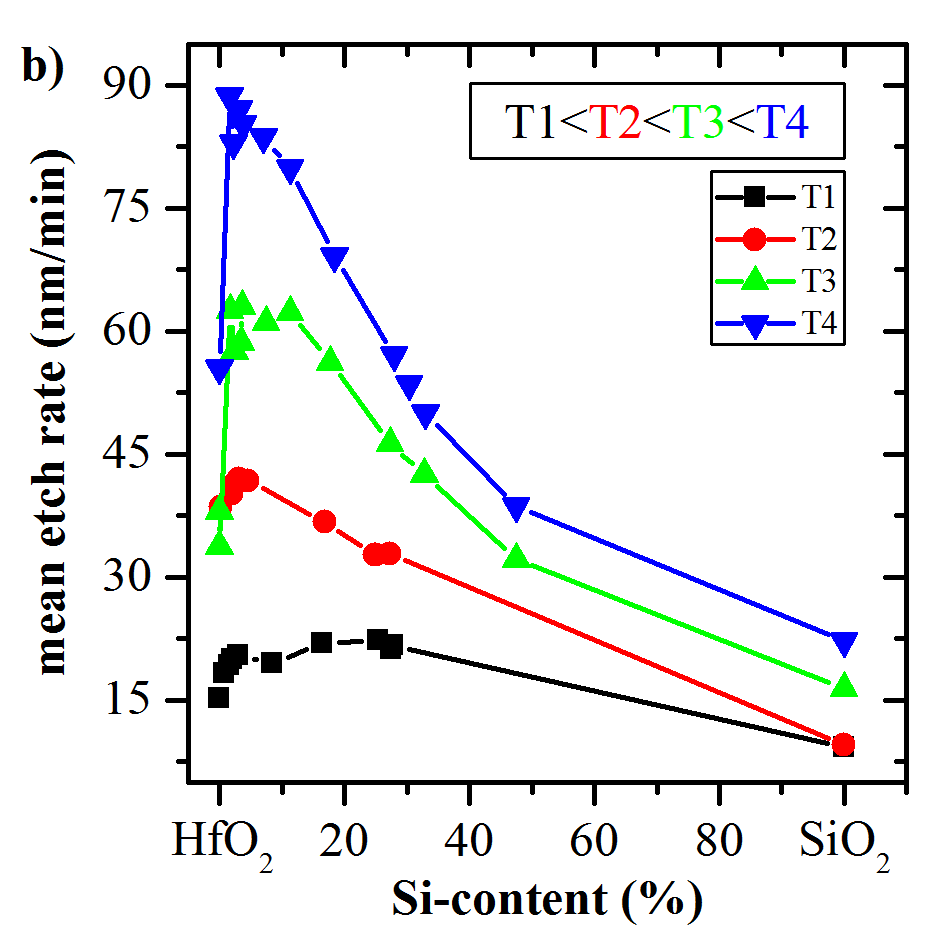
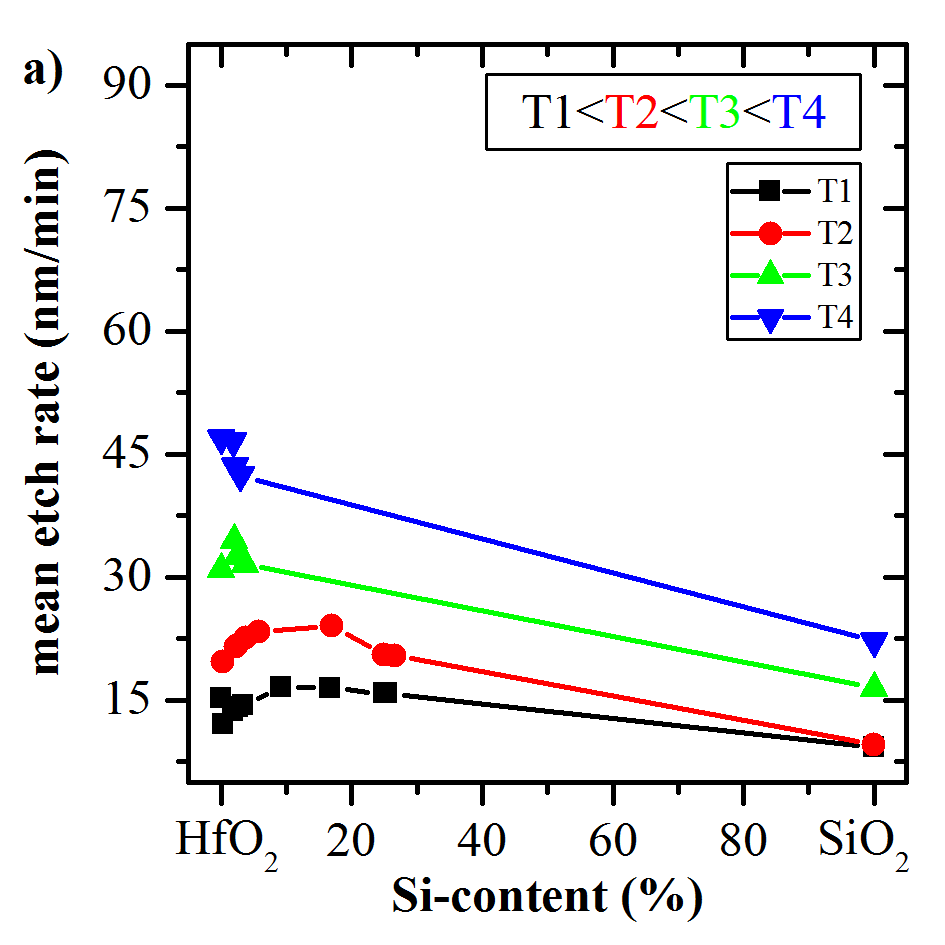


Figure 6**.** Etch rate during gate patterning plotted as a function of silicon content Si:HfO2 and susceptor temperature for (a) crystalline and (b) amorphous Si:HfO2.

First patterning tests on Si:HfO2 based FeFET gate stacks resulted in a high TiN undercut (Fig. 7a), which was already observed when using elevated temperatures for gate patterning of charge trapping devices [19–21].

Hence, the TiN etch profile was optimized and a sidewall protection liner was used to avoid a TiN undercut during Si:HfO2 etch (Fig. 7b). After stabilization of the Poly/TiN profile the Si:HfO2 etch had to be optimized to decrease footing. This footing is a critical issue for subsequent deposition of liners and etching of the contacts. However, as can be seen from Figure 7c, a steep sidewall angle and strongly reduced footing can be achieved by adjusting the electrostatic chuck temperature as well as the HfO2 etching process parameters.

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Figure 7**.** Gate patterning TEM micrographs of a Si:HfO2 based FeFET (a) with a strong TiN undercut, (b) with a TiN protection liner and (c) an adjusted etching temperature and optimized Si:HfO2 etch step.

Compatibility to CMOS Processing and Shared Process Steps

In the previous section the necessity of an adjusted gate etch for the patterning of the thicker ferroelectric hafnium oxide was addressed. Even though this gate etch module has to be kept separate, it is still highly desired that besides this marked difference the FeFET memory transistors share as many process steps with the standard CMOS transistors as possible. The most important aspects of such a simultaneous processing will be addressed in the following.

A great simplification of the parallel memory and logic transistor processing can be achieved by using a combined stack consisting of the logic and ferroelectric memory dielectric in the area of the memory array as suggested in [22]. This approach allows for multiple integration pathways in gate first as well as gate last technologies. The feasibility of this integration approach is demonstrated in Figure 8a, showing the counter clockwise transfer characteristic of a ferroelectric hafnium oxide based FeFET containing the silicon doped hafnium oxide and the thin work function modified logic dielectric within the same gate stack.

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Figure 8**.** (a) Id-Vg hysteresis of a FeFET combining a thin undoped HfO2 layer and a thick Si:HfO2 layer within the same gate stack. Program and erase voltages were set to ±5 V. (b) Cumulative probability plots of ferroelectric MW distribution extracted from a small NOR array for differently processed (details are described in the main text) Si:HfO2 based FeFETs.

Despite these modifications a ferroelectric memory window comparable to stand alone Si:HfO2 FeFETs can be extracted [5].

Further modifications derived from this approach denoted as reference are depicted as a memory window distribution plot in Figure 8b. It is clearly observed that ferroelectric memory functionality can be maintained when adding additional standard gate first processing steps. This includes the addition of a work function metal drive in anneal and adjusting the stress liner from tensile to compressive. These results show that the ferroelectric hafnium oxide based FeFET provides the robustness required for maintaining the stress and work function engineering usually applied during gate first CMOS processing.

Whereas the aforementioned transistor modifications have only limited impact on the FeFET functionality, a severe impact of the silicon doping concentration on the memory window distribution can be detected (Figure 8b). Even though the difference between the high and the low doping is only ~2 mol% of silicon, a significant degradation of the statistics can be observed when the ideal doping concentration is not met. This is due to the high sensitivity of Si:HfO2 ferroelectric phase stability on silicon content and motivates the already addressed search for a material with a broader compositional range.

**Conclusions**

One-transistor ferroelectric memory cells based on hafnium oxide emerge as a straightforward embedded memory solution for advanced high-k metal gate CMOS technologies. The close resemblance of the ferroelectric memory transistor gate stack to that of the conventional CMOS device as well as its robustness with respect to the performance engineering applied to the logic device allows for multiple shared process steps greatly reducing manufacturing costs. The gate etch module, remaining dedicated to the memory gate stack, can be handled utilizing advanced high temperature gate etch technology.

The high thermal stability requirements of gate first transistor processing are met by Si:HfO2, which at the same time shows a disadvantageously high sensitivity of

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ferroelectric phase stability on silicon content. HZO base systems and its laminates with Al2O3 are suggested as a material alternative with a broad ferroelectric composition range and the ability to cover the thermal requirements reaching from low temperature gate last to high temperature gate first processing.

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