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Demonstration of a p-Type Ferroelectric FET

With Immediate Read-After-Write Capability

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***Abstract— In this letter, p-type ferroelectric field-effect-transistors (FeFETs) based on HfO2 and embedded in GlobalFoundries 28 nm bulk high-k metal gate (HKMG) technology (28SLPe) are systematically investigated and compared to their n-type counterparts. We show that the two device types, based on Si channel, exhibit a symmetric memory window (MW) and very similar switching behavior, yet profoundly different trapping kinetics. In contrast to n-FeFETs, p-FeFETs display a full MW immediately after the write operation and apparently no parasitic electron trapping. Based on this, we demonstrate an immediate read-after-write operation. Finally, we illustrate how slight struc-tural changes of the gate stack, such as the introduction of the SiGe channel material, can enhance charge trapping and nullify the above-mentioned advantages.***

***Index***  ***Terms— Ferroelectric***  ***field-effect***  ***transistor (FeFET), hafnium oxide, charge trapping, ferroelectric memories, n-FeFET, p-FeFET.***

I. INTRODUCTION   
**F** on ferroelectric (FE) HfO2 [1] are promising can- ERROELECTRIC field-effect transistors (FeFETs) based

didates for future applications ranging from non-volatile

memory [2], [3] to neuromorphic [4]–[6] and computing-

in-memory concepts [7]–[9]. FeFETs not only offer low-power

and fast switching, but also are fabricated in a CMOS com-

patible process [2], [3], [10]. While prior research has mainly

focused on the n-type FeFET, little research has been reported

on CMOS compatible p-type devices [11]–[14]. To increase

the versatility of the FeFET circuit design and to enable Fer-

roelectric CMOS (FeCMOS), especially in view of emerging

computing applications, also the integration of a p-type FeFET

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is highly required. Both n-type and p-type devices essentially use the same field-effect induced by a FE layer in the gate stack which can have two different but stable polarization states. As a result, two logic states can be distinguished by a shift in the threshold voltage (*VT )* of the transistor.

However, parasitic charge trapping is one of the challenges the FeFET is currently facing. Positive gate voltages during write operations induce electron trapping in proximity to the HfO2-SiO2 interface, which results in a shifted *VT* and a severely reduced memory window (MW) directly after the write operation. This is caused by the electrons screening of the FE polarization and its effect onto the channel. The MW recovers only gradually in time as the trapped electrons are released from the gate stack [15]–[17]. Hence a delay of a few hundreds of milliseconds between write and read operation is necessary to clearly distinguish the *VT* states. Although the de-trapping time and the consequent read latency can be significantly accelerated by suitable de-trapping electrical pulses [18], it is desirable to reduce parasitic charge trapping in the first place. This would enable a minimized read latency, essential for fast and real-time computation with FeFETs.

In this letter, the immediate read-after-write in p-type FeFETs on Si substrate is demonstrated. The comparison to the n-type FeFET conterparts in terms of trapping kinetics, MW and switching performance is explored. The impact of variations in device fabrication, such as the introduction of the CMOS compatible SiGe substrate and its detrimental effect on the read delay, is revealed for both p- and n-type FeFETs. Finally, a stable data retention is demonstrated for p-FeFETs on Si substrate.

II. EXPERIMENTS AND RESULTS

Experiments were performed on FeFETs fabricated by GlobalFoundries in a 28 nm bulk high-k metal gate CMOS technology with a gate-first approach. The schematic structures of the n- and p-type FeFETs are illustrated in Fig. 1(a) and (b), respectively. The gate-stack consists of a TiN gate electrode, an ∼10 nm thick doped HfO2 FE layer and an ∼1 nm thick SiO2 interfacial layer. The Si substrate is p-doped in the n-type FeFET and n-doped in the p-type FeFET construction. The channel length (*L)* and width (*W)* of the tested devices are 450 nm and 450 nm, respectively.

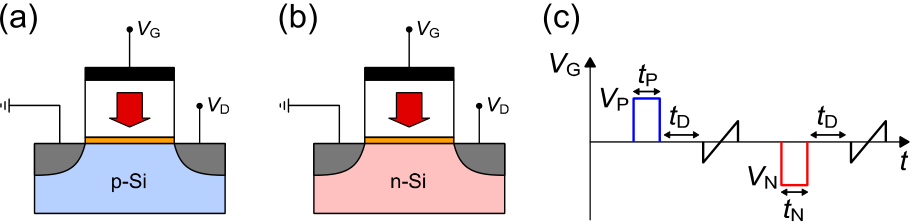
Electrical characterizations were performed at room tem-perature with fast pulsing measurements using a Keithley

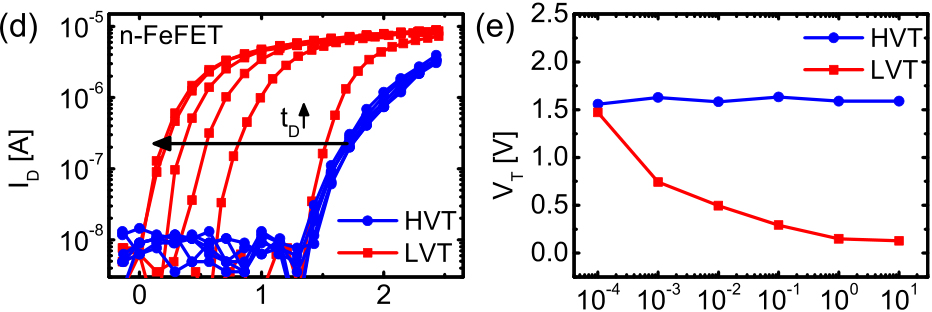
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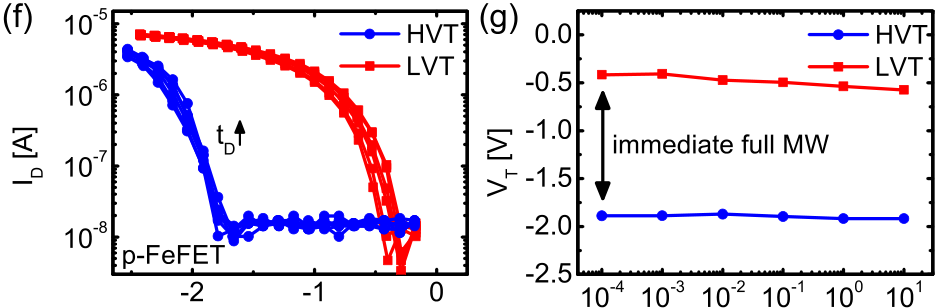


Fig. 1. Sketch of the (a) n-FeFET and (b) p-FeFET structure and its terminals. (c) Gate voltage (VG) waveform for write and read operations. Read operation is performed while applying a constant drain voltage (VD) of VD = 100 mV for n-type FeFETs and VD = −100 mV for p-type FeFETs. ID − VG characteristics of (d) n- and (e) p-FeFETs for different delay times and extracted corresponding threshold voltages (f) and (g). The used write pulse amplitudes are VN = −4.5 V and VP = 4 V with tN = tP = 1 *µ*s.

4200-SCS Semiconductor Analyzer. The write and read oper-ations are schematically displayed in Fig. 1(c). During read, the drain current (*ID)* is measured utilizing a fast gate voltage (*VG)* sweep with a total duration of 100 *µ*s, whereas the polarity of the sweep was adjusted according to the n- or p-type device. The *VT* is extracted at *ID* = 100 nA. Write operations are achieved by applying sufficiently large negative (*VN)* and positive gate voltages (*VP)*, while all other terminals are grounded, resulting in a remanent polarization in the FE pointing up or down, and a respective *VT* shift. Due to the devices differing polarity these two differing polar-ization states define the high-*VT* (HVT) and low-*VT* (LVT) states of the n-FeFET while yielding the LVT and HVT states of the p-FeFET, respectively. The MW is calculated as MW = |HVT - LVT|. To study the read latency after a write pulse, a delay time *tD* between the write and the following read is inserted (Fig. 1(c)) and varied from 100 *µ*s to 10 s. Fig. 1(d) and (f) shows the *ID-VG* characteristics of the n-FeFET and p-FeFET, respectively, for both states HVT (blue) and LVT (red) at different *tD*. The dependence of the corresponding *VT* is shown in Fig. 1(e) and (g). Notably, the full MW (after *tD* = 10 s) for both devices is approximately the same and is around 1.5 V, so that no interface adjustment is needed, contrarily to what proposed in [13]. However, the two devices exhibit a completely different behavior in terms of electron de-trapping. The n-FeFET shows the typical behavior as e.g. observed in [16], [18], [19]. While the HVT state characteristics are not influenced by *tD*, the LVT state characteristics experience a

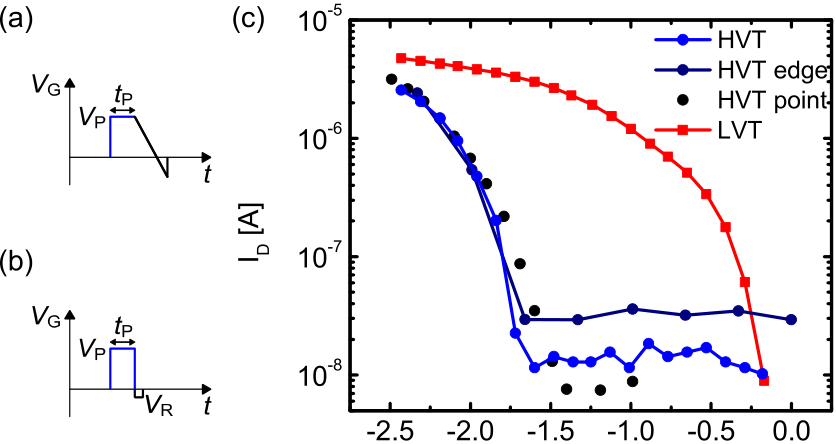




Fig. 2. (a) Gate voltage (VG) waveforms for fast write and read operations, measured on the falling VG-edge a) and as single measure-ment points (b). (c) ID-VG characteristics measured under different read conditions.

significant shift with *tD*, so that *VT* evolves from 1.5 V to 0 V as *tD* increases from 100 *µ*s to 1 s. This originates from the electrons trapped by the positive gate pulse necessary to set the LVT state. The trapped electrons require several hundreds of ms to be released from the gate stack again (de-trapping phase), after which the fully saturated LVT state can be observed, yielding the full MW. In marked contrast to this, the p-type FeFET apparently exhibits no de-trapping phase, so that the LVT and HVT characteristics are independent of the *tD* (Fig. 1(f)) and do not show any shifts of the *VT* (Fig. 1(g)). In other words, the full MW is available immediately after the write operation, indicating the immediate read-after-write capability.

To validate this and to exclude the possibility of any mea-surement artifacts or disturbs in Fig. 1(f-g), we perform two additional tests shown in Fig. 2(a) and (b) in order to assess the *VT* immediately after the positive *VG* pulse. Fig. 2(a) depicts a fast readout scheme that collects the *ID*-*VG* on the falling edge of the positive gate pulse to exclude any delay between the write and read. Fig. 2(b) shows another delay-free readout scheme wherein a single short gate-pulse of amplitude VR with a total length of 20 *µ*s is applied immediately after the write pulse rather than a *VG* sweep. Such single point measure-ments are repeated at different VR to capture the full *ID*-*VG*. Fig. 2(c) shows the comparison between *ID*-*VG* curves from the measurements of Fig. 1(f) at *tD* = 0.1 s and the *ID*-*VG* curves from the delay-free experiments in Fig. 2(a) and (b). As this test yields coinciding measurement results, immediate read-after-write for p-FeFETs could be confirmed.

While the fastest read capability in this work was restricted to a few tens of microseconds due to the external tester setup, a full in-chip setup can yield a much faster write and read speed in the tens of nanoseconds regime [3].

Another important metric of a FeFET is its switching kinet-ics, i.e. switching voltage and time. Fig. 3(a) and (b) shows the results of switching experiments performed with the write/read scheme in Fig. 1(c), where *VN* and *VP* are varied while *tN* = *tP* = 1 *µ*s. It can be seen that *VP* ≈ 3.5 V and *VN* ≈ −4 V are required for the p-FeFET to complete LVT → HVT and requires very comparable voltages for the same transitions of HVT → LVT transitions, respectively. Similarly, the n-FeFET the polarization in the FE layer. Displayed in Fig. 3(c) is the switching time *tS* as a function of *VG* amplitude required to

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1776 IEEE ELECTRON DEVICE LETTERS, VOL. 42, NO. 12, DECEMBER 2021



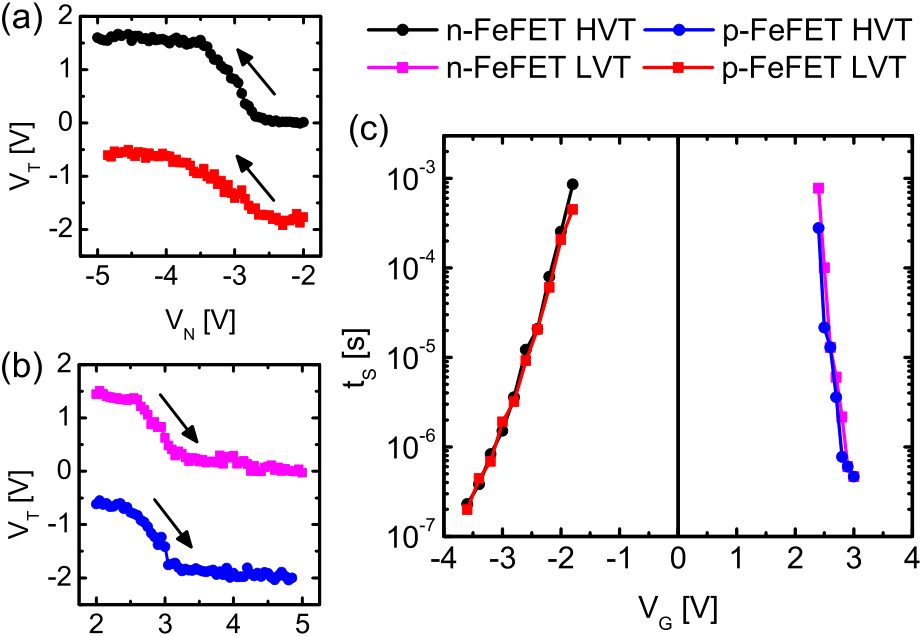




Fig. 3. p-FeFET switching into HVT- (a) and LVT-state (b) and n-FeFET switching into LVT- (a) and HVT-state (b) with increasing VG amplitude. (c) Switching time tS as a function of VG amplitude required to shift the VT by half the MW, as described in [19].

shift the *VT* by half the full MW, procedure as described in [19]. As the transitions of both devices exhibit coinciding values both for the switching voltage and the switching time, this indicates almost identical switching kinetics for the two device types. Therefore, these results exclude the hypothesis that the differences in switching kinetics are responsible for the striking discrepancies in de-trapping behavior in Fig. 1. Hence, the differences should be sought in dissimilar trapping probabilities for the p- and n-type gate-stacks.

Although only little attention has been dedicated to this topic, because p-type transistors are generally not exposed to a positive gate stress, some previous studies on conventional p- and n-MOSFETS have already shown that the former are much less prone to the *VT* degradation under positive bias compared to the latter. The main contributors of this *VT*

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| instability were identified as the positive charge injected from |

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| the gate side and the negative charge (electrons) injected from |

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| the substrate in the accumulation regime of the p-MOSFET. |

Nevertheless, it has been found that several factors, such as geometry effects, unfavorable energetic levels for electron trapping as well as shorter emission times for already trapped electrons, give rise to a lower *VT* degradation upon electron trapping in p-MOSFETs [20]–[24]. It is therefore very likely that this explanation also applies to the absence of *VT* shifts for our p-FeFETs under positive write voltages.

Nevertheless, although this result indicates that p-FeFETs might be more suitable for memory devices compared to the n-FeFETs, still a great caution is needed when fabricating these devices. So far, we have presented the results with

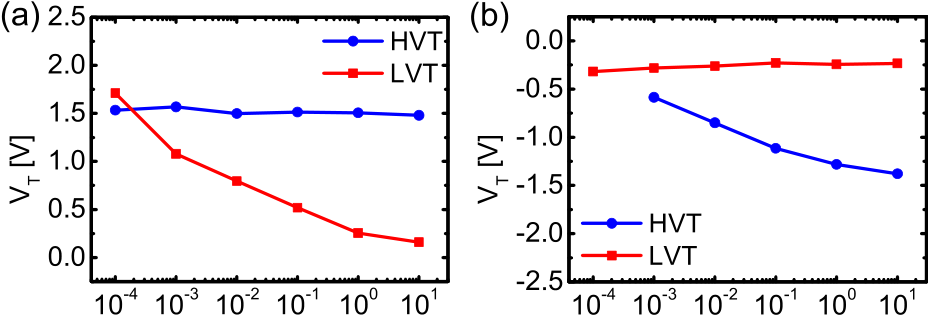


Fig. 4. Threshold voltages for different delay times for (a) n-FeFET and (b) p-FeFET with a SiGe channel.

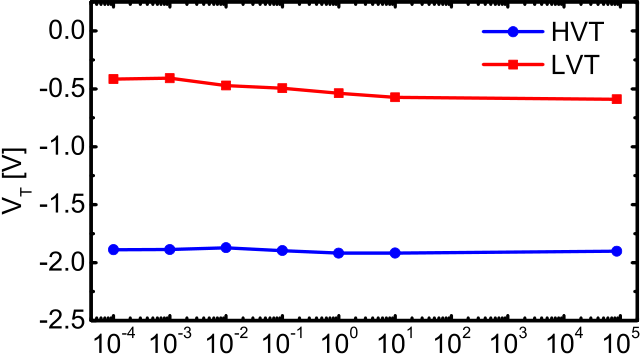




Fig. 5. Retention of the two distinct VT states for p-FeFETs with a Si channel for delay times up to 24 h.

slight structural and compositional changes can impair the advantages of a p-FeFET, and give rise to increased trapping characteristics, calling for a careful device design.

In addition to the abovementioned device characteristics one key figure of merit of the FeFET as an emerging memory device is its data retention. Fig. 5 displays the data retention characteristics of the two distinct states for p-FeFETs with a Si channel. We report a stable data retention for times up to 24 h indicating that the studied device not only features a full MW available immediately after the write operation but also retains its state over a longer period of time.

III. CONCLUSION

We investigated and revealed drastically different parasitic trapping characteristics in Si-channel p- and n-type FeFETs based on FE HfO2. While the latter show typical MW screen-ing and require hundreds of milliseconds of delay between write and read, the former feature a full MW immediately after the write, thus yielding an immediate read-after-write. We showed that the two device types have symmetric MW and very comparable switching behavior, so that the differences in trapping behavior most likely originates from energeti-cally unfavorable electron trapping in p-FeFETs. Nevertheless, slight changes in interface quality, e.g. through the use of SiGe as the channel material, can enhance the parasitic trapping, thus nullifying the presented advantages and calling for careful

devices having Si as the substrate material. However, Fig. 4 device design.

shows the same experiment of Fig. 1 for devices having SiGe (Ge content of ∼30%) as the channel material (as it is commonly done in classical p-FETs in order to increase the hole mobility). Now, not only the n-FeFETs but also p-FeFETs exhibit a significant dependence of *VT* on *tD* and have a very pronounced de-trapping phase. This observation can be explained by the increased defect density due to the lower quality of the interface layer grown on SiGe and the therefore increased trap density [25]–[27]. Hence, even such

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