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Recovery of Cycling Endurance Failure in

Ferroelectric FETs by Self-Heating

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***Abstract— This letter investigates the impact of self-heating on the post-cyclingfunctionalityof a scaled hafnium oxide-based ferroelectric field-effect transistor (FeFET). The full recovery of FeFET switching properties and data reten-tion after the cycling endurance failure is reported. This is achieved by damage annealing through localized heat-ing, which is intentionally induced by a large current flow through the drain (source)*−*body p*−*n junctions. The results highlight that the local thermal treatments could be exploited to extend the cycling endurance of FeFETs.***

***Index***  ***Terms— Ferroelectric***  ***field-effect***  ***transis-tor (FeFET), hafnium oxide, cycling endurance, self-heating, failure recovery.***

I. INTRODUCTION   
**T** ferroelectric hafnium oxide (HfO2*)* is currently being HE ferroelectric field-effect transistor (FeFET) based on

considered as a possible candidate for embedded nonvolatile memory [1]. Moreover, its particular switching behavior has

recently inspired several proposals for unconventional appli-cations, including artificial neurons [2] and synapses [3], [4],

ferroelectric oscillators [5], logic-in-memory devices [6], [7] and random number generators [8]. However, FeFETs have

a rather limited cycling endurance, which typically ranges between 104and 107cycles [9]–[13], depending on the struc-

ture, fabrication and cycling process. The related degradation has been mainly attributed to the wear-out of the interface

between HfO2 and silicon, driven by the charge trapping upon the bipolar voltage cycling [14]. Such a limitation might be

the main bottleneck for the success of some of the above-mentioned applications and, thus, strategies for increasing the

number of switching cycles are needed.

Recently, local annealing methods have been investigated for improving or restoring the degraded performance of logic

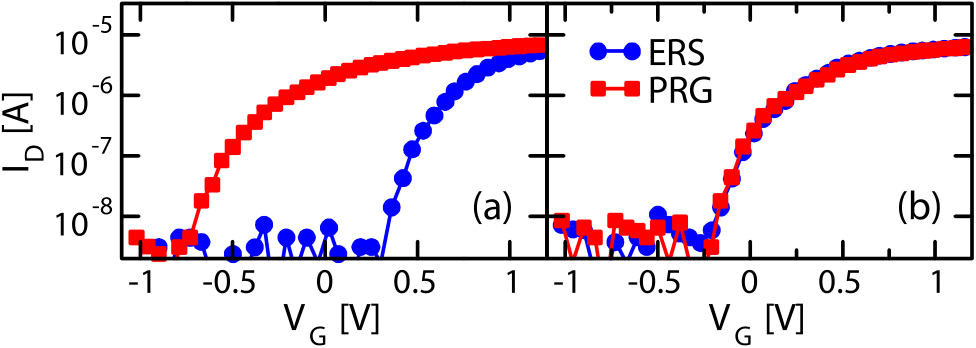
and memory devices. They rely on damage healing by the

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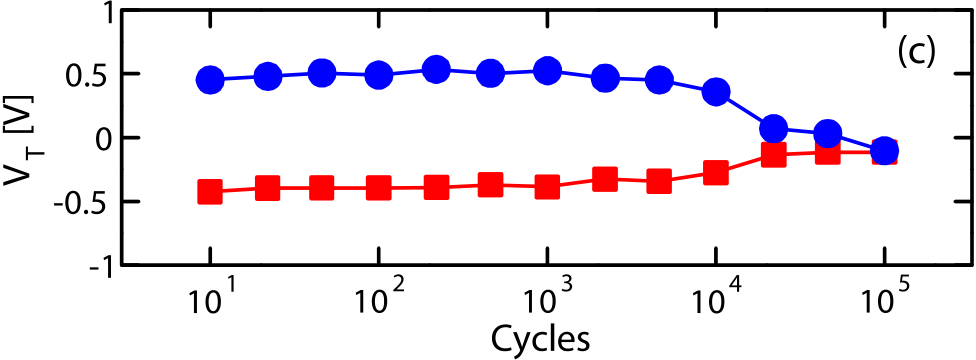


Fig. 1. Effect of the bipolar cycling with PRG: (V P = 3.2 V, 1 *µ*s), and ERS: (VN = −4.5 V, 1 *µ*s). ID-V G curves for the two states after (a) 102cycles, and (b) 105cycles. (c) V T evolution with cycling. The curves are measured at drain voltage V D = 100 mV by a fast V G sweep, which limits the lower resolution to 10 nA. V T is extracted at constant drain current ID = 0.1 *µ*A·W/L.

localized heat generation, e.g. induced by the current flow through a double-ended word-line in NAND flash mem-ory [15] and gate-all-around MOSFETs [16], the *p*−*n* junction forward current [17], the die-stacked heaters [18], [19] and monolithically integrated micro-heaters [20].

In this letter, we explore the impact of self-heating on the post-cycling functionality and endurance of scaled FeFETs. By locally inducing Joule heating, which in our experi-ments is generated upon intentionally forward−biasing the drain (source)−body junction, a full recovery of the FeFET switching and data retention after the cycling endurance failure is reported. Finally, the adoption of this method for enhancing the device endurance is discussed.

II. EXPERIMENTAL RESULTS

Experiments were performed on FeFETs fabricated using the 28 nm high-k metal gate process flow in a gate-first approach, as described in [21]. The devices are characterized by a 1.2 nm thick SiON interface layer and a 10 nm thick Si:HfO2 layer. The channel length (*L)* and width (*W)* of the transistor are 30 nm and 80 nm, respectively.

To set the FeFET into low (high) threshold voltage (*VT )* state, a sufficiently large positive *VP* (negative *VN)* gate pulse

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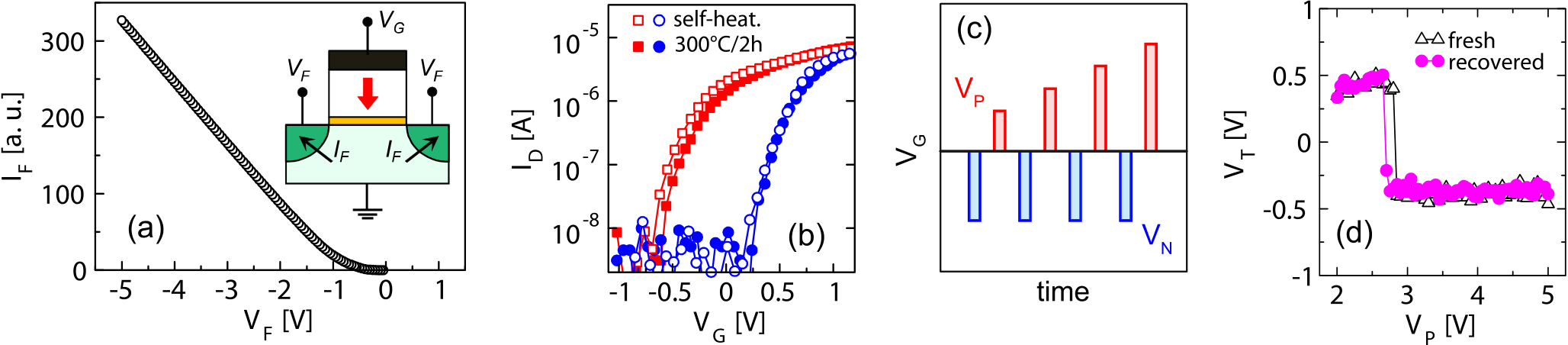


Fig. 2. (a) Forward-bias current IF through drain-body p-n junction, measured by sweeping the drain voltage V F; (b) ID-VG curves of a recovered device for two types of thermal treatment: self-heating under VF pulses and baking in the oven; (c) pulsing scheme for investigating the switching from low- to high-V T state. After each pulse, the corresponding ID-VG is collected; (d) Switching of the fresh and recovered device shown as V T vs. V P, obtained with the waveform shown in (c).

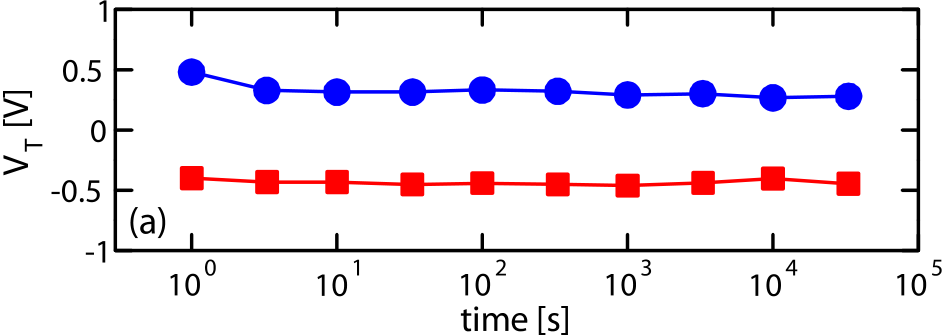
has to be applied. In this way, a program, PRG (erase, ERS) transition is induced.

and their evolution with the increasing number of endurance Fig. 1 shows the so obtained PRG and ERS *ID* −*VG* curves

cycles. The memory window and the *VT* values relative to the two logic states remain almost constant up to 104cycles. However, further cycling rapidly leads to performance degra-dation and to the complete collapse of the memory window after 105cycles (endurance failure, Fig. 1b).

Interestingly, by forward biasing the drain-body and source-body junction and performing a DC sweep at room tem-perature as indicated in Fig. 2a, such a post-cycled and nonfunctional FeFET fully regains the switching property and its memory window. The same effect is achieved in the pulsed regime as well, where *VF* pulses are simultaneously applied at source and drain, while keeping the bulk grounded. For instance, (−3 V, 1 s), and (−4 V, 100 ms) were found to be suited combinations of *VF* amplitude and duration, where the latter pulse setting will be used in the following discussion. the device of Fig. 1 after the pulsed treatment. The recovery Fig. 2b shows the restored PRG and ERS *ID* − *VG* curves of effect is attributable to the local Joule heating generated by the large forward current in the *p*−*n* junction, which heals out the damage at the SiON interface induced by cycling. A similar healing phenomenon has been previously reported for recover-ing the hot-carrier injection induced damage in short channel logic devices [17]. It should be mentioned that the recovery after cycling can be alternatively achieved just by externally annealing the device at elevated temperatures (e.g. by baking in the oven at 300°C for 2 hours, as shown for comparison in Fig. 2b). Even though this is the first experimental evidence for the recovery in FeFETs through an external thermal treatment, such an off-chip technique has a very limited applicability. On the other hand, the recovery could not be achieved by applying a write pulse (ERS or PRG) of an excessively large amplitude and/or duration, as has been reported for some sorts of resistive switching devices [22]. This would, namely, lead to the irreversible hard breakdown of the gate-stack.

Although the recovered device displays a proper memory window, it might be affected by an undesired shift of the PRG and ERS *VT* levels and/or a significant change of the switching response. To verify this, we have performed the analysis of the switching voltage of the pre-cycled and of the recovered device by using the gate waveform shown in Fig. 2c. As can



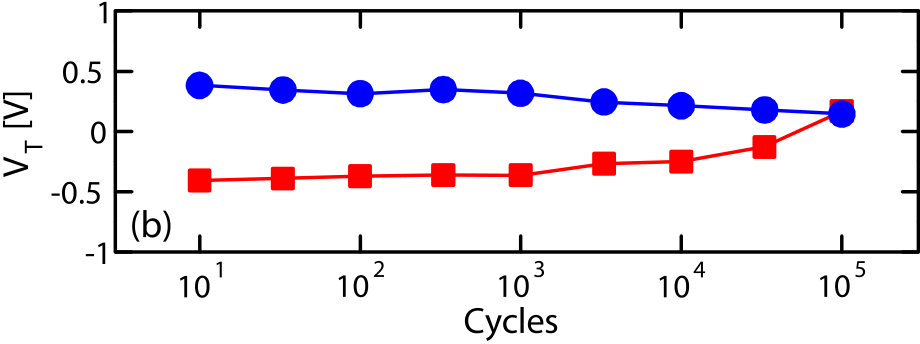


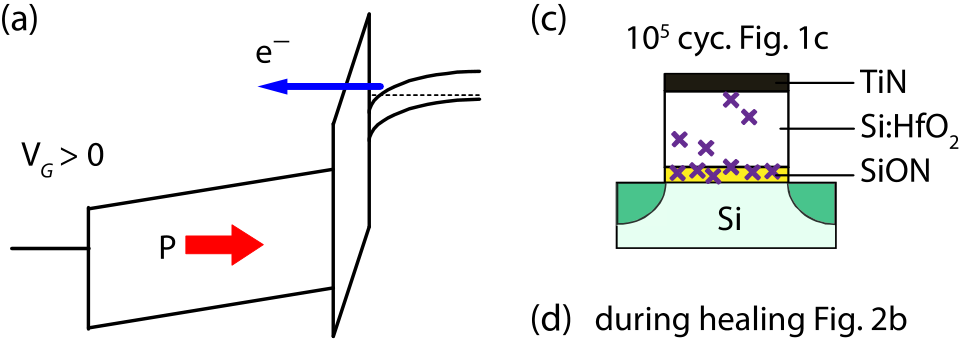
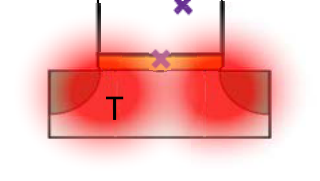
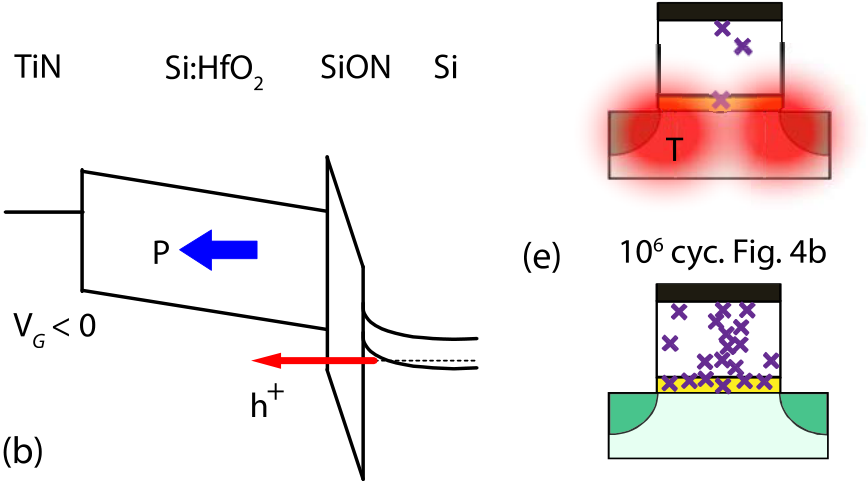
Fig. 3. (a) Retention at room temperature and (b) cycling endurance for the two VT states of the recovered device.

be observed in Fig. 2d, the switching voltage, defined as the gate pulse *VP* for which an abrupt transition from high- to low-*VT* state occurs [21], is almost unchanged and differs by only 100 mV. Note that this value is within the cycle-to-cycle statistical dispersion range, which is normally displayed by these devices [8], [21]. In addition, both PRG and ERS *VT* levels are preserved after the recovery.

To gain more insight into the performance of the recovered device, we performed data retention and cycling endurance experiments. Fig. 3a shows that the FeFET exhibits a very stable retention of the two logic states, similar to the one of the fresh device [23]. The endurance experiment of Fig. 3b shows that the recovered FeFET can still withstand between 104and 105switching cycles prior to the failure. However, in contrast to the fresh device, the degradation sets in for both 100 ms) is not the optimal healing condition and further tuning states already after 103cycles. This might imply that (−4 V, of *VF* parameters is needed.

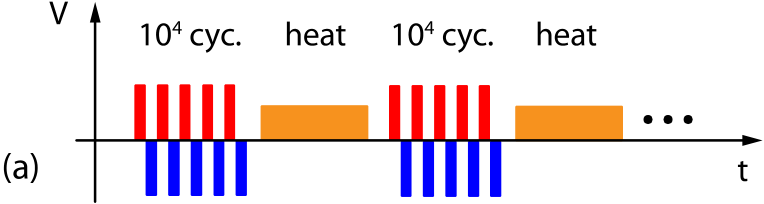
The beneficial effect of the local heating could be exploited to extend the FeFET endurance. A conceivable approach in this regard might be to periodically apply self-heating pulses before a significant degradation sets in, for instance, after a limited number of switching cycles that are not capable of causing the endurance failure (e.g. *N* ≤ 104*)*. Fig. 4b shows

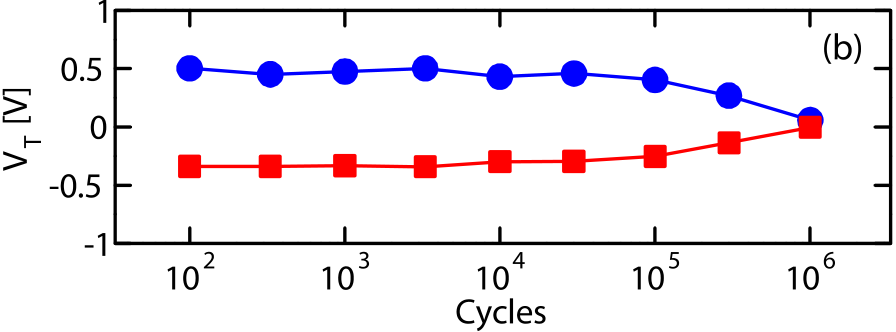
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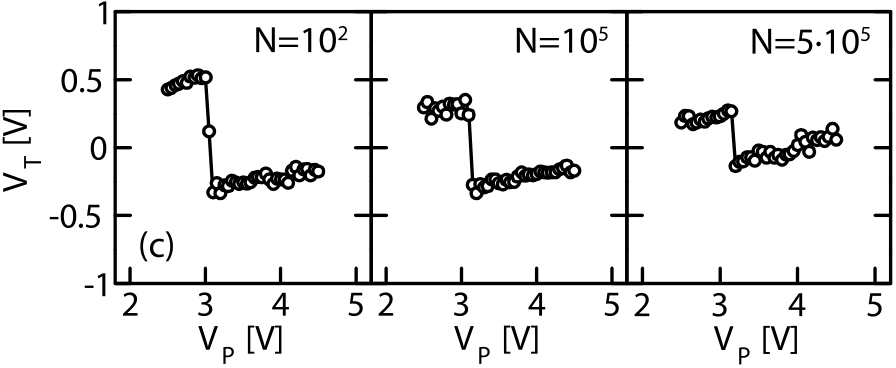


Fig. 4. (a) Pulsing scheme for extending the cycling endurance. A self-heating VF pulse at drain and source terminal is interposed between blocks of 104switching cycles. (b) V T evolution with the cycling scheme in (a); (c) switching behavior after 102, 105and 5 · 105bipolar cycles.

the results of one such experiment, where the *VF* pulses are interposed between blocks of 104bipolar cycles, as depicted schematically in Fig. 4a. The endurance indeed improves and extends for more than a factor of 10 with respect to the result in Fig. 1. Moreover, Fig. 4c shows that the proper and abrupt switching could be detected even after 105cycles as well as after 5 · 105cycles, though with a smaller memory window. However, although the results clearly confirm the bene-fit of adopting the self-heating pulses, this approach can-not be used to indefinitely extend the cycling endurance in FeFETs. Indeed, the memory window collapses before reaching 106cycles, after which the device cannot be recov-ered anymore. This might be explained by assuming that the rate of defect generation under 104PRG/ERS cycles is larger than the healing rate upon a self-heating pulse, which inevitably induces degradation. In fact, the positive and the negative switching pulses approximately correspond to the energy band diagrams of the gate stack depicted in Fig. 5a and 5b, respectively. Owing to the large difference in dielectric constant between HfO2 and SiON, a large portion of the applied *VG* drops across the thin SiON layer. While this favors a significant tunneling of electrons during PRG (Fig. 5a) and holes during ERS (Fig. 5b), the high interfacial field stress induces the generation of defects and the consequent rapid degradation of SiON (Fig. 5c) [14]. Since the created defects act as traps for the injected carriers, the charge trapping drastically increases at this point. The so trapped charge counteracts or even impedes the ferroelectric switching, which causes the collapse of the memory window after 105cycles without healing pulses (Fig. 5c). Nevertheless, this failure is recoverable with *VF* pulses (Fig. 5d), since the defects are located in the proximity of the generated heat. How-ever, further cycling (*N >* 105*)* induces the generation and

Fig. 5. Energy band diagrams of the gate stack during (a) PRG and (b) ERS operation. Only the predominant carrier injection flows are illustrated; additional tunneling paths exist as well. (c) – (e) Schematic illustration of the generation and healing of defects upon cycling and self-heating, respectively. Scenarios for (c) – (d) the recoverable and (e) the permanent breakdown.

redistribution of defects deeper in the HfO2 bulk [24], which cannot be easily healed out. This might cause the formation of defect percolation paths (Fig. 5e), which eventually leads to the hard breakdown [24].

Nevertheless, the results shown here might open up a new path for using the local annealing to boost the endurance. To achieve excellent cycling doses (e.g. the ones shown by Sakai *et al.* for perovskite based FeFETs [25]), further optimization and/or adoption of alternative heating methods might be taken into consideration. For instance, the heating through double-ended word-lines [15] or monolithically inte-grated micro-heaters [20] could be a possible option. Special attention should be given to the device geometry as well, which greatly influences the heat transfer [26]. Finally, these thermal approaches could possibly complement other, already proposed strategies for endurance enhancement [27].

III. CONCLUSION

We have explored the impact of the local heating on the performance of a cycled FeFET device. Joule heating, which is intentionally induced by forward-biasing the drain (source)-bulk *p-n* junctions, almost completely restores the FeFET functionality after the endurance failure. Moreover, external annealing (e.g. baking in the oven) leads to the same outcome. The recovered device preserves the switching behavior, i.e. switching voltage and abruptness of the switching transitions, threshold levels for the two states, and data retention. A puls-ing scheme for extending the endurance has been proposed, which indeed shows the improvement of more than a factor of 10. Further optimization and adopting of alternative heating methods might lead to more significant improvements.

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