

Ferroelectric deep trench capacitors based on Al:HfO2 for 3D nonvolatile memory Applications

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***Abstract* —Aiming for future nonvolatile memory applications**   
**the fabrication and electrical characterization of 3-dimensional**

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| **trench capacitors based on ferroelectric HfO2 is reported. It will** | **Resist+HM** | **RIE etch** |
| **be shown that the ferroelectric properties of Al-doped HfO2** |
| **ultrathin films are preserved when integrated into 3-dimensional** |
| **geometries. The Al:HfO2 thin films were deposited by ALD and** |
| **electrical data were collected on trench capacitor arrays with a** |

**trench count up to 100k. Stable ferroelectric switching behavior**

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| **was observed for all trench arrays fabricated and only minimal** | **TiN BE+FE-HfO2** | **TiN TE** |
| **remanent polarization loss with increasing 3-dimensional area** |

**gain was observed. In addition these arrays were found to**   
**withstand 2\*109 endurance cycles at saturated hysteresis loops.**   
**With these report the 3D capability of ferroelectric HfO2 is**   
**confirmed and for the first time a feasible solution for the vertical**   
**integration of ferroelectric 1T/1C as well as 1T memories is**

|  |  |  |
| --- | --- | --- |
| **presented.** | **Resist+HM** | **Litho 2** |

***Index Terms*—ferroelectric, hafnium oxide, 3D, trench,**   
**nonvolatile memory, FRAM.**

I.INTRODUCTION   
 Among the various emerging memory technologies the long term contender ferroelectric random access memory

**SC1 etch**  **Mask removal**

**3D FE-HfO2**

|  |  |  |  |  |  |  |  |  |  |  |  |
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| (FRAM) is still a promising candidate for future ultralow | | | | | **1.6µm** | **Pr=152µC/cm2** | | | | | 300   (projected area A\*B) **2] P [µC/cm**  150  0  -150  -300 |
| power | nonvolatile | memory | application. | However, the |
| conventionally implemented ferroelectric materials like lead | | | | |
| zirconium titanate (PZT) or strontium bismuth tantalate (SBT) | | | | |
| have revealed several drawbacks in terms of CMOS | | | | |
| compatibility, scalability, and process control. [1] Hence the | | | | |
| material choice for 1T and 1T/1C ferroelectric memory | | | | |
| -4 | -2 | 0 | 2 | 4 | |
| solutions is crucial and poses a major threat to its continues | | | | |
| **E-Field [MV/cm]** | | | | | |
| ability to compete. Especially the large physical thickness of | | | | |

the perovskite ferroelectrics and the lack of feasible thin film technologies has restricted the capacitor-based FRAM architecture to planar capacitor geometries and thereby to the 130 nm CMOS node. According to these limitations, the current storage densities of commercial FRAM products stagnates at 128 MB/cm2 [2]. 20 year ago and at a similar storage density, dynamic random access memory (DRAM) technology struggled with a similar problem eventually leading to the introduction of area enhanced trench and stack capacitors. From this point on scaling continued to current storage densities of above 1 GB/cm2 [3]. In order to establish a similar pathway for future FRAM the implementation of 3-dimensional ferroelectric capacitors is essential.

With the discovery of ferroelectricity in doped HfO2 ultrathin films new capabilities are at hand to overcome the

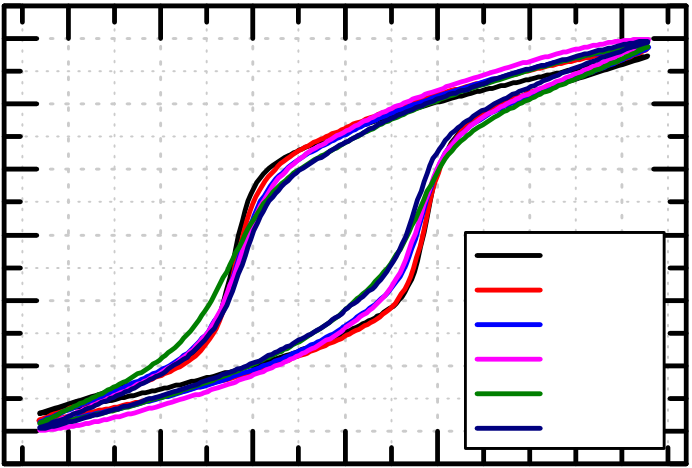
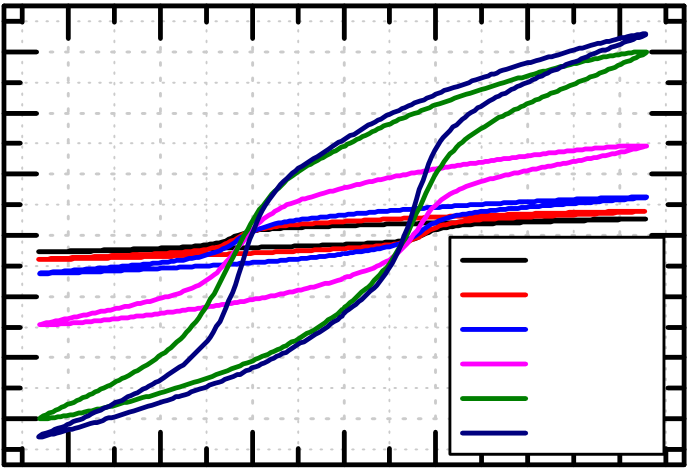
***Fig. 1*** *Process flow scheme for the fabricated ferroelectric deep trench capacitors with high aspect ratio of 13:1 and the accordingly measured hysteresis loop of a 3D deep trench capacitor*

aforementioned integration issues ([4] and therein). As a gate stack material in HKMG and as a capacitor dielectric in DRAM storage nodes HfO2 has proven its CMOS-compatibility and mature ALD processing technology. Leveraging on this assets we will show for the first time that ferroelectric HfO2 maintains its ferroelectric properties when integrated in 3-dimensional structures opening up a perspective for capacitor-based as well as new 1T FRAM cell concepts.

II.EXPERIMENT

To proof the ALD- and 3D-deposition capability of

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **2]** | (pojected area A\*B) | 300 | **a)** | **E-Field [MV/cm]** | | | | | | **2]** | | 30 | **b)** | | **E-Field [MV/cm]** | | | | |
| -3 | -2 | -1 | 0 | 1 | 2 | 3 |
| -3 | -2 | -1 | 0 | 1 | 2 | 3 |
| **polarization [µC/cm** | planar | | | | | | | **polarization [µC/cm** | | 20 | planar | | | | | | |
| 200 |
| 100 | 10 |
| 0 | 0 |
| -100 | 1k array | | | | | | | -10 | 1k array | | | | | | |
| 3k array | | | | | | | 3k array | | | | | | |
| -200 | -20 | 10k array | | | | | | |
| 10k array | | | | | | |
| -300 | 30k array | | | | | | | 30k array | | | | | | |
| -30 |
| 100k trench | | | | | | | 100k array | | | | | | |
| **gain factor** | 12 | 1k 10k 100k  **trench count** | | | | | | | **norm to** | **planar Pr [%]** |  | | | | | | |
| 100 |
| 8 |
| 4 | 80 |
| 60 |
| 0 |
| 1k | | 10k  **trench count** | | | 100k | |

***Fig. 1***   
***a)*** *P-E characteristics for different trench arrays related to the number of trenches for the projected planar area and the calculated gain factor in accordance to the increase of the capacitor area*

***b)*** *Normalized, to the real capacitor area, hysteresis loops of the measured trench arrays and the relative polarization loss in relation to the planar capacitor value*

aluminum doped, ferroelectric HfO2, deep trench metal-insulator-metal capacitors were fabricated on 300 mm silicon

maintain the same size of their planar projection. The 100k trench array has a slightly bigger planar size due to the number

substrates. of trenches. Only the count of trenches may increase from

Therefore, at first a SiO2 hardmask and a photoresist were deposited, followed by an eBeam lithography step to define the trench capacitor arrays. Afterwards, the holes for the trench capacitors are etched into the substrate by a reactive ion etching process (RIE). Subsequently, the resist and hardmask are removed and an approximately 10 nm TiN bottom electrode was deposited by thermal atomic layer deposition (ALD) at 450 °C from TiCl4 and NH3. Furthermore, the 12 nm Al:HfO2 ferroelectric layer was deposited through an ALD process at 300 °C substrate temperature. The control of the Al doping in the HfO2-layer was adjusted by the ratio between tetrakisethylmethylaminohafnium (TEMAHf) / ozon (O3) and trimethylaluminum (TMA) / ozon (O3) ALD cycles. A 35 nm thick TiN top electrode was deposited by pulsed chemical vapor deposition at 400 °C. A second lithographic exposure was necessary, for the final contact patterning. After this final structuring process the exposed TiN was removed selectively with a SC1 wet etch. Lastly, the mask residuals were removed. As a result, electrically accessible deep trench capacitor arrays were fabricated with trench counts ranging from 1k to 100k and with an aspect ratio of 13:1.

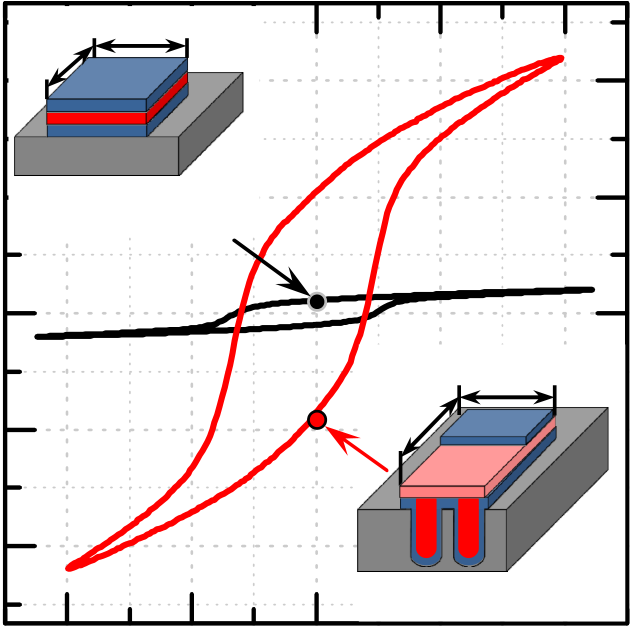
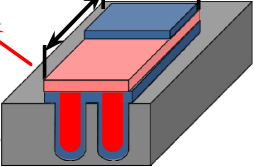
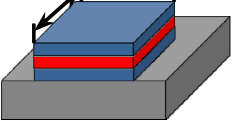
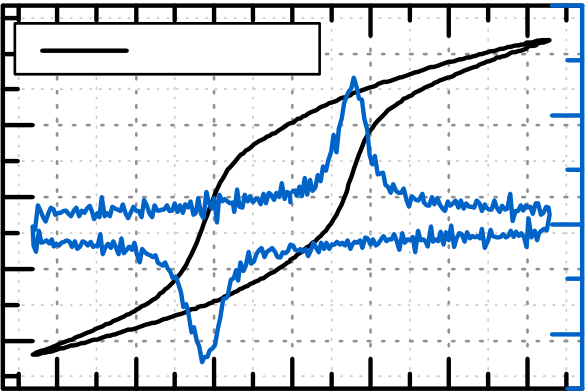
The P-E Hysteresis and endurance measurement were conducted with an aixACCT TF Analyzer 3000 measurement setup. The C-V Hysteresis was recorded with an Agilent E4980A LCR-Meter.

III.RESULTS AND DISCUSSION

The fabricated test chip contains capacitors with an increasing count of trenches. All capacitors up to 30k trenches

capacitor to capacitor device. With this test structure it is possible to investigate the relation between the increase of polarization and the increase of capacitor area. The area gain factor compared to the planar projected area depends on the number of trench holes, the diameter of a single trench and the determined depth of the trenches which was extracted from the STEM analysis. As basis for the area calculation of the regularly rectangular shaped trench holes an elliptic model was used. It is needed to take the rounded corners of the holes into account. Even if this approach is the most conservative it was applied to avoid an overestimation of the trench area. The measured planar capacitor served as reference value for the measured polarization of the trench arrays.

In Fig. 2 a) the polarization for different trench arrays with respect to the projected planar area as well as the calculated area gain factor for the measured devices is illustrated. In contrast to this, Fig. 2 b) illustrates the area normalized polarization hysteresis for the different trench arrays and compares them to the planar area hysteresis loop. Further it summarizes the loss of remanent polarization with increasing number of trenches. For the planar capacitor, without trenches, a remanent polarization of 15 µC/cm2 was measured. The trench array with 100k trenches has a calculated area gain factor of 11.12 and the measured remanent polarization based on the projected planar area of this array is 152 µC/cm2 (Fig. 3). This translates to an actual remanent polarization of 13.6 µC/cm2. This remanent polarization value of the 100k array suggests that all parts, including the trench side walls, contribute to the overall polarization gain. The low remanent



**E-Field [MV/cm]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 300 | | **A** | **B** | | | | | -3 | | | | | -2 | -1 | 0 | 1 | 2 | 3 | | |
| **2]**� | �(pojected area A\*B)� | 300 | | | 100k array | | | current [a.u.] | | | | |
| **polarization [µC/cm** |
| **2]** | | | | | | | | 150 | | |
| **polarization [µC/cm**  (projected area A\*B) | 150 | **2D** | | | | **A** | **B** |
| **Pr=15 µC/cm2** | | | | 0 | | |
| 0 | -150 | | |
| -300 | | |
| -150 | ε**r** | | 50 |  | | | | | | | | | |
| -300 | | **3D** | | | | | | 45 |
| **Pr=152 µC/cm2** | | | | | | | | 40 |
| -4 | | | | -2 | 0 | 2 | 4 |
| -3 | | | | | -2 | -1 0 1 2  **E-Field [MV/cm]** | | | | 3 | | |
| **E-Field [MV/cm]**  ***Fig.3*** *Comparison of P-E hysteresis between a planar capacitor and 100k trench capacitor with same planar area (projected area). The* | | | | | | | |
| ***Fig.4*** *P-E hysteresis loop of the densest trench array with the* | | | | | | | | | | | | |
| *highest* | *remanent* | | | *projected* | | | *planar* | *polarization* | | | *and* | *the* |

*calculated area gain, due to the additional trench surface, is electrically reflected in the P-E hysteresis*

polarization loss of about 11% compared to the planar value may be attributed to the conservative approximation of the 3-dimensional surface area. Nevertheless, an intrinsic loss of ferroelectric polarization due to Al-dopant fluctuations and therewith ferroelectric phase stability fluctuations with increasing trench depth cannot be excluded. These issues, however, are likely to be fixable with further ALD processing

*corresponding C-V curve.*

frequency of 10 kHz was applied to stress the devices and emulate continuous read/write operations. In between of these pulse trains a hysteresis measurement was performed. In Fig. 5 the summarized results of these endurance measurements are illustrated for the 100k trench array. The highest endurance for a saturated and therewith stable hysteresis [7] was measured with 2\*109 cycles at a field of 2.5 MV/cm. Lowering the stress

iterations. signal amplitude to 2 MV/cm, however, already reveals a

Further measurements were carried out on the 100k array to determine the ferroelectric behavior of the densest array. The measurement results are illustrated in Fig. 4. The collected data are a clear evidence for a real ferroelectric behavior of the deep trench capacitors. A characteristic P-E hysteresis loop as well as the corresponding current peaks clearly distinguishable from

subloop behavior and a stronger impact of polarization fatigue is observed. Increasing the stress amplitude above 2.5 MV/cm lowers the time to dielectric breakdown and therewith limits the possible endurance cycles. This results show that in spite of the excellent 3D-capability and thickness scaling properties further electrode and material optimization will be required to

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| leakage currents could be measured with a 1 kHz triangular | meet | the | endurance | requirements | of | current | FRAM |
| voltage sweep. The dual sweep C-V measurement at 30 kHz | applications. | | IV.CONCLUSION | |
| and 50 mV amplitude further showed the characteristic |
| capacitance maxima at bias voltages corresponding to the |

coercive field strength. From the calculated permittivity value of about 38 it can be concluded that the Al:HfO2 layer is crystalline [5], which is essential to obtain ferroelectric behavior in HfO2 thin films.

State of the art FRAM metal-ferroelectric-metal capacitors have been engineered to be highly durable and electrically stable. These conventional ferroelectrics withstand 1012 endurance cycles, [6] whereas for comparison, common Flash memory endurance ranges between 103 and 106 cycles. However, due to the destructive read out operation of capacitor based FRAM these high endurance values are required and can be considered essential for all application scenarios. In this context the endurance behavior of the fabricated capacitors

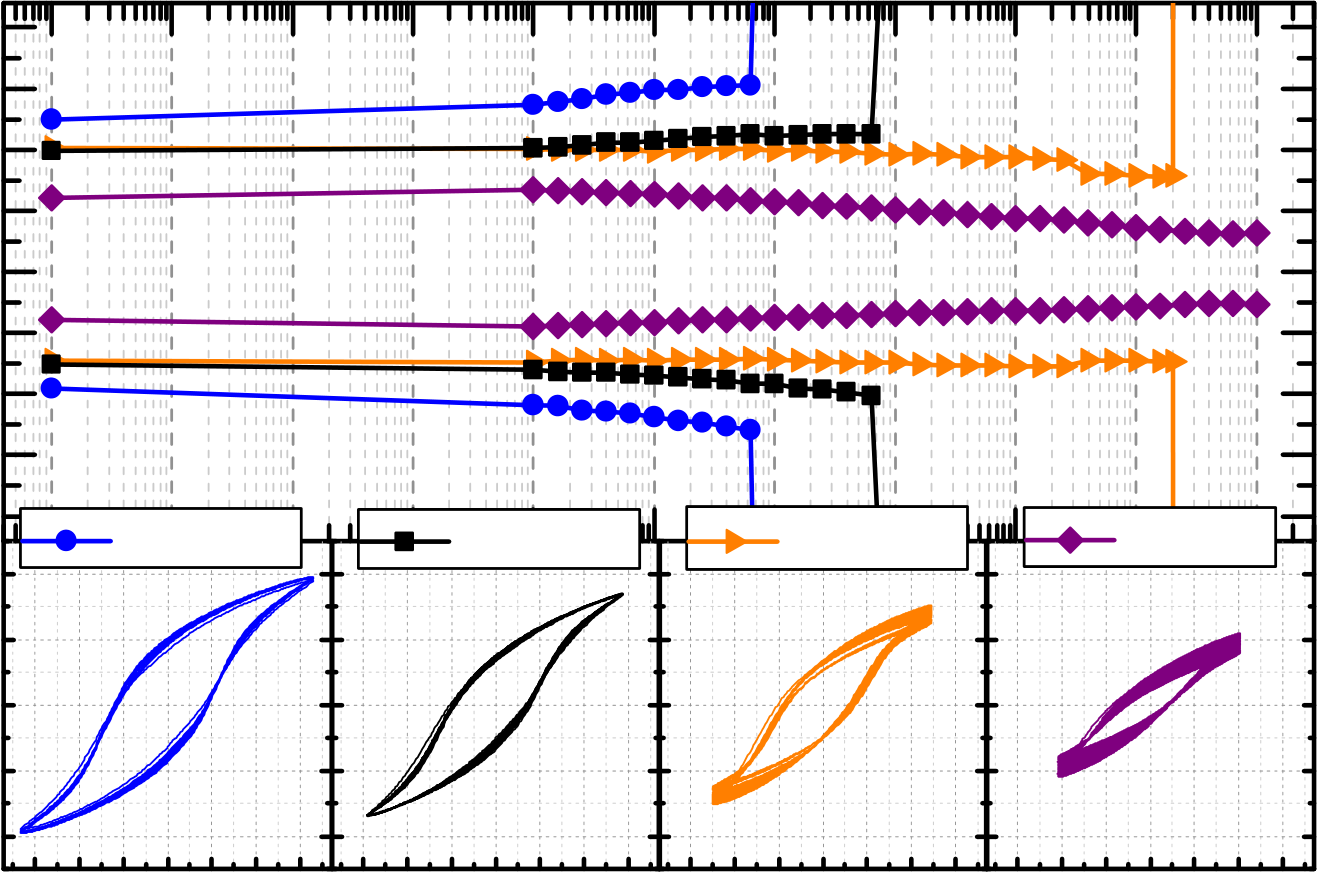
In this article we demonstrated the first fully functional, ultrathin film, ferroelectric, deep trench capacitor. For 100k trench arrays a planar area projected remanent polarization of 152 µC/cm2 was achieved, revealing minimal remanent polarization loss due to vertical integration. Endurance characteristic of these 3-dimenisonal capacitors further showed that 2\*109 switching cycles within a saturated, stable hysteresis loop can be performed without fatigue or dielectric breakdown of the ferroelectric HfO2.

The now possible introduction of CMOS-compatible ferroelectric trench and stack capacitors provides a pathway to 1T/1C FRAM lateral area scaling and therewith higher memory densities. It should be noted that in terms of MIM stack

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| were investigated. Therefore, the 100k arrays were charged | configuration, | material | choice, | and | geometric | trench |

with different voltages. All tested structures have been previously conditioned to guarantee the same starting condition for all samples. A rectangular pulse train with a cycling

dimensions this demonstration of a nonvolatile memory operation closely resembles the volatile eDRAM approach



**cycles [n]**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **2]** | (pojected area A\*B) | 200 | 0  10 | 1  10 | 2 10 | 3  10 | 10 | 4 | 5 10 | 6  10 | 10 | 7 | 10 | 8 | 9  10 | 10 | 10 |
| **remanent polarization [µC/cm** |
| 150 |
| 100 |
| 50 |
| 0 |
| -50 |
| -100 |
| (pojected area A\*B) | 3.3 MV/cm | | | 2.9 MV/cm | | | | 2.5 MV/cm | | | 2 MV/cm | | | | |
| -150 |
| -200 |
| **2]** |
| 300 |
| **polarization [µC/cm** |
| 150 | -3 -2 -1 0 1 2 3 | | | -3 -2 -1 0 1 2 3 | | | | -3 -2 -1 0 1 2 3 | | | -3 -2 -1 0 1 2 3 | | | | |
| 0 |
| -150 |
| -300 |
| **E-Field [MV/cm]** | | | | | | |

***Fig.5*** *Endurance characteristics of the 100k trench array for different stress conditions. Excellent results have been observed for measurements with an amplitude of 3V (2.5 MV/cm) for a saturated and stable window.*

introduced by INTEL in 2013 [8]. This underlines the manufacturability of this NVM approach.

Besides its implications on capacitor based ferroelectric memories this 3D- capability provides a new perspective for 1T ferroelectric memory solutions as well. As an embedded memory in HKMG technology the HfO2-based ferroelectric field effect transistor (1T FRAM) has to be able to adapt to its CMOS environment. In other words, with a transition from gate first to gate last (full replacement gate) to

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ultimately | trigate | transistor | a | conformal | deposition |

technology for the logic as well as for the memory transistor becomes essential. Additionally increasing memory density further will eventually require 3D-architectures and vertical integration comparable to other 1T memory solutions such as 3D vertical NAND. With the feasibility demonstration of 3D-integration presented here, the framework to investigate such new memory solutions is set.

ACKNOWLEDGMENT

K. Biedermann is acknowleged for the STEM micrographs. J. Paul is acknowleged for the RIE etch and the whole eBeam group of our institute for the patterning process.

This work was financially supported within the EFRE fund of the European Community and by the Free State of Saxony (Cool Memory).

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| embedded | DRAM | SoC | technology | featuring | tri-gate |

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