A 28nm HKMG super low power embedded NVM

technology based on ferroelectric FETs

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| ***Abstract*—**We successfully implemented a one-transistor | The | hafnium-based | FeFET | was | embedded | into |

(1T) ferroelectric field effect transistor (FeFET) eNVM into a 28nm gate-first super low power (28SLP) CMOS technology platform using two additional structural masks. The electrical baseline properties remain the same for the FeFET integration and the JTAG-controlled 64 kbit memory shows clearly separated states. High temperature retention up to 250 °C is demonstrated and endurance up to 105 cycles was achieved. The FeFET unique properties make it the best candidate for eNVM solutions in sub-2x technologies for low-cost IoT applications.

**I.**  **INTRODUCTION**

A cost effective, ultra-low-power embedded non-volatile-memory (eNVM) is essential for IoT applications. One candidate among the emerging memory concepts is the ferroelectric field effect transistor (FeFET). The discovery of ferroelectricity in silicon doped hafnium oxide (Si:HfO2) in 2011 [1] enabled the transfer of ferroelectric based devices into mainstream CMOS platforms due to its scalability and CMOS compatibility [2,3]. Those single device results established the foundation when going from development to mass production. For the first time we demonstrate FeFET eNVM functionality on larger memory arrays embedded into a foundry standard 28nm SLP HKMG CMOS flow. We have developed a non-disruptive eNVM process and show JTAG-controlled array results, together with initial retention and endurance data.

**II.RESULTS AND DISCUSSION**

*A. Experimental Details*

The test vehicle (Fig. 1) comprises several 64 kbit FeFET arrays with NOR and AND architectures and different transistor dimensions ranging from 30 nm x 80 nm to 500 nm x 500 nm. Each 1T memory cell can be accessed individually for write operations and parametric measurements via an integrated decoder circuitry. The logic state of each device is detected by an on-chip current sense amplifier. The chip features a JTAG interface for addressing and configuration of the step sequence. Since the chip mainly acts as a multiplexer, neither on-chip charge pumps nor clock generators are required. Voltage pulses for writing and readout are generated externally.

GLOBALFOUNDRIES high-volume gate-first 28nm HKMG super low power platform (28SLP, Table I). The simultaneous integration of CMOS devices together with the FeFET on the same chip is demonstrated (Fig. 2). The FeFET gate stack (material, thickness, etc.) can be optimized independently from the baseline 28nm device integration. An arbitrarily mixed placement of CMOS and FeFET devices in the same circuit is possible with platform logic design rules.

*B.Platform Compatibility*

The fully CMOS compatible embedded FeFET integration scheme requires two additional structural DUV-masks. The electrical device parameters of the 28SLP platform are not shifted by the FeFET integration as shown exemplarily for the logic device performance in Fig. 3. The additional process steps do not increase the defectivity level as was demonstrated on a matured high-volume product (not comprising an actual FeFET area) where the implemented FeFET module did not affect the D0-limited yield. The current integration scheme enables a direct transfer of the FeFET module into more advanced technologies, like the 22FDXTM platform.

*C.Single Device FeFET Functionality*

Fig. 4 shows the polarization hysteresis measured on 10,000 µm2 TiN-Si:HfO2-TiN (MFM) capacitors as a reference. ID-VG-characteristics of a single device fabricated using the ‘Generation 0’ embedded FeFET process is shown in Fig. 5a for both “low-VT” and “high-VT” states with a memory window of MW=1 V. The difference in VT from low-VT and high-VT state results in a drain current ratio > 100. As

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| compared to classical FRAM, the 1T architecture allows for |

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| non-destructive reads and a memory operation comparable to |

that of eFLASH cells. The domain-driven ferroelectric switching behavior [4] for a 500x30 nm2 device is shown in Fig. 5b and observed to be extremely abrupt, indicating high stability against disturbs. For positive gate pulses the VT shifts to lower values at around VG=3 V, whereas for negative gate pulses around 4 V the VT shifts to higher values. Pulse lengths at the moment are still in 1-10 µs range, gated by the external pulse generation. Shorter pulse lengths are beneficial for

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| endurance and fast read-out after writing, as it shifts the |

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| balance between two contradictory mechanisms, trapping and |

polarization, in a favorable direction [5].

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*D.64 kbit Macro*  *F.Benchmarking*

In order to verify the effective addressability of arrays within the chip, the functionality of the JTAG interface was tested across the wafer (Fig. 6). A full functionality could be observed for a wide range of addressing voltages.

The distribution of high-VT and low-VT states was investigated considering single devices connected in a 64 kbit AND array. To this purpose a stripe pattern was programmed which consisted in erasing the complete array by block erase and writing the low-VT state in cells along every second word-line (WL). As shown in Fig. 7 a clear distinction between the two states has been achieved. The two distributions are visualized in the histogram of Fig. 8. The reverse programmed pattern is also shown with a very similar distribution. Fig. 9 shows the fully normal distributed states with a clear separation of their mean values by a factor of ~10 and without any remaining superposition. Parasitic charge trapping effects

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| (esp. | for | the | low-VT | distribution) | and | non-uniform |

ferroelectric film properties among cells [4] are being further optimized. The cross-wafer signature of overlapping cells in Fig. 10 is related to variations of the ferroelectric film properties (thickness and doping) caused by the ALD cross flow profile [3]. A correlation of the number of overlapping cells to the drain current ratio is visible in Fig. 11. Single cell access was demonstrated by successfully writing a low-VT checkerboard pattern after block erase (Fig. 12).

It should be noted that the data presented here are showing the natural/intrinsic low-VT and high-VT distribution after single pulse programming. More advanced programming

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| schemes such as incremental step pulse programming (ISPP) |

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| or verify algorithms can be used for further optimization. |

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| Alongside error-correction code (ECC) and further material |

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| optimization will stabilize memory operation towards Mbit |

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| arrays. |

*E.Endurance and Retention*

Performance of the array was explored by means of endurance and retention tests. Fig. 13a shows the distributions of the two states after the array has been subjected to 100 and 104 bipolar cycles. Evolution of the endurance up to 106 is shown in Fig. 13b indicating a gradually reduction of the ferroelectric memory window starting at 105 cycles. The low-VT state is mainly affected by the degradation which has been investigated in previous studies on single devices [6]. This behavior is attributed to the wear-out of the interfacial layer between HfO2 and silicon substrate and the consequent increase of charge injection (Fig. 14). The interfacial layer has not been optimized yet and endurance beyond 105 cycles is expected based on previous publications [7,8].

The data retention was tested at 105 °C for 72 h and at elevated temperatures of 250 °C for 1 min (tester limited to ≤250 °C). The programmed pattern was entirely preserved after the bake time (Fig. 15a) confirming the high thermal stability of the ferroelectric hafnium oxide. The time-dependent retention at 105 °C (Fig. 15b) shows an initial degradation (after 1 min) of the high-VT state whereas the cell state separation is stable afterwards for longer stress-times.

The FeFET, as a one-transistor (1T) based embedded memory implemented in the FEoL, can be directly bench-marked against eFLASH solutions that are currently being developed on HKMG technology platforms. These embedded FLASH technologies have a long history of development and testing that has earned them a large customer acceptance and trust ranging from consumer up to automotive products. However, when comparing the unique physical mechanism controlling the threshold voltage shift in FeFETs to the charge based programming of FLASH technologies the potential of the ‘Generation 1’ FeFET to emerge as a superior technology is clearly revealed (see Table II):

(1) Opposed to the energy inefficient hot carrier injection of eFLASH at high Gate and S/D voltages (only a small portion of the programming current reaches the floating gate) the FeFET is programmed at low gate voltages using the electric field for polarization switching. The energy/bit consumption and array efficiency due to a downsizing of charge pumps and scaling of channel length is accordingly improved. The scalability of the bit-cell is mainly limited by the ~4 V power routing and less by ferroelectric high-k film thickness which has been demonstrated to retain its ferroelectric properties down to 6 nm [9].

(2) Opposed to the charge based storage mechanism of FLASH devices the concept of ferroelectric switching provides radiation hardness and allows for ultra-fast switching in the nanosecond range.

(3) The simplicity of the FeFET device (e.g. no Floating-Gate, no Erase-Gate, no IPD, etc.) and its close resemblance to the HKMG base device greatly facilitates its manufacturing and lowers mask adders significantly.

**III.SUMMARY**

A fully functional 64 kbit FeFET eNVM array embedded into a 28nm HKMG CMOS technology has been fabricated and characterized. The binary cell states of the FeFET are clearly separated and initial retention and endurance data is reported. The FeFET can be seamlessly integrated into a generic *gate-first* HKMG CMOS logic platform, like 22FDXTM and is likely transferable also to *gate-last* and FinFET technologies.

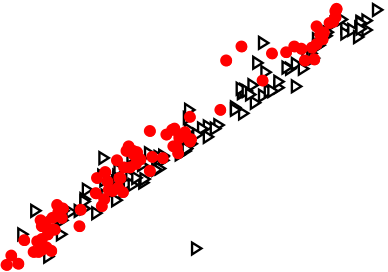
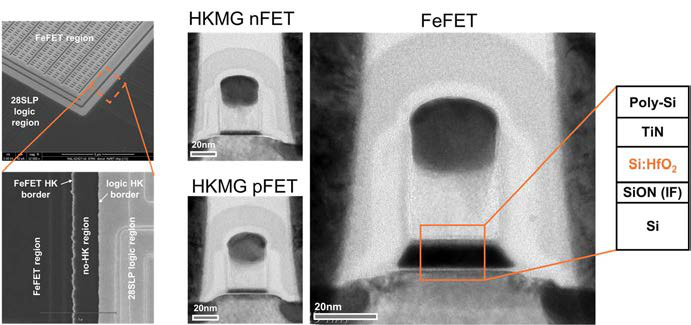
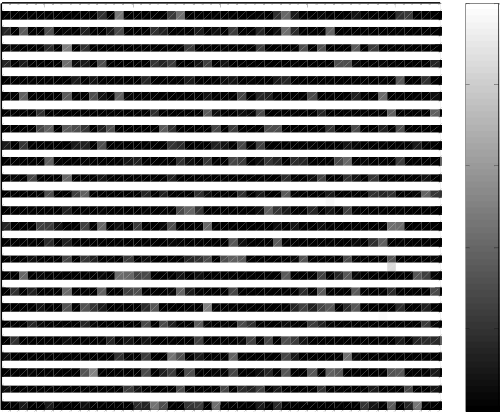
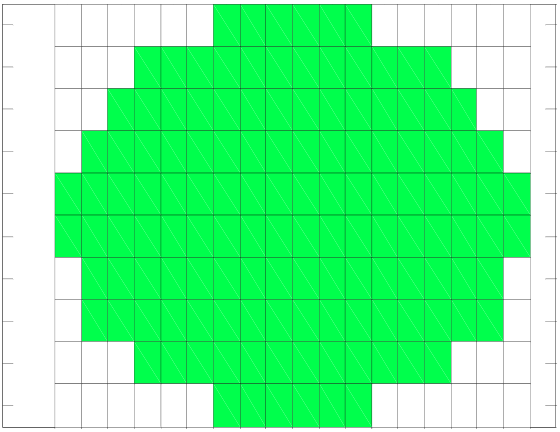
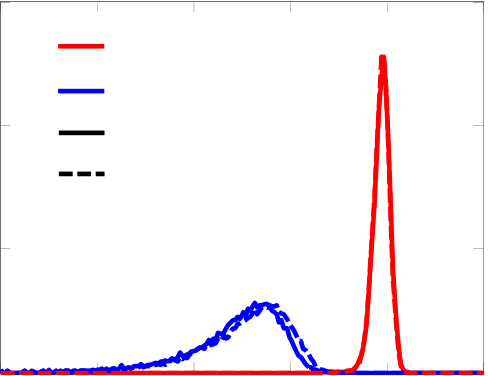
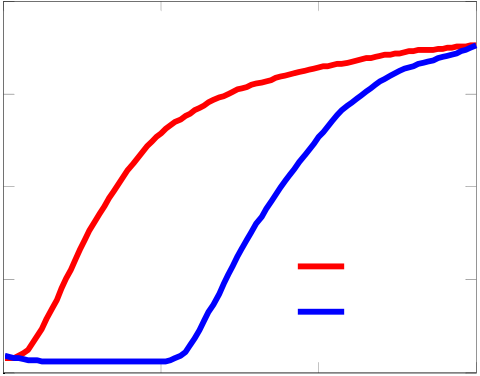
ACKNOWLEDGMENT

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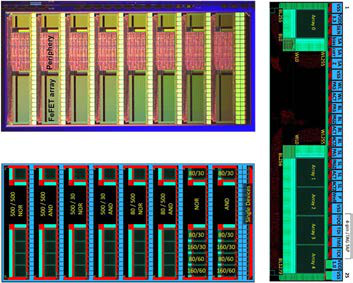


Fig. 1. Die picture (top left) and layout   
(bottom left) showing the 64 kbit array macro with its different test blocks. A detailed view of a 5x64 kbit block is shown to the right.

Fig. 2. (left) SEM top-views of the embedded FeFET macro, TEM crosssections of the HKMG logic transistors (middle) and the embedded FeFET (right) from the same wafer. Inset shows the gate stack details of the FeFET.

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| Table I. The FeFET eNVM extends the 28nm super low power platform offering. | | | | | | | | | 3  10 | | | |  | | --- | | nFET  reference 28SLP  28SLP w/ FeFET | | | | | | 3  10  10  10  10  -1  -2  -3   |  | | --- | | pFET    reference 28SLP  28SLP w/ FeFET |   2  10  1  ID,OFF [nA/μm]   10  0  10  200 400 600 800  **(b)**  ID,ON [μA/μm] | | |
| 2  10 | | |
| ID,OFF [nA/μm] | 1 10  0 10  -1 10 | |
| -2  10 | | |
| -3  10 | | |
| 400 | 600 800  ID,ON [μA/μm] | | 1000 | |
| **(a)** | | |
| Fig. 3. Ion-Ioff performance curves of (a) nFET and (b) pFET logic devices. The embedded 28nm SLP-FeFET flow is matched to the reference 28nm SLP platform performance. | | | | | | | | | | |
| Polarization [µC/cm²] | 40 |  | | | | | | | -4  10 | | | | 0 | VG [V] | 1 | low-VT | 2 | 1  -0.5  -1.5-1  -5 -4 -3 -2 2 3 4 5 0.5  0  V T [V]  (b) V G [V] V G [V] | 1 |
| 30 | 0.5 |
| -6  10 | | | |
| 20 |
| 10 | ID [A] | | -8  10 | | 0 |
| 0 | -0.5 |
| -10 | -10  10 | | | |
| -1 |
| -20 | high-VT |
| -30 | -12  10  -1  (a) | | | | -1.5 |
| -40 |
| -3 | | | -2 | -1 | 0 | 1 | 2 | 3 |

Voltage [V]

Fig. 4. Polarization hysteresis measured on 10,000 µm2 metal-ferroelectric-metal (MFM) capacitor.

Fig. 5. (a) ID-VG characteristics from a FeFET device for the two distinct polarization states (low-VT and high-VT). The switching voltage behavior of this device is shown in (b).

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| 1 | | | | | | | -5 | | | | | | | 0.15 | | | | | | |
| 2 | | | | | | | 170 | | | | | | |
| low-VT | | | | | | |
| -5.1 | | | | | | |
| 3 | | | | | | |
| Normalized counts | 0.1 | high-VT | | | | |
| 4 | | | | | | | 160 | | | | | | |
| normal | | | | |
| Wordline | 150 | -5.2   log10(ID) -5.3 | | | | |
| die Y | 5 | 100% JTAG yield | | | | | 0.05 |
| reverse | | | | |
| 6 |
| 7 | | | | | | |
| 140 | | | | | | |
| 8 | | | | | | |
| -5.4 | | | | | | |
| 9 | | | | | | | 0-9  10 | | -8  10 | -7  10 | -6  10 | -5  10 | -4  10 |
| 130 | | | | | | |
| 10 | | | | | | |
| 130 | | 140 | 150 | 160 | 170 | -5.5 |
| 1 | | 3 | 5 | 7 | 9 | 11 13 15 17 |
| Bitline | | | | | | | Current [A] | | | | | | |
| die X | | | | | | |
| Fig. 6. JTAG yield across the wafer. Full | | | | | | | Fig. 7. Stripe pattern of the drain current ID of | | | | | | | Fig. 8. Distribution of the drain current ID | | | | | | |
| the FeFET device (small portion of the entire | | | | | | |
| functionality was observed all across the wafer. | | | | | | | for the low-VT and high-VT state cells of | | | | | | |
| 64 kbit array shown only) written for alternating | | | | | | |
| the 64 kbit FeFET array. Reverse pattern is | | | | | | |
| word-lines. | | | | | | |
| shown to be matched. | | | | | | |
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| Cumulative distribution | | 0.99999 0.9999  0.999 |  | | | |  | | low-VT | | | 1 | | | | 5000 | | | | | | | 1 | | | 5 | | | | | | | | | | |
| die Y | 2 | | | 4000 | | | | | | n# overlapping cells | die Y | | 2 | 4 | | | | | | | | | | log10(ID,low-VT/ID,high-VT) |
| 3 | | | 3 |
| 0.99 |
| 0.9 | 4 | | | 3000 | | | | | | 4 | 3 | | | | | | | | | |
| 0.5 | 5 | | | 5 | 2 | | | | | | | | | |
| 6 | | | 2000 | | | | | | 6 |
| 0.1 | 7 | | | 7 |
| 1 | | | | | | | | | |
| 0.01 | 8 | | | 8 |
| 1000 | | | | | | 0 | | | | | | | | | |
| 0.001  0.0001  0.00001 | 9 | | | 9 |
| high-VT | | |
| 10 | | | 1 | 3 | 5 |  | 9 11 13 15 17 die X | 0 | | | 10 | | |  | 3 | |  |  | 9 11 13 15 17 | | | | -1 | |
| -10 | | | 0 | | | 10  Current [μA] | | | 20 | | 30 | 7 | 1 | 5 | 7 |
| die X | | | | | | | | | | | | | |
| Fig. 9. Cumulative distribution of the drain | | | | | | | | | | | | Fig. 10. Number of overlapping cells in the | | | | | | | | | | | Fig. 11. Wafer map of single-device FeFET | | | | | | | | | | | | | |
| current ID for the programmed pattern (32 kbit | | | | | | | | | | | | 64 kbit array after pattern writing shown as | | | | | | | | | | | current ratios, log(ID-low-VT / ID-high-VT). Clear | | | | | | | | | | | | | |
| in low-VT and 32 kbit in high-VT state) of the | | | | | | | | | | | | wafer map. Cross-wafer signature is caused by | | | | | | | | | | | separation of the two cell states (low- & high- | | | | | | | | | | | | | |
| 64 kbit array. No error exclusion was done. | | | | | | | | | | | | ALD cross flow profile [3]. | | | | | | | | | | | VT) with ratios >10.000 are demonstrated. | | | | | | | | | | | | | |
| -5 | | | | | | | | | | | | -4  10 | | | |  |  |  |  | | --- | --- | --- | --- | | low-VT  high-VT | | | | | | | | | | | | | | | |
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