1

Ferroelectric HfO2 Memory Transistors with

High-*κ* Interfacial Layer and Write Endurance

Exceeding 1010Cycles

|  |  |
| --- | --- |
| arXiv:2103.08806v1 [physics.app-ph] 16 Mar 2021 | Ava Jiang Tan, Yu-Hung Liao, Li-Chen Wang, Jong-Ho Bae, Chenming Hu,  Sayeef Salahuddin  **Abstract**  We demonstrate ferroelectric (FE) memory transistors on a crystalline silicon channel with en-durance exceeding 1010cycles. The ferroelectric transistors (FeFETs) incorporate a high-*κ* interfacial layer (IL) of thermally grown silicon nitride (SiN*x*) and a thin 4.5 nm layer of Zr-doped FE-HfO2 on a *∼*30 nm SOI channel. The device shows a *∼* 1V memory window in a DC sweep of just *±* 2.5V, and can be programmed and erased with voltage pulses of *VG* = *±* 3V at a pulse width of 250 ns. The device also shows very good retention behavior. These results indicate that appropriate engineering of the IL layer could substantially improve FeFET device performance and reliability.  I. INTRODUCTION  Despite the fact that there has been much rekindled interest in ferroelectrics-based nonvolatile memories due to the discovery of CMOS-compatible doped HfO2 materials [1]–[8], one of the key roadblocks facing the development of FeFETs specifically is endurance. It has been shown, for thicker *>*5-6 nm FE oxides, that bulk charge-trapping and interfacial layer breakdown (due to the large coercive fields associated with ferroelectric HfO2, and therefore, the larger write |

This work was supported in part by the Berkeley Center for Negative Capacitance Transistors, the ASCENT Center, one of the six centers within the DARPA/SRC JUMP initiative and the DARPA FRANC program. The work of A. J. Tan was supported by the National Defense Science and Engineering Graduate Fellowship (NDSEG).

A. J. Tan, Y-H. Liao, L-C. Wang, C. Hu, and S. Salahuddin are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, Berkeley, CA 94720 USA (e-mail: ava@eecs.berkeley.edu).

J-H. Bae was with the University of California, Berkeley. He is now with the Department of Electrical Engineering, Kookmin University, Seoul 02707, South Korea.

2

voltages needed to program FeFETs with thicker FE oxides) tend to cause premature device failure [9], [10], with many groups reporting typical endurance metrics of 104-106cycles [11]–[14]. For thinner FE oxides *<*5nm in physical thickness, hot electron-induced hole damage and channel/oxide interface degradation tend to be the key agents limiting device endurance [15]. Proposals to extend the cycling lifetime of FeFETs include interfacial oxide engineering, gate workfunction engineering, modulating the material properties of the FE layer itself, and many others [16]–[21]. In this work, we combine a high-*κ* interfacial layer (IL) together with a thin FE film (*∼*4.5 nm). This is motivated by the previous observation by many authors (such as [5]) that the endurance cycling is mostly limited by IL breakdown. In fact, in a metal-FE-metal capacitor configuration, cycling endurance metrics exceeding 1010are routinely observed [2]. In a recent report, Abhishek et. al. circumvented the interfacial layer breakdown problem by fabricating a bottom-gate, channel last transistor, where an oxide semiconductor channel was grown directly on the FE material, thus achieving an endurance exceeding 1012cycles [22]. Similarly, Kim et. al. recently reported on the fabrication of vertical 3D NAND FE thin film transistors utilizing indium zinc oxide as the semiconductor channel, showing a cycling endurance of up to 108 [23]. Nonetheless, when crystalline Si is used as the channel material, as is required for high performance memory, formation of an IL is inevitable, and therefore endurance still remains a critical challenge to be addressed.

In the context of IL breakdown, it is known that ‘time-to-breakdown’ has an exponential relationship to the applied electric field in the interfacial layer [24]. In other words, a mild decrease in the electric field could still lead to a substantial increase in the ‘time-to-breakdown’, and therefore could slow the generation of traps that eventually counteract the FE hysteresis. For the same charge density, a high-*κ* IL reduces the electric field by the ratio of its permittivity to that of SiO2. Our choice of high-*κ* IL is thermal nitridation of chemically formed silicon oxide. This provides a simple way to achieve an IL with a permittivity *∼* 8. Thermally grown silicon nitride also has a comparable breakdown field to SiO2 [25]. A thin 4.5 nm of FE HZO is chosen to suppress the effects of bulk charge trapping [15] and demonstrates the thickness scalability of FE HZO. We show that this combination substantially improves the device performance. In a DC sweep, almost a 1V memory window can be achieved with just *±*2*.*5V. More importantly, with bipolar stress pulsing at *±*3V, 250 ns, the endurance exceeds 1010cycles on silicon.

3

II. EXPERIMENT AND EOT COMPARISON

The structure of the FeFET device characterized in this work is shown in Fig. 1(a), and TEMs to compare its gate stack incorporating a nitrided IL against that of a baseline device with an SiO2 IL (characterized in previous work [15]) are shown in Fig. 1(c) and Fig. 1(b), respectively. The process flow to realize the FeFET is described in [11], with the IL formation step involving thermal nitridation of the SOI substrate at 850 °C in NH3 ambient rather than a self-terminated chemical growth of SiO2. As confirmed through TEM, the FE oxide thickness of both the control SiO2 FeFET and the FeFET with a nitrided IL are the same (roughly 4.5 nm after 45 cycles of deposition). The IL thicknesses of the SiO2 IL and nitrided IL are *∼*8 ˚*A* and*∼*1.5 nm, respectively.

Fig. 1(d) compares the CV of the baseline FeFET with a SiO2 IL to the CV of the FeFET with a nitrided IL. Though the physical thickness of the gate stack of the latter is larger, its capacitance is also larger. Using Synopsys TCAD, we have estimated the net EOT of the nitrided sample to be roughly 1 ˚*A* smaller than the baseline sample, based upon the accumulation capacitances.

This allows us to make an estimate for the effective *κ* of the IL as follows:

|  |  |  |
| --- | --- | --- |
| *κ* | *t*NIL | = 3*.*9 *×*15 7*.*5 = 7*.*8 |
| *κ*NIL SiO2 *×* | *t*baseline *− δ*EOTnet |

where *κ*NIL and *κ*SiO2 indicate the *κ* values of the nitrided IL and SiO2 IL respectively; *t*NIL and *t*baseline indicate the physical thicknesses of the nitrided IL and SiO2 IL respectively; and *δ*EOTnet is the simulated EOT difference between the two ILs. This calculation indicates the IL is nearly all Si3N4. Therefore, we expect to reduce the electric field in the IL layer by two times, which will ultimately result in a substantial increase in the time to breakdown.

III. RESULTS AND DISCUSSION

We first investigate the DC hysteresis of the fabricated device with a nitrided IL. Fig. 2(a) shows results of a doubly swept *IDVG* curve. Nearly a 1V memory window can be achieved with just *±*2*.*5V sweep. We note that, compared to published literature, this is quite a low voltage requirement. For example, our baseline devices as reported in [15] do not demonstrate any appreciable memory window at *±*2*.*5V. Nonetheless it is also well known that the time to switch a given amount of polarization depends strongly on the applied voltage. Therefore, although the

4

DC sweep is a good way of visualizing the hysteresis, it is important to also probe the high-speed switching behavior. Fig. 2(b) and (c) show measured current at a read voltage of *VG* = *±*0*.*25V as a function of pulse width. We define the high current/low *VT* state as the ERS state, and the low current/high *VT* state as the PGM state. Unsurprisingly, we observe a strong dependence of the current with the applied voltage. Below 1 *µ*s, 2.5V is not good enough to provide the current level we see in the DC hysteresis. As the voltage amplitude increases, the current increases, signifying switching of a larger amount of polarization. At *VG* = 3V, the current approaches the level seen in DC hysteresis, even for a pulse width of *∼* 100 ns. Similarly, for the PGM state, *VG* = *−*3V brings the current level down to almost the level seen in the DC hysteresis at a pulse width of *∼* 250 ns. The asymmetry between PGM and ERS states is expected – accumulation of a thin SOI body requires a much larger voltage drop across the semiconductor, as discussed in previous reports [4]. Therefore, for a reasonably fast and symmetric operation, we choose a pulse width of 250 ns and a gate voltage of *VG* = *±*3V for endurance cycling.

In many studies, the endurance is quantified by measuring *±VT* after a certain number of bipolar stress pulses. The *±VT* determination requires one to perform sweeps over a small voltage range, which typically takes *∼* 1 second to complete. On the other hand, the importance of fast reading has recently been discussed (e.g. [22]). It is known from charge pumping experiments (as discussed in [15], [26]) that beyond several *µ*s, charge trapping/de-trapping starts to manifest. These effects could in principle be quite complex, and could arise from the interplay between traps with varying time constants. Therefore, while slow sweeps to determine *±VT* could provide important insights into trap assisted phenomena, they are also expected to *artificially* affect the actual currents that will be observed in a real application where the device is read quickly. Due to these considerations, we adopt fast reading of the device to determine its state. The complete endurance testing protocol is detailed in Fig. 3(a). During the stressing phase of the endurance test, bipolar voltage pulses of *±*3V, 250 ns are applied at the gate of the FeFET, with a 250 ns delay between sequential pulses to achieve a stressing period of 1 *µ*s total in duration. Periodically, a state determination test is conducted to evaluate the margin between the PGM and ERS states. For this, a 10 *µ*s read pulse is applied at the gate of the FeFET (after either the ERS or PGM pulse), after ramping and stabilizing the drain voltage to 50 mV (see Fig. 3(a), right panel). The averaged current value during this 10 *µ*s reading period is determined to be the read current. Figs. 3(b) and (c) show the readout current during the 10 *µ*s reading period for the high *VT* (PGM) and low *VT* (ERS) states, respectively. In both cases, the current saturates well within

5

the READ duration of 10 *µ*s.

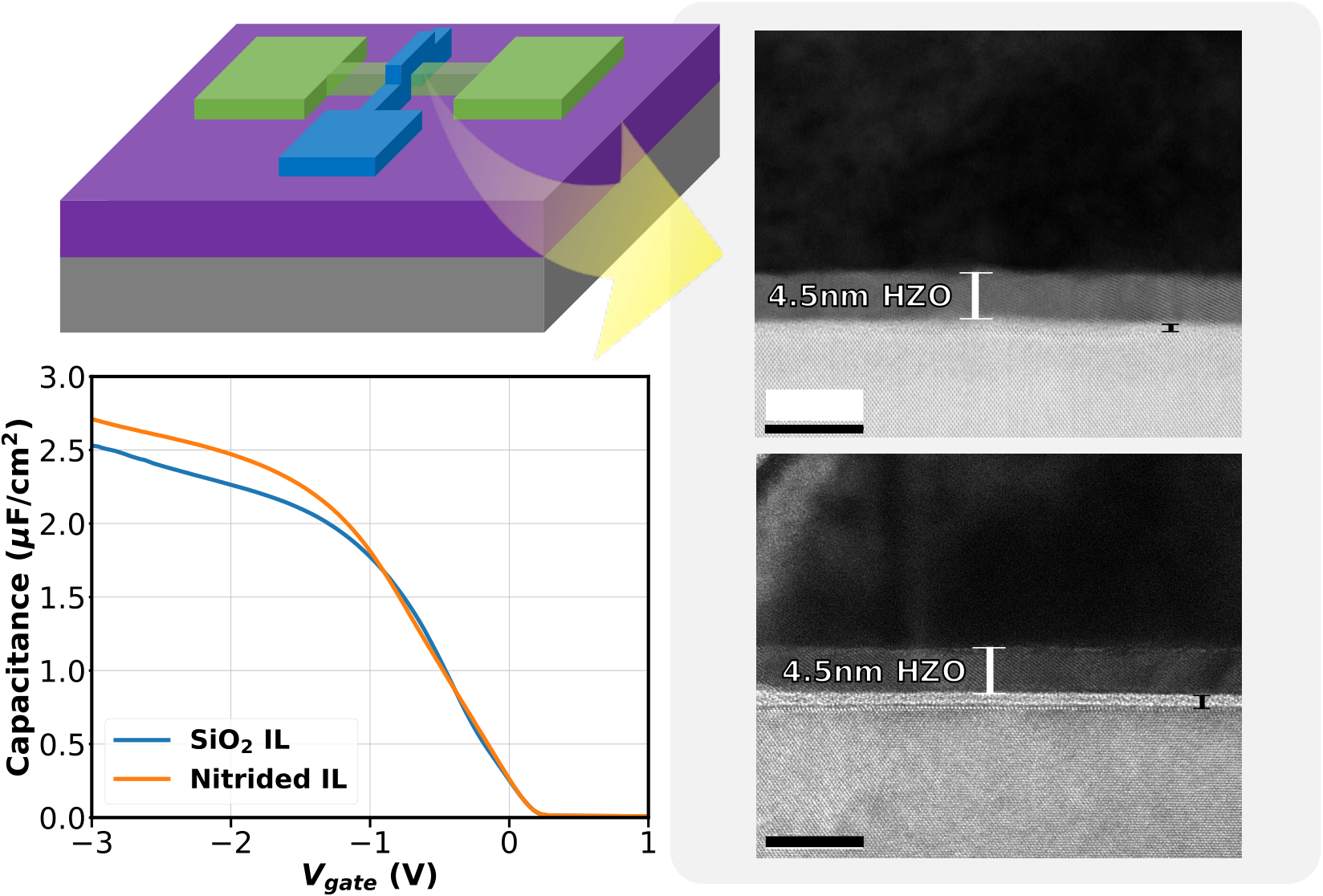
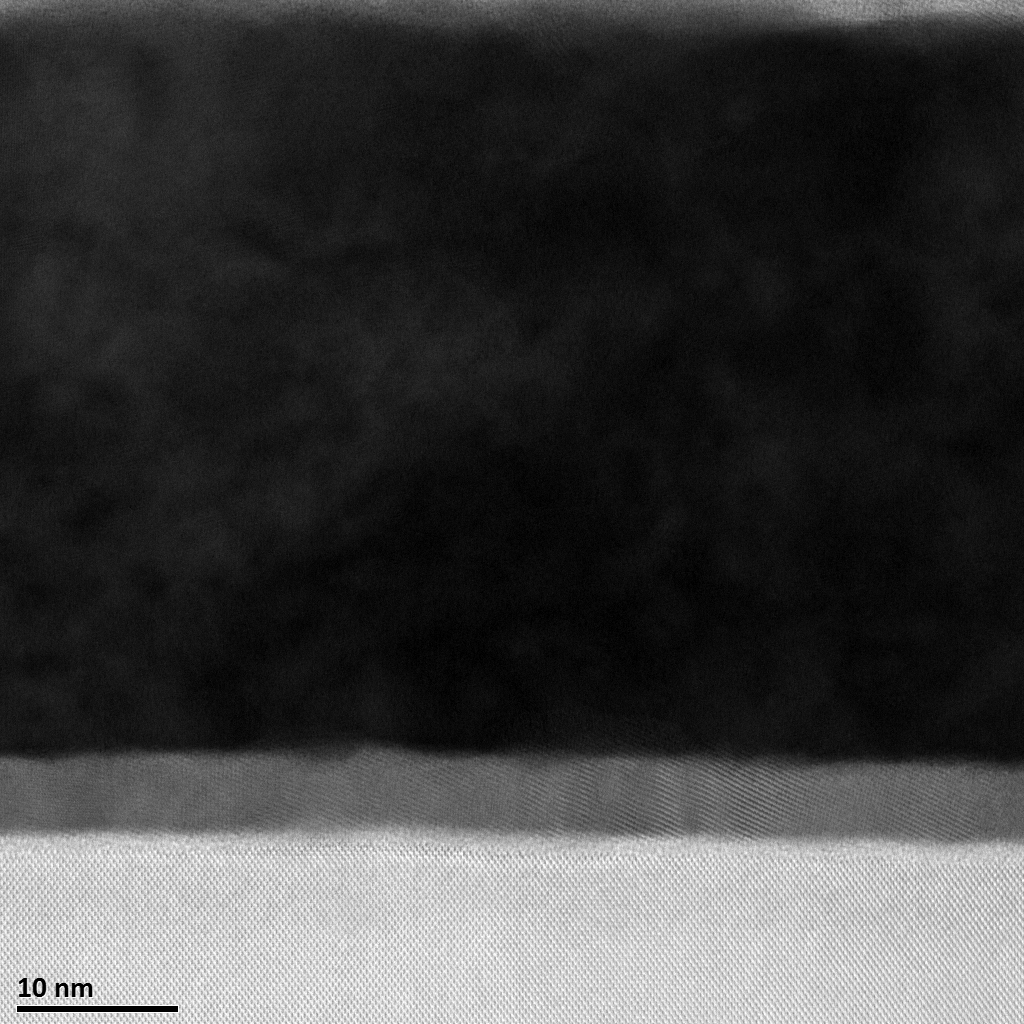
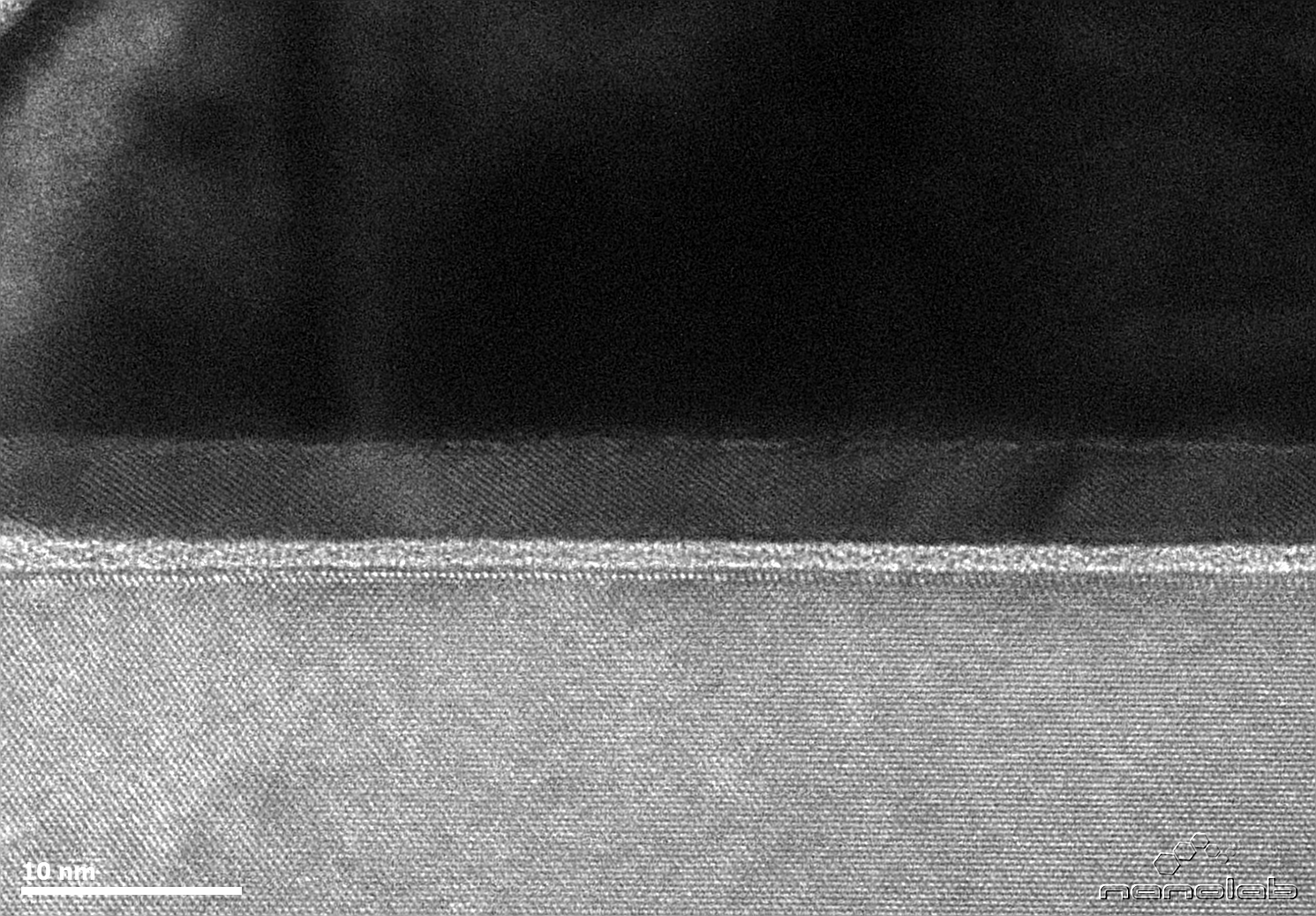
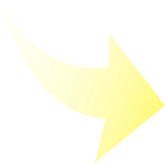
Fig. 4(a) shows the results of endurance testing across different devices, proving that the devices with a nitrided IL can be reliably cycled to 1010. The data is plotted as *I*ERS*/I*PGM vs. fatigue cycles for ease of comparison. The exact current levels are shown for a device in Fig. 4(b). First, we note that the high and low current levels are very similar to those measured from a DC sweep. This indicates that the device is switched properly with the PGM/ERS pulses. Interestingly, the device does not show any rapid degradation after 104*−* 106cycles, as reported in most studies. Rather, the high current level shows a slow degradation. The envelope of the low current similarly shows a slow degradation (increase); yet the separation of the current levels retains a margin of 103until 6*×*1010cycles. Beyond that point, a sudden breakdown is observed. Notably, this sudden breakdown is correlated with the gate leakage through the device shooting up several orders of magnitude, as shown in Fig. 4(c), indicating that the gate oxide itself breaks down close to 1011cycles. We note that, there are devices that does not experience such a breakdown. For example, Fig. 4(d) shows DC *IDVG* sweep from an exemplary device cycled to 1012. The anti-clockwise Hysteresis is still clearly visible. This should compared with previous studies where total reversal of handedness of Hysteresis happens after just 104-105cycles. This also shows that the Ferroelectric itself remains quite robust even after one trillion cycles. Finally, we present the retention behavior. As seen in Fig. 5, the retention looks unaffected for a testing duration of 104seconds for both the PGM and ERS states. The retention looks robust at both 25°C and 85°C. Thus despite relatively lower voltage operation and very large endurance, there is no discernible effect on the retention behavior.

IV. CONCLUSION

In conclusion, we have demonstrated a FeFET memory device with an engineered high-*κ* IL that shows larger than 1010endurance cycles at a relatively small PGM/ERS voltage of *VG* = *±*3V and pulse width of 250 ns. Endurance measured on multiple devices show robust and repeatable behavior over 1010endurance cycles. We have identified total oxide breakdown as the main limiting factor as opposed to defect (interface and bulk) induced clock-wise Hysteresis that has been reported by many previous studies. Understanding charge injection during the endurance test and optimizing to reduce the total oxide breakdown could increase the endurance over 1012cycles, as our data shows that the FE film remains robust even beyond that cycling number. Additional optimization of the IL and FE layers could allow for further reduction in the

6

operating voltage to below 2V, while maintaining and/or even enhancing the endurance behavior. One potential drawback of using such a high-*κ* IL could be a reduction in mobility. However, somewhat reduced mobility could still be tolerable as these devices are not expected to compete with the gate-delay of logic devices.



7

|  |  |  |  |
| --- | --- | --- | --- |
| **(a)** | **source** | **drain** | **(b)** |

**gate**

**BOX**

|  |  |
| --- | --- |
| **Silicon** | **8.2Å IL** |

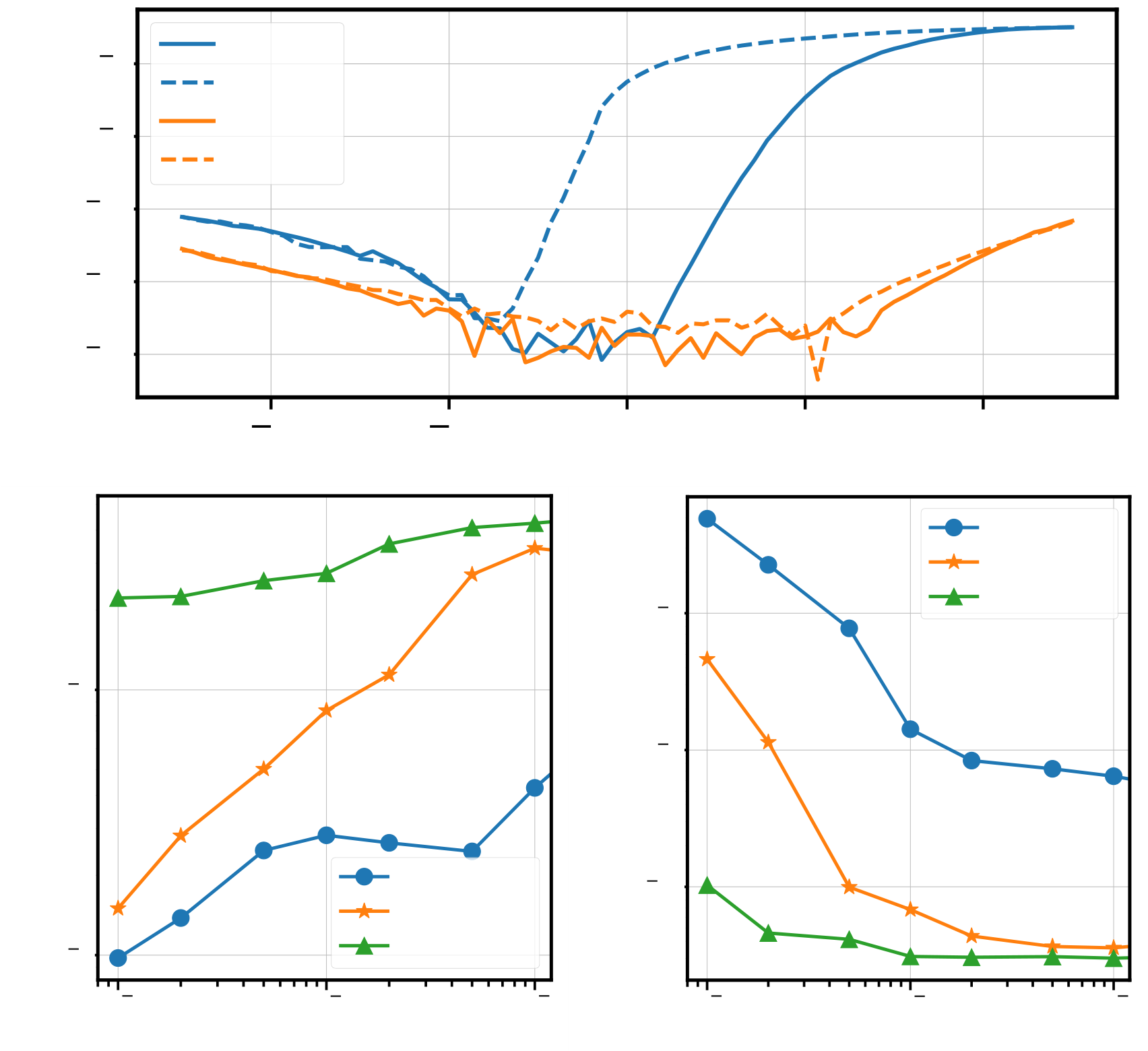
**10 nm**

**(c)**

**1.5nm IL**

**(d)**   
 **10 nm**

Fig. 1. (a) Schematic of a SOI, gate-first FeFET device. (b) TEM of 4.5 nm HZO gate stack with 8.2 ˚*A* SiO2 IL. (c) TEM of 4.5 nm HZO gate stack with 1.5 nm SiNxIL. (d) CV comparison of gate stack with SiO2 IL to the gate stack with nitrided IL, both taken at 100 kHz.



8

10 6 ID, PGM

ID, ERS

Idrain or Igate (A) Drain Current at VG = 0.25V (A)   
 10 8 IG, PGM

IG, ERS

10 10

10 12

10 14 (a)

2 1 0 1 2

Vgate (V)

(b) ID, -2.5V Drain Current at VG = 0.25V (A)   
 ID, -2.75V

10 8 ID, -3V

10 6

10 9

ID, +2.5V 10 10

ID, +2.75V

10 7 ID, +3V (c)

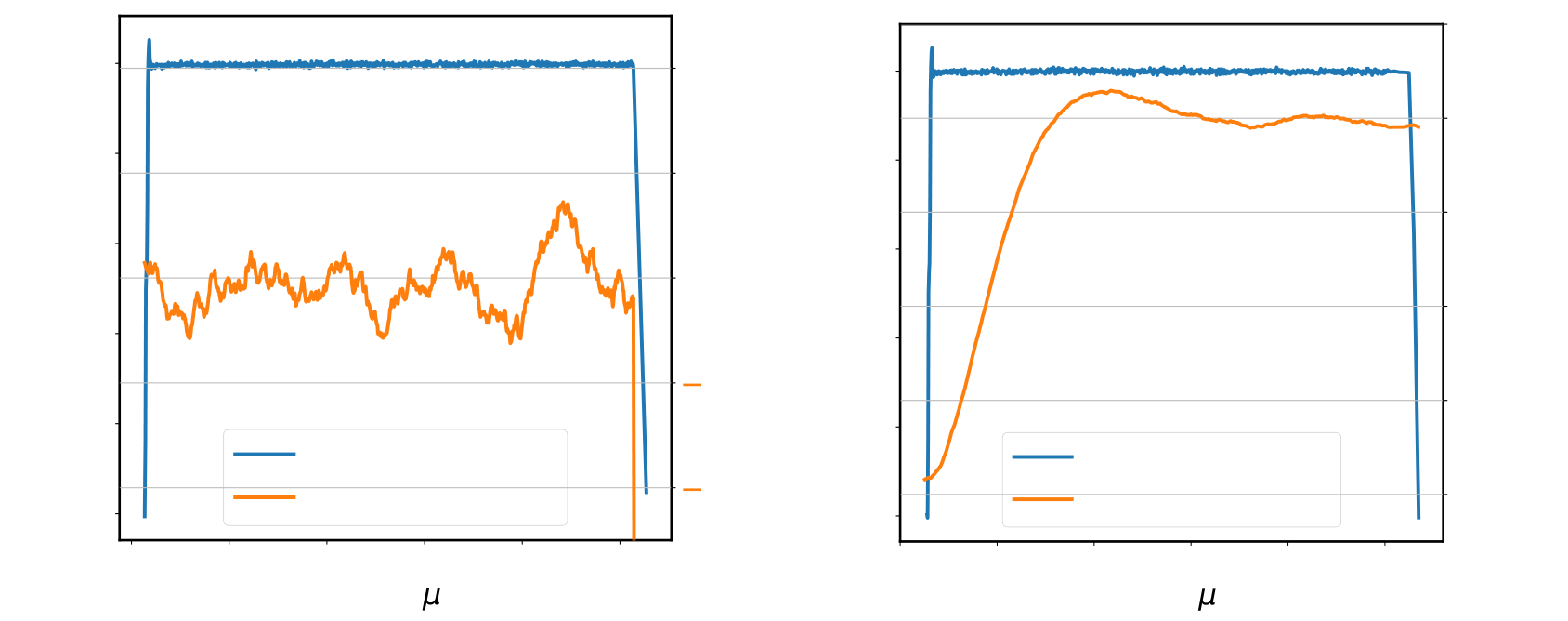
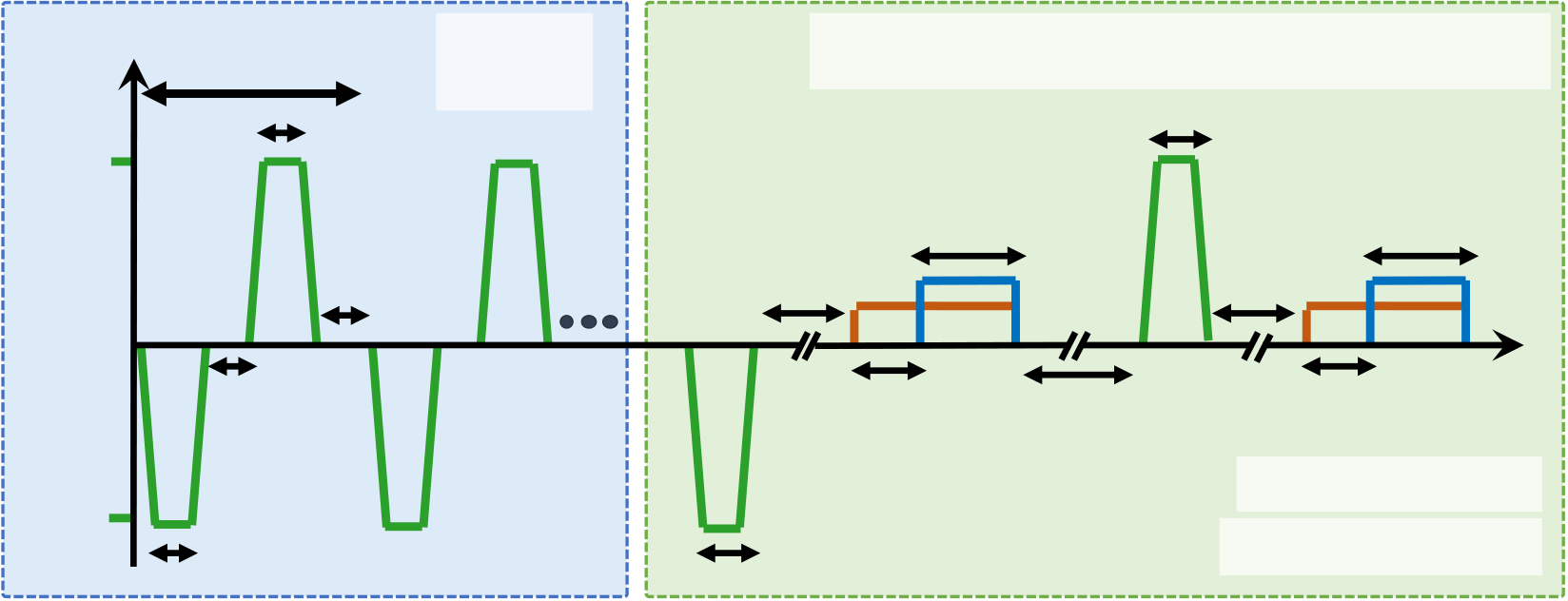
10 7 10 6 10 5 10 7 10 6 10 5

Pulse Duration (s) Pulse Duration (s)

Fig. 2. (a) *IDVG* of a typical FeFET with 4.5 nm HZO on a 1.5 nm nitrided IL. The device is doubly-swept from *±*2*.*5V

at a drain bias of *VD* =50 mV. (b) Typical ERS characteristics for the FeFET. (c) Typical PGM characteristics for the FeFET.

Voltage magnitudes range from *±*2*.*5 *−* 3V and pulse durations from 100 ns to 10 *µ*s.



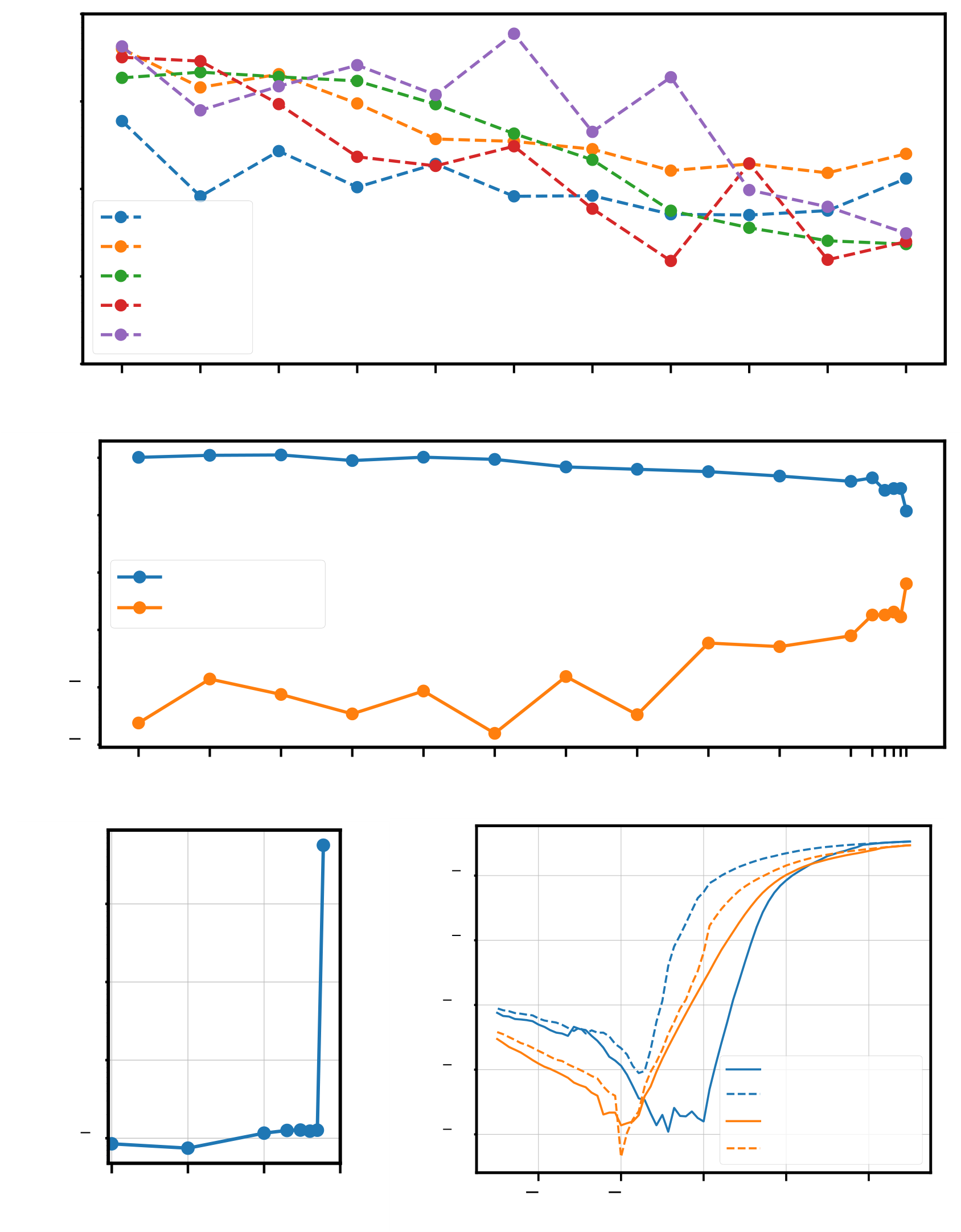
9

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **(a)** | | **Stressing Sequence** | | | | | | **Determination of FE State**  **trise/fall = 10ns for all cycling and state waveforms**  **Pulse durations/amplitudes not drawn to scale**  **th** | | | | | | | | | | | |
| **V(t)** | | | **tpd = 1μs** | | **VG,cycle** | | |
| **= ±3V** | | |
| **+3V** | | **th** | | | | | |
| **tw,1 =** | | | **tread =** | | | **tw,** | | | | **tread** | |
| **td**  **td =**  **250ns**  **th =**  **250ns** | | | | | | | | **10μs** | | |
| **80μs** | | |
| **1** | | | | | | | | | | **t** | |
| **tstab =** | | | | **tw,2 =** | | | **tstab** | | | | |
| **20μs** | | | | **VG,read = 0.25V** | | | | |
| **100μs** | | |
| **th** | | | | **VD,read = 50mV** | | | | | | | |
| 0.25 | | (b) | | | | | | 40 | 0.25 | | | (c) | | | | | | | 1200 |
| Gate Voltage VG (V) | 0.20 | Gate Voltage VG  Drain Current ID | | | | | | Drain Current ID (nA) 20  0   20 | Gate Voltage VG (V) | 0.20 | | Gate Voltage VG Drain Current ID | | | | | | 1000   Drain Current ID (nA)  800  600  400 | |
| 0.15 |
| 0.15 | |
| 0.10 |
| 0.10 | |
| 0.05 |
| 0.05 | |
| 0.00 | 40 |
| 200 | |
| 0.00 | |
| 104 | | 106 | | 108 110  Time ( s) | | 112 | 114 | 318 | | | | 320 | 322 324  Time ( s) | | | 326 | 328 | | |

Fig. 3. (a) Endurance stressing sequence and subsequent ferroelectric state determination waveforms used to characterize the

FeFETs in this work. (b) Transient current readout waveform corresponding to the high *VT* state (and low readout current). (c)

Transient current readout waveform corresponding to the low *VT* state (and high readout current).



10

105 (a) IERS/IPGM at VG = 0.25V (nA) ID at VG = 0.25V (nA) IG at VG = 2.5V (nA)   
 104

103

Device 1

Device 2

102 Device 3

Device 4

Device 5

101

100 101 102 103 104 105 106 107 108 109 1010

Bipolar Fatigue Cycles

103

102

101 Low VT State

High VT State

100

10 1

10 2 (b)

100 101 102 103 104 105 106 107 108 109 1010

Bipolar Fatigue Cycles

(c)

10 6 (d)

102

10 8

Idrain (A)   
101

10 10

100 10 12 PGM, 1 cycle

ERS, 1 cycle

10 1 10 14 PGM, 1012 cycles

ERS, 1012 cycles

108 109 1010 1011 2 1 0 1 2

Bipolar Fatigue Cycles Vgate (V)

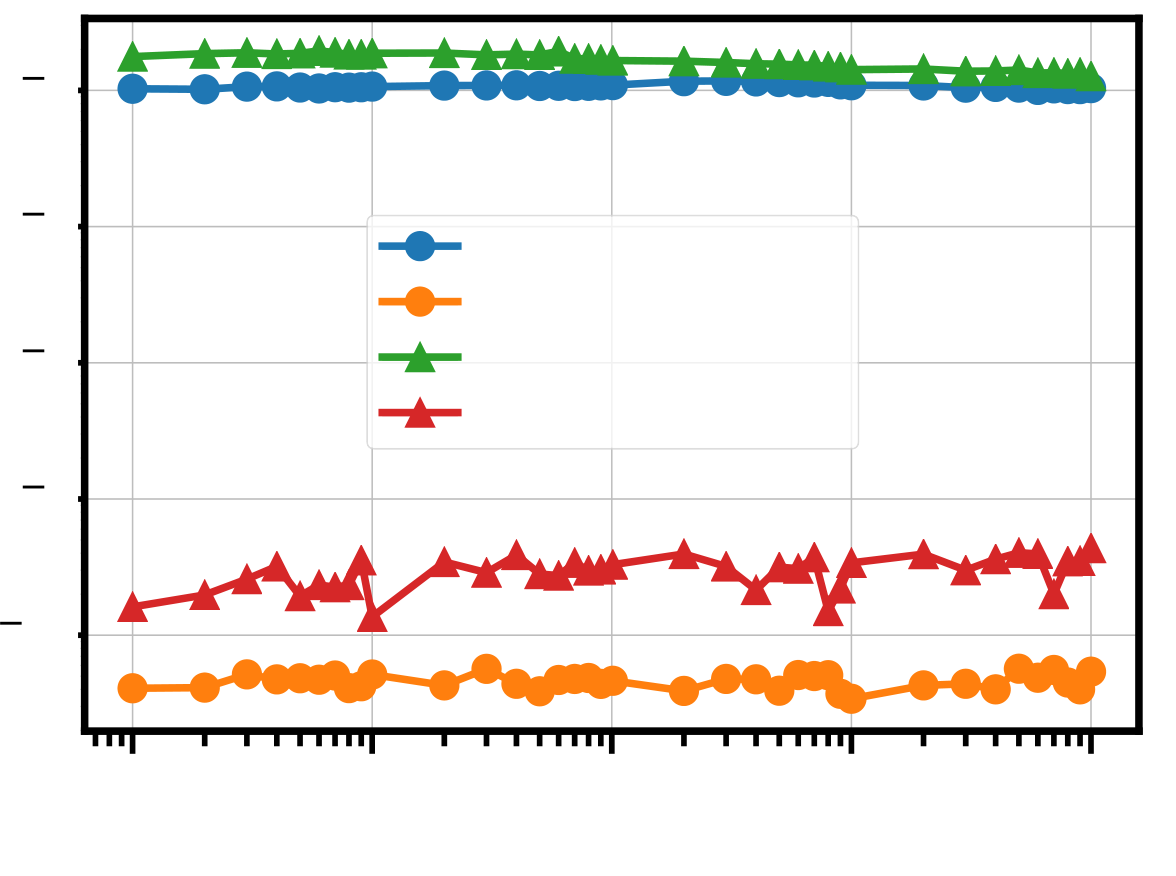
Fig. 4. (a) Endurance characteristics of multiple FeFET devices cycled from 1 to 1010fatigue cycles. Results are reported as

the ratio of the low *VT ID* readout to the high *VT ID* readout at every decade of cycling. (b) A device cycled until *∼*1 order

of magnitude of current separation remains after 6 *×* 1010cycles. (c) *IG* at *VG* = 2*.*5V as a function of cycling for the same

device in (b), showing a strong correlation between oxide wearout and loss of memory window. (d) *IDVG*’s of an exemplary

device cycled to 1012cycles, showing some remaining ferroelectric hysteresis at the end of the endurance test.



11

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 10 | | 6 | 100 | ERS state ID, 25°C  PGM state ID, 25°C  ERS state ID, 85°C  PGM state ID, 85°C | 104 |
| ID Readout (A) | 10 10 10 | 7 |
| 8 |
| 9 |
| 10 | | 10 | 101 102 103  Time (seconds) |

Fig. 5. Retention testing at room temperature (25 °C) and at elevated (85 °C) for 104seconds. Gate read voltage is chosen

to the same at both testing conditions after correcting for the leftward *VT* shift due to an effective substrate doping change at

elevated temperature.

12

REFERENCES

[1] A. J. Tan, L. C. Wang, Y. H. Liao, J. H. Bae, C. Hu, and S. Salahuddin, “Reliability of ferroelectric hfo2-based memories: From mos capacitor to fefet,” in *2020 Device Research Conference (DRC)*, 2020. doi: 10.1109/DRC50226.2020.9135148 pp. 1–2.

[2] M. Peˇsi´c, U. Schroeder, S. Slesazeck, and T. Mikolajick, “Comparative study of reliability of ferroelectric and anti- ferroelectric memories,” *IEEE Transactions on Device and Materials Reliability*, vol. 18, no. 2, pp. 154–162, 2018. doi: 10.1109/TDMR.2018.2829112   
[3] H. Mulaosmanovic, E. T. Breyer, T. Mikolajick, and S. Slesazeck, “Recovery of cycling endurance failure in ferroelectric fets by self-heating,” *IEEE Electron Device Letters*, vol. 40, no. 2, pp. 216–219, 2019. doi: 10.1109/LED.2018.2889412 [4] J. H. Bae, D. Kwon, N. Jeon, S. Cheema, A. J. Tan, C. Hu, and S. Salahuddin, “Highly scaled, high endurance, omega-gate, nanowire ferroelectric fet memory transistors,” *IEEE Electron Device Letters*, vol. 41, no. 11, pp. 1637–1640, 2020. doi: 10.1109/LED.2020.3028339   
[5] K. Chatterjee, S. Kim, G. Karbasian, A. J. Tan, A. K. Yadav, A. I. Khan, C. Hu, and S. Salahuddin, “Self-aligned, gate last, fdsoi, ferroelectric gate memory device with 5.5-nm hf0.8zr0.2o2, high endurance and breakdown recovery,” *IEEE*  *Electron Device Letters*, vol. 38, no. 10, pp. 1379–1382, 2017. doi: 10.1109/LED.2017.2748992   
[6] H. Liu, C. Wang, G. Han, J. Li, Y. Peng, Y. Liu, X. Wang, N. Zhong, C. Duan, X. Wang, N. Xu, T. K. Liu, and Y. Hao, “Zro2 ferroelectric fet for non-volatile memory application,” *IEEE Electron Device Letters*, vol. 40, no. 9, pp. 1419–1422, 2019. doi: 10.1109/LED.2019.2930458   
[7] K. Lee, J. Bae, S. Kim, J. Lee, B. Park, and D. Kwon, “Ferroelectric-gate field-effect transistor memory with recessed channel,” *IEEE Electron Device Letters*, vol. 41, no. 8, pp. 1201–1204, 2020. doi: 10.1109/LED.2020.3001129 [8] A. J. Tan, Z. Zhu, H. S. Choe, C. Hu, S. Salahuddin, and A. Yoon, “Ferroelectric si-doped hfo2 capacitors for next- generation memories,” in *2019 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, 2019. doi: 10.1109/VLSI-TSA.2019.8804657 pp. 1–2.

[9] E. Yurchuk, J. M¨uller, S. M¨uller, J. Paul, M. Peˇsi´c, R. van Bentum, U. Schroeder, and T. Mikolajick, “Charge-trapping phenomena in hfo2-based fefet-type nonvolatile memories,” *IEEE Transactions on Electron Devices*, vol. 63, no. 9, pp.

3501–3507, 2016. doi: 10.1109/TED.2016.2588439   
[10] H. Mulaosmanovic, E. T. Breyer, T. Mikolajick, and S. Slesazeck, “Ferroelectric fets with 20-nm-thick hfo2 layer for large memory window and high performance,” *IEEE Transactions on Electron Devices*, vol. 66, no. 9, pp. 3828–3833, 2019.

doi: 10.1109/TED.2019.2930749   
[11] A. J. Tan, K. Chatterjee, J. Zhou, D. Kwon, Y. Liao, S. Cheema, C. Hu, and S. Salahuddin, “Experimental demonstration of a ferroelectric hfo2-based content addressable memory cell,” *IEEE Electron Device Letters*, vol. 41, no. 2, pp. 240–243, 2020. doi: 10.1109/LED.2019.2963300   
[12] K. . Chen, H. . Chen, C. . Liao, G. . Siang, C. Lo, M. . Liao, K. . Li, S. T. Chang, and M. H. Lee, “Non-volatile ferroelectric fets using 5-nm hf0.5zr0.5o2 with high data retention and read endurance for 1t memory applications,” *IEEE Electron*  *Device Letters*, vol. 40, no. 3, pp. 399–402, 2019. doi: 10.1109/LED.2019.2896231   
[13] T. Ali, P. Polakowski, S. Riedel, T. B¨uttner, T. K¨ampfe, M. Rudolph, B. P¨atzold, K. Seidel, D. L¨ohr, R. Hoffmann, M. Czernohorsky, K. K¨uhnel, P. Steinke, J. Calvo, K. Zimmermann, and J. M¨uller, “High endurance ferroelectric hafnium oxide-based fefet memory without retention penalty,” *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3769–3774, 2018. doi: 10.1109/TED.2018.2856818   
[14] K. Florent, S. Lavizzari, L. Di Piazza, M. Popovici, E. Vecchio, G. Potoms, G. Groeseneken, and J. Van IHoudt, “First

13

demonstration of vertically stacked ferroelectric al doped hfo 2 devices for nand applications,” in *2017 Symposium on VLSI Technology*. IEEE, 2017, pp. T158–T159.

[15] A. J. Tan, M. Peˇsic, L. Larcher, Y. H. Liao, L. C. Wang, J. H. Bae, C. Hu, and S. Salahuddin, “Hot electrons as the dominant source of degradation for sub-5nm hzo fefets,” in *2020 IEEE Symposium on VLSI Technology*, 2020. doi: 10.1109/VLSITechnology18217.2020.9265067 pp. 1–2.

[16] A. J. Tan, A. K. Yadav, K. Chatterjee, D. Kwon, S. Kim, C. Hu, and S. Salahuddin, “A nitrided interfacial oxide for interface state improvement in hafnium zirconium oxide-based ferroelectric transistor technology,” *IEEE Electron Device*  *Letters*, vol. 39, no. 1, pp. 95–98, 2018. doi: 10.1109/LED.2017.2772791   
[17] S. Deng, Z. Liu, X. Li, T. P. Ma, and K. Ni, “Guidelines for ferroelectric fet reliability optimization: Charge matching,” *IEEE Electron Device Letters*, vol. 41, no. 9, pp. 1348–1351, 2020. doi: 10.1109/LED.2020.3011037   
[18] K. Ni, P. Sharma, J. Zhang, M. Jerry, J. A. Smith, K. Tapily, R. Clark, S. Mahapatra, and S. Datta, “Critical role of interlayer in hf0.5zr0.5o2 ferroelectric fet nonvolatile memory performance,” *IEEE Transactions on Electron Devices*, vol. 65, no. 6, pp. 2461–2469, 2018. doi: 10.1109/TED.2018.2829122   
[19] A. G. Chernikova, M. G. Kozodaev, D. V. Negrov, E. V. Korostylev, M. H. Park, U. Schroeder, C. S. Hwang, and A. M.

Markeev, “Improved ferroelectric switching endurance of la-doped hf0.5zr0.5o2 thin films,” *ACS Applied Materials &*  *Interfaces*, vol. 10, no. 3, pp. 2701–2708, 2018. doi: 10.1021/acsami.7b15110 PMID: 29282976. [Online]. Available: <https://doi.org/10.1021/acsami.7b15110>  
[20] R. Cao, B. Song, D. Shang, Y. Yang, Q. Luo, S. Wu, Y. Li, Y. Wang, H. Lv, Q. Liu, and M. Liu, “Improvement of endurance in hzo-based ferroelectric capacitor using ru electrode,” *IEEE Electron Device Letters*, vol. 40, no. 11, pp.

1744–1747, 2019. doi: 10.1109/LED.2019.2944960   
[21] S. Oh, J. Song, I. K. Yoo, and H. Hwang, “Improved endurance of hfo2-based metal- ferroelectric-insulator-silicon structure by high-pressure hydrogen annealing,” *IEEE Electron Device Letters*, vol. 40, no. 7, pp. 1092–1095, 2019.

doi: 10.1109/LED.2019.2914700   
[22] A. A. Sharma, B. Doyle, H. J. Yoo, I.-C. Tung, J. Kavalieros, M. V. Metz, M. Reshotko, P. Majhi, T. Brown-Heft, Y.-J. Chen, and V. H. Le, “High speed memory operation in channel-last, back-gated ferroelectric transistors,” in *2020 International*  *Electron Devices Meeting*. IEEE, 2020.

[23] M.-K. Kim, I.-J. Kim, and J.-S. Lee, “Cmos-compatible ferroelectric nand flash memory for high-density, low-power, and high-speed three-dimensional memory,” *Science Advances*, vol. 7, no. 3, 2021. doi: 10.1126/sciadv.abe1341. [Online].

Available: <https://advances.sciencemag.org/content/7/3/eabe1341>  
[24] K. F. Schuegraf and C. Hu, “Hole injection sio/sub 2/breakdown model for very low voltage lifetime extrapolation,” *IEEE*  *transactions on electron devices*, vol. 41, no. 5, pp. 761–767, 1994.

[25] T. Ito, T. Nozaki, H. Arakawa, and M. Shinoda, “Thermally grown silicon nitride films for high-performance mns devices,” *Applied Physics Letters*, vol. 32, no. 5, pp. 330–331, 1978.

[26] M. Pesic, A. Padovani, S. Slcsazeck, T. Mikolajick, and L. Larcher, “Deconvoluting charge trapping and nucleation interplay in fefets: Kinetics and reliability,” in *2018 IEEE International Electron Devices Meeting (IEDM)*, 2018. doi: 10.1109/IEDM.2018.8614492 pp. 25.1.1–25.1.4.