

IEEE ELECTRON DEVICE LETTERS, VOL. 39, NO. 1, JANUARY 2018 95



A Nitrided Interfacial Oxide for Interface State

Improvement in Hafnium Zirconium Oxide-

Based Ferroelectric Transistor Technology

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***Abstract— We examine the nature of the interface states induced during the integration of ferroelectric hafnium zirconium oxide on silicon. Metal-ferroelectric-insulator-silicon capacitors, with a thin layer of hafnium zirconium oxide grown by atomic layer deposition as the ferroelectric and various interfacial oxide layers as the insulator, are investigated. Since a high-temperature post-annealing is necessary to induce the formation of the ferroelectric phase in this oxide stack, the integrity of the oxide/silicon inter-face must be preserved after high-temperature processing. As such, we show that a nitrided interlayer provides an improved midgap interface state density among all interfa-cial oxides investigated. Furthermore, we quantify the inter-face states using the ac conductance technique and model the interface trap distribution across the silicon bandgap in order to explain and verify the experimental measurements.***

***Index Terms— Ferroelectrics, hafnium zirconium oxide, high-k dielectrics, interface traps, ac conductance.***

I. INTRODUCTION   
**F** in recent years with the discovery of ferroelectricity in ERROELECTRICS have garnered much renewed interest

a commercially prevalent high-*κ* dielectric, HfO2 [1]. Many different dopants, such as Zr [2], Si [3], Al [4], Gd [5],

and Sr [6] have since been shown to successfully stabilize

the ferroelectric phase, which has been linked to the non-

centrosymmetic orthorhombic crystalline phase of HfO2. This critical discovery bodes well for the design of low-power

embedded, non-volatile memory and negative capacitance

transistor devices [2], [7], [8]. Moreover, because HfO2-based thin films can be ferroelectric down to a mere 2.5 nm [9], they

are especially attractive in the context of aggressively scaled

devices. Particularly, as HfO2 is now well-incorporated into

Manuscript received October 29, 2017; accepted November 8, 2017. Date of publication November 13, 2017; date of current version December 27, 2017. This work was supported in part by the Berkeley Center for Negative Capacitance Transistors and the E2CDA ENIGMA center jointly funded by NSF and GRC/NRI. The review of this letter was arranged by Editor B. S. Doyle. (Corresponding author: Ava J. Tan.) A. J. Tan, A. K. Yadav, K. Chatterjee, D. Kwon, C. Hu, and S. Salahuddin are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, Berkeley, CA 94720 USA (e-mail: ava@eecs.berkeley.edu).

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Digital Object Identifier 10.1109/LED.2017.2772791

the gate stack of modern CMOS transistors, the discovery of ferroelectricity in HfO2-based films expedites the development of CMOS-compatible ferroelectric transistor technology.

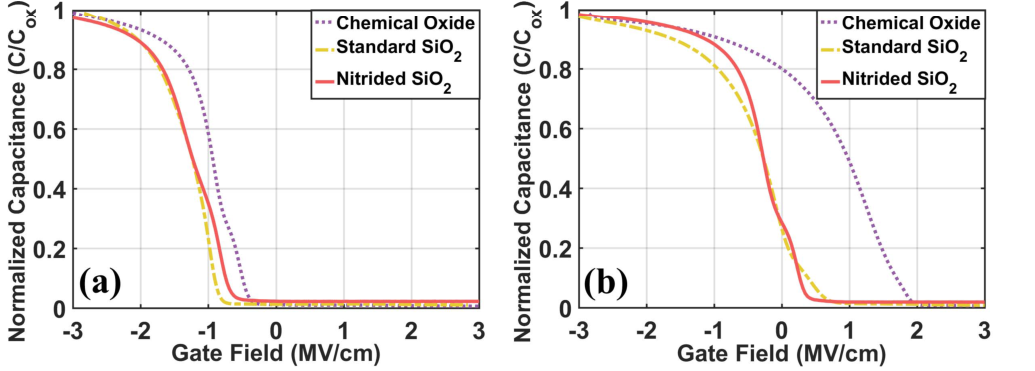
However, one of the major potential challenges barring suc-cessful integration of ferroelectric HfO2 is the poor interface between the silicon substrate and the ferroelectric material. The atomic layer deposition (ALD) process can be tuned to produce a high quality HfO2-based gate oxide, but the subse-quent stabilization of the ferroelectric phase involves a moder-ately high temperature anneal (commonly 400 °C or higher), which may perturb the interface between oxide and silicon. The effects of this so-called phase anneal on film crystallinity are well-documented [10], [11], but the effects on interfacial properties are yet to be properly understood.

In this letter, we investigate the effects of the ferroelectric phase anneal on the interface properties of a MOSCAP device. By utilizing the AC conductance technique proposed by Nicollian and Goetzberger [12], the midgap trap density (*Dit*) is measured directly. Furthermore, we show that a nitrided interfacial layer between hafnium zirconium oxide (HZO) and the silicon substrate minimizes degradation of the interface during the ferroelectric phase anneal, yielding a device with a peak midgap trap density in the mid-1011cm−2eV−1range, which is amenable for modern day device technologies.

II. EXPERIMENT

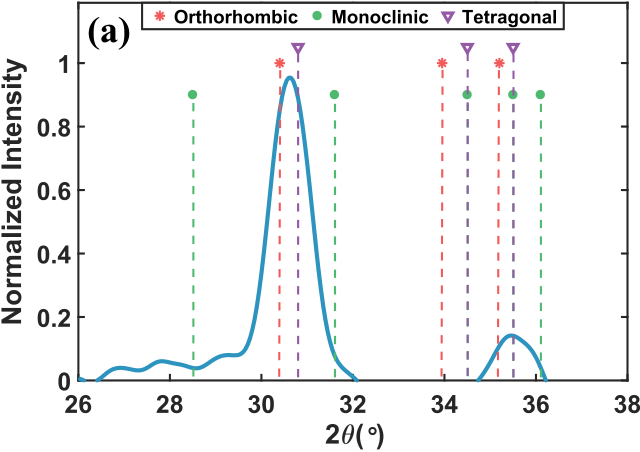
Three different interfacial oxides on lightly doped (1015cm−3) p-type silicon substrates were investigated: chem-ical oxide, thermal SiO2, and thermal nitrided SiO2. The chemical oxide was grown by placing a cleaned substrate in a heated solution of 2 NH4OH:5 H2O2:200 H2O, producing several monolayers of oxide. Thermal SiO2 was grown by placing a silicon substrate in a rapid thermal annealing (RTA) chamber at 900 °C in an O2 ambient for 20 seconds. Nitrided SiO2 was grown by placing a silicon substrate in a RTA cham-ber at 900 °C in O2 for 10 seconds followed by N2O for 5 seconds in situ. Next, alternating monolayers of HfO2 and ZrO2 were grown by ALD to achieve an overall film composition of Hf0*.*5Zr0*.*5O2. 100 total cycles were deposited to yield a film thickness of roughly 8.9 nm as determined by X-ray reflectometry (XRR). 60 nm of TiN was then sputtered onto the stacks, which were subsequently annealed in an RTA tool at 500 °C for 30 seconds in an N2 ambient to crystallize the HZO film.

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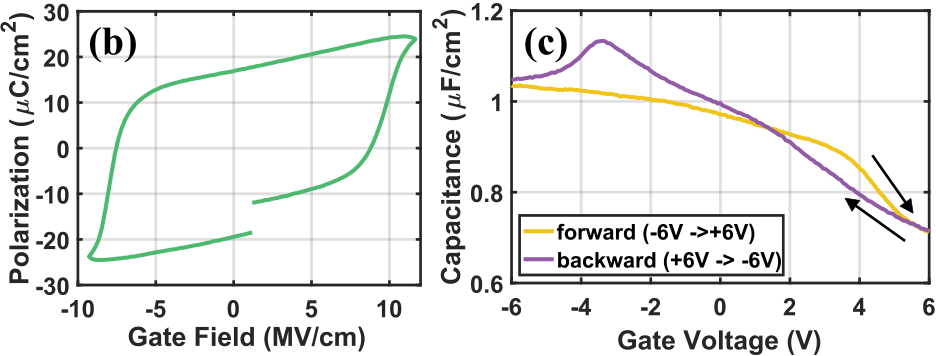


Fig. 1. Proof of ferroelectricity in annealed HZO films. (a) A GIXRD diffractogram, taken with an incident angle of 0.35°, suggests orthorhom-bic/tetragonal crystalline phases in a 100 cycle ALD Hf0.5Zr0.5O2. (b) PE (polarization-electric field) measurement on a 100 cycle ALD Hf0.5Zr0.5O2 film. (c) CV measurement on a 100 cycle ALD Hf0.5Zr0.5O2 film.

The mixed crystalline phases in the resulting polycrystalline films were characterized with grazing incidence X-ray diffrac-tion (GIXRD). Electrical measurements were taken using a Keysight B1500A Semiconductor Parameter Analyzer.

III. RESULTS AND DISCUSSION   
 For structural characterization, grazing-incidence X-ray dif-fraction (GIXRD) was performed on the annealed HZO films. As depicted in Fig. 1a, the GIXRD scan shows a set of diffraction peaks which suggests the presence of orthorhom-bic and/or tetragonal phases of hafnia [10]. The absence of diffraction peaks corresponding to the monoclinic phases of HfO2 or ZrO2 [13] or any other impurity phases of Hf*x*Zr1−*x*O2 [14] can also be seen in the same scan. To complement the XRD results, ferroelectric proper-ties have been further verified through PE (polarization-electric field) and CV (capacitance-voltage) data shown in Fig. 1b and 1c, respectively. The representative PE and CV data shown here are taken on device stacks nearly identical to the ones discussed in the experimental section, except a degenerately doped (1019cm−3) Si substrate is used as a highly conductive back electrode. The remanent polarization value is 14.73 *μ*C/cm2over a sweep range of ± 10 MV/cm, as seen in Fig. 1b.

After the 500 °C ferroelectric phase anneal, it is observed that stretch-out occurs in the CV characteristics of the capac-itors with chemical oxide or with standard SiO2 as the interfacial layer, as seen in Fig. 2. Furthermore, in com-paring Figs. 2a and 2b, the stretch-out suggests that the midgap *Dit* in particular increases more dramatically for the sample with SiO2 or chemical oxide as an interfacial layer. This phenomenon suggests that a strong degradation of the interface of the oxide/Si stack has occurred as a result of the anneal, particularly because the Si/SiO2 system is known to exhibit an intrinsically low interface trap density [15], [16]. The capacitor with nitrided SiO2 demonstrates the least

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| Fig. 2. | Normalized CV curves for samples with chemical oxide (dotted |
| purple), standard SiO2 (dash-dotted yellow), and nitrided SiO2 (solid red). (a) Representative CV curves before the ferroelectric phase anneal.  (b) Representative CV curves after annealing. | |

stretch-out, suggesting that this device structure possesses the lowest overall *Dit* after annealing.

The CV curves in Fig. 2 are plotted with capacitance values normalized to *Cox* and applied voltage normalized to film thickness (represented as electric field) to account for differ-ences in equivalent oxide thickness. For comparison, a rep-resentative CV prior to annealing is shown in the inset. The The cause of the strong flatband voltage shift for the sam-voltage sweep direction for each device is from −3V to +3V. ple with chemical oxide in comparison to the samples with thermally grown interfacial oxides may be due to differing nucleation and growth mechanisms of the ALD HZO film on surfaces terminated via different synthesis techniques.

It is therefore hypothesized that there is substantial diffusion of hafnium and zirconium atoms during the ferroelectric phase anneal to the underlying silicon substrate, disrupting the inter-facial bonds or forming defective silicates. This observation is in light of numerous trap neutralization anneals developed for Si/SiO2 at temperatures comparable to the ferroelectric phase anneal discussed here, whereby the interface trap density consistently decreases [16], [17]. We suspect that the nitrided interface provides a strong barrier against Hf/Zr diffusion during high-temperature post-processing steps. This hypoth-esis is motivated by the well-known incorporation of nitrided oxides in highly scaled gate dielectrics in order to prevent boron diffusion to the channel silicon from the p+ polysil-icon gate [18]–[20]. To establish this hypothesis, however, a detailed SIMS study will be necessary.

The HZO capacitor with nitrided SiO2 is thus cho-sen for further study to understand the interface trapping characteristics. The dynamic filling and emptying of trap states located at the interface between silicon and nitrided SiO2 is characterized using the frequency-dependent AC conductance method [12]. As trap states often occupy particular energy lev-els within the bandgap, they can be characterized by changing the surface potential of the semiconductor through an applied gate voltage. When the silicon substrate is depleted, fast traps located at the interface modulate the measured capacitance and conductance values as a function of frequency [21]. Thus, we can obtain information about the trap density and time response from CV and GV (conductance-voltage) measure-ments on MOSCAPs.

Peaks in the GV curves, shown in Fig. 3, indicate a response due to interface trapping. The peak midgap conductance values, seen near an applied voltage of 0V, increases as the measurement frequency increases from 1 – 100 kHz. Moreover, by reinterpreting the measured capacitance and



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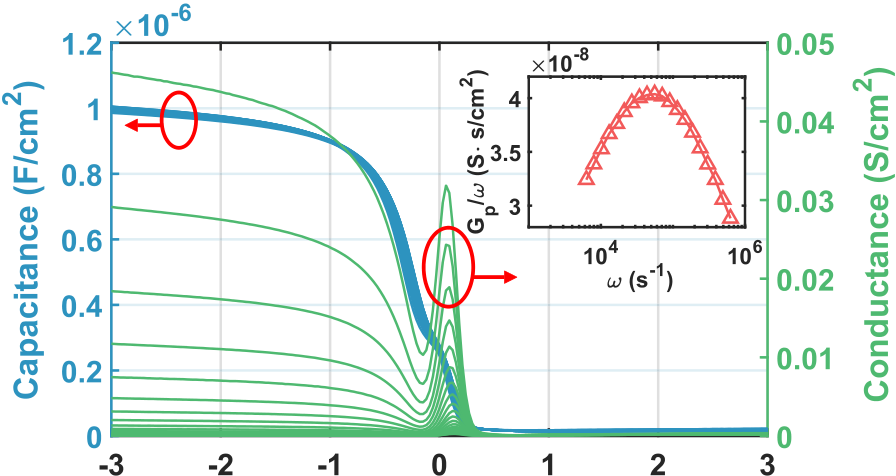




Fig. 3. Direct measurement of Dit on a MOSCAP with nitrided SiO2. CV/GV curves, from 1 – 100 kHz, indicate minimal frequency dispersion. Inset shows a normalized conductance vs. frequency curve for Dit extraction.

conductance data as a function of frequency, the midgap interface trap density can be extracted [12], [21]. A rep-resentative normalized conductance curve is plotted versus frequency (*G P/ω* vs. *ω*) in the inset of Fig. 3.

The normalized conductance here is calculated as: *G P(ω)*  *ωCoxGm*

where *Cm* and *Gm* are the measured capacitance and conduc-



*ω*  =



*G*2*m* + *ω*2*(Cox* − *Cm)*2   
 (1)

tance data, respectively.

Utilizing the equivalent circuit model for a MOSCAP as discussed in [12], we note that at the peak *G P/ω* value, *Dit* can be extracted with the relation:   
 *Dit* =2*.*5 · *G P(ω*max*)/ω*  (2)

where *q* is electronic charge, and *ω*max is the frequency at which the maximum conductance value occurs. Using this relationship, we extract the maximum *Dit* in depletion for the capacitor with nitrided SiO2 after the phase anneal as roughly 6 × 1011cm−2eV−1. In comparison, the maximum midgap *Dit* of the chemical oxide or SiO2 interlayer is 2*.*9×1012cm−2eV−1and 2*.*3×1012cm−2eV−1, respectively. Finally, a CV model to capture the influence of interface trapping is presented. The “ideal” flatband voltage of the MOSCAP, sans the effect of interface traps, is extracted from a single high frequency CV (one taken at 1 MHz). Then, a flatband capacitance is calculated based on the Debye length, and a flatband voltage (*VFB*) is also assigned. In the device analyzed, *VFB* is determined to be −0*.*201V. The oxide capacitance, *Cox*, is defined as the combined capacitance of the interfacial oxide and the HZO film, and is determined experi-mentally as the measured capacitance in strong accumulation. A model CV based on standard MOSCAP theory is then constructed with and without the effect of interface traps. To the first order, the presence of *Dit* manifests itself as an additional *Cit* in the circuit model proposed by [12]. One can calculate an approximate distribution of *Dit* across a portion of the silicon bandgap, roughly from the valence band to midgap:

*Cit* = *Cp* − *Cs*   
*Cp* =�

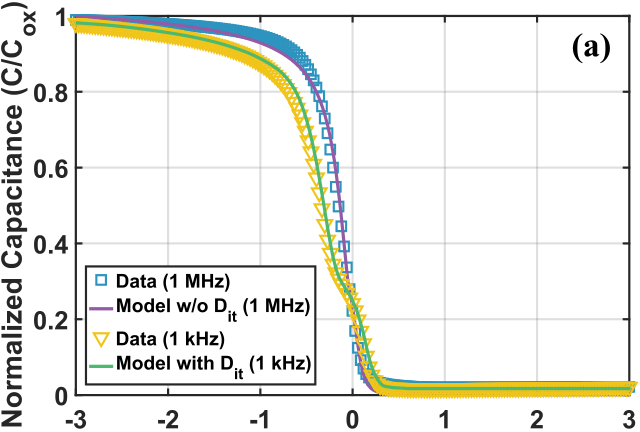
*Cmeas*−



*Cox*�−1 (3)

(4) 1 1

where *Cp* captures the capacitance contribution from silicon depletion and interface trapping, and *Cit* subtracts off *Cs*, the expected depletion capacitance. *Cs* is determined, from





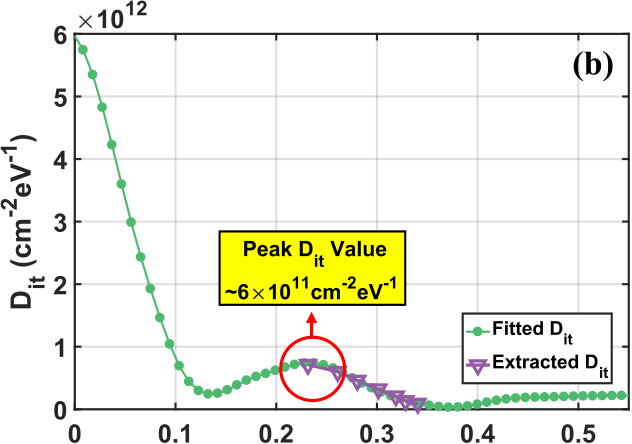




Fig. 4. A model CV and Dit distribution can be fitted from the experimental VFB, Cox, and Na. (a) Calculated and measured CV’s at 1 kHz and 1 MHz. (b) Comparison of fitted *Dit* for CV model and measured Dit with AC conductance.

standard CV calculations, as the differential change in the semiconductor charge as the surface potential is stepped.

Fig. 4a contains fitted CV’s, both with and without an assumed *Dit* distribution, based on experimental data taken at 1 kHz and 1 MHz. Fig. 4b shows *Dit* versus the occu-pational energy of the traps in the silicon bandgap for the *Dit* data extracted using the AC conductance method and the fitted *Dit* used in the 1 kHz CV model. The depletion-regime *Dit* from the fitted distribution agrees well with the *Dit* extraction.

Lastly, we note a small peak in the *Dit* distribution around 200 mV from the valence band edge. This manifests in the 1 kHz CV in Fig. 4a as a characteristic “shoulder” in depletion. The cause of this peak are traps which have a specific origin and location relative to the interface, which could be due to *Pb* centers [22], [23], but also could result from residual Hf/Zr atoms reaching the silicon interface during the phase anneal.

IV. CONCLUSION

In conclusion, the nature of the interface states of the ferroelectric HZO/Si material system has been investigated in detail. Various interfacial oxides, crucial for obtaining a good interface between HZO and silicon, were analyzed for integrity after the phase anneal. It is shown, using the AC conductance method, that a nitrided SiO2 interfacial layer provides the lowest midgap trap density and furthermore can withstand the high-temperature phase anneal by acting as a barrier against dopant diffusion. Finally, a CV model and experimental CV data were used to calculate the *Dit* distribution, which has a narrow energy peak close to the valence band. Subsequent studies will focus on optimizing the nitrided SiO2 for an improved trap distribution.

ACKNOWLEDGMENT

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| The | authors | would | like | to | thank | Hong | Zhou | and |

Justin C. Wong for fruitful discussions.

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