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Self-Aligned, Gate Last, FDSOI, Ferroelectric

Gate Memory Device With 5.5-nm Hf0.8Zr0.2O2,

High Endurance and Breakdown Recovery

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***Abstract— We demonstrate a nonvolatile single transis-tor ferroelectric gate memory device with ultra-thin (5.5 nm) Hf0.8Zr0.2O2 (HZO) fabricated using a self-aligned gate last process. The FETs are fabricated using silicon-on-insulator wafers, and the ferroelectric is deposited with atomic layer deposition. The reported devices have an ON/OFF drain cur-rent ratio of up to 106, a read endurance of > 1010read cycles, and a program/erase endurance of 107cycles. Fur-thermore, healing of the transistorafter gate insulatorbreak-down is demonstrated.***

***Index Terms— Ferroelectric, hafnium zirconium oxide, gate last, memory, silicon-on-insulator.***

I. INTRODUCTION   
**N** attractive due to their potential for single transistor ONVOLATILE ferroelectric gate memory devices are

operation and non-destructive, fast read operation [1], [2]. The

memory element in these devices consists of a ferroelectric in the gate stack rather than the usual dielectric. Then, switching the polarization of the film by applying a gate voltage pulse induces a shift of the threshold voltage according to the final orientation of the polarization. This, in turn, results in a large

change in channel conductance at zero gate bias.

Recently, doped HfO2 was found to be ferroelectric in the orthorhombic phase [3]. The remanent polarization and

the coercive field of these films are tunable with doping concentration, annealing conditions, and capping layer [2].

Importantly, HfO2 is CMOS process compatible [4]. How-ever, to be amenable for integration with ultra-short channel transistors, it is imperative to explore memory operation in

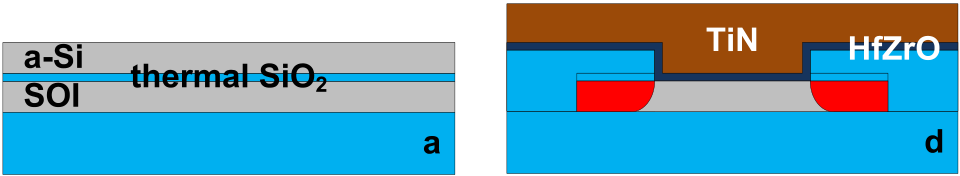
Manuscript received August 15, 2017; accepted August 27, 2017. Date of publication September 4, 2017; date of current version September 25, 2017. This work was supported by the Berkeley Center for Negative Capacitance Transistors. The review of this letter was arranged by Editor C. V. Mouli. (Korok Chatterjee and Sangwan Kim contributed equally to this work.) (Corresponding author: Korok Chatterjee.)   
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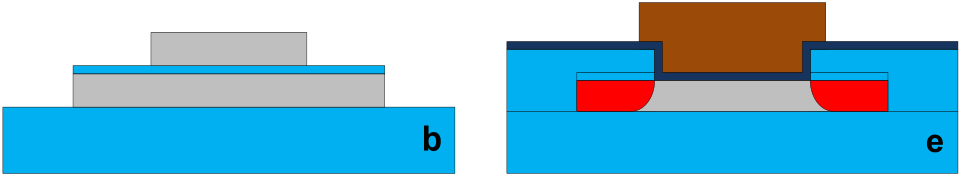
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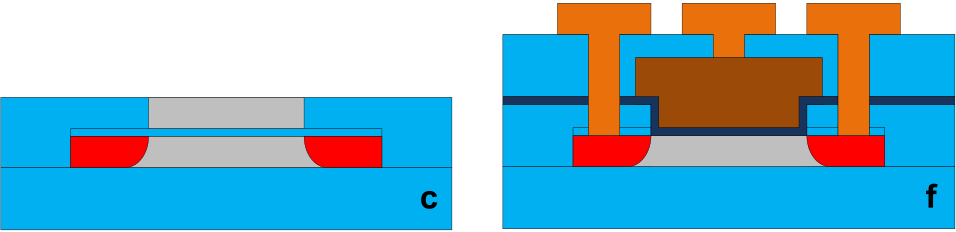


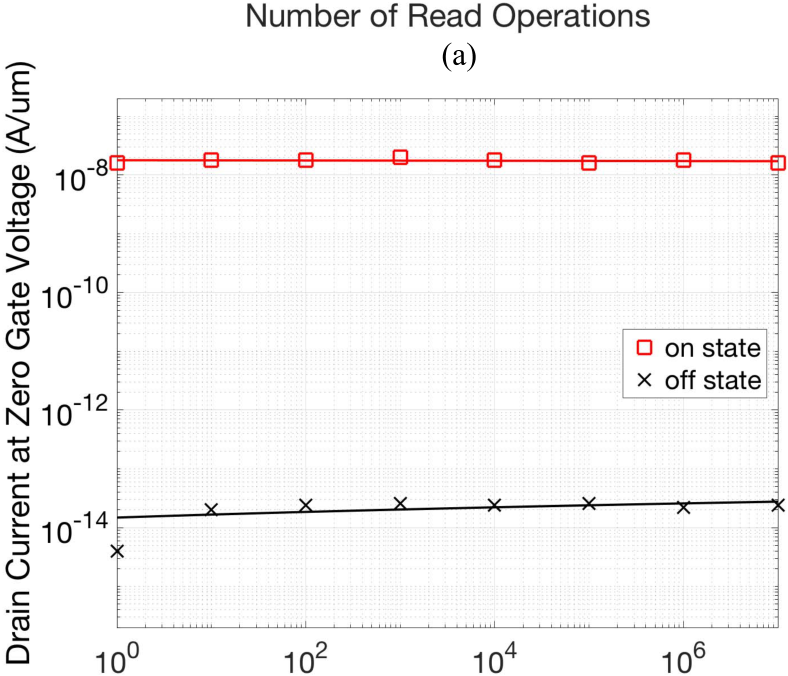
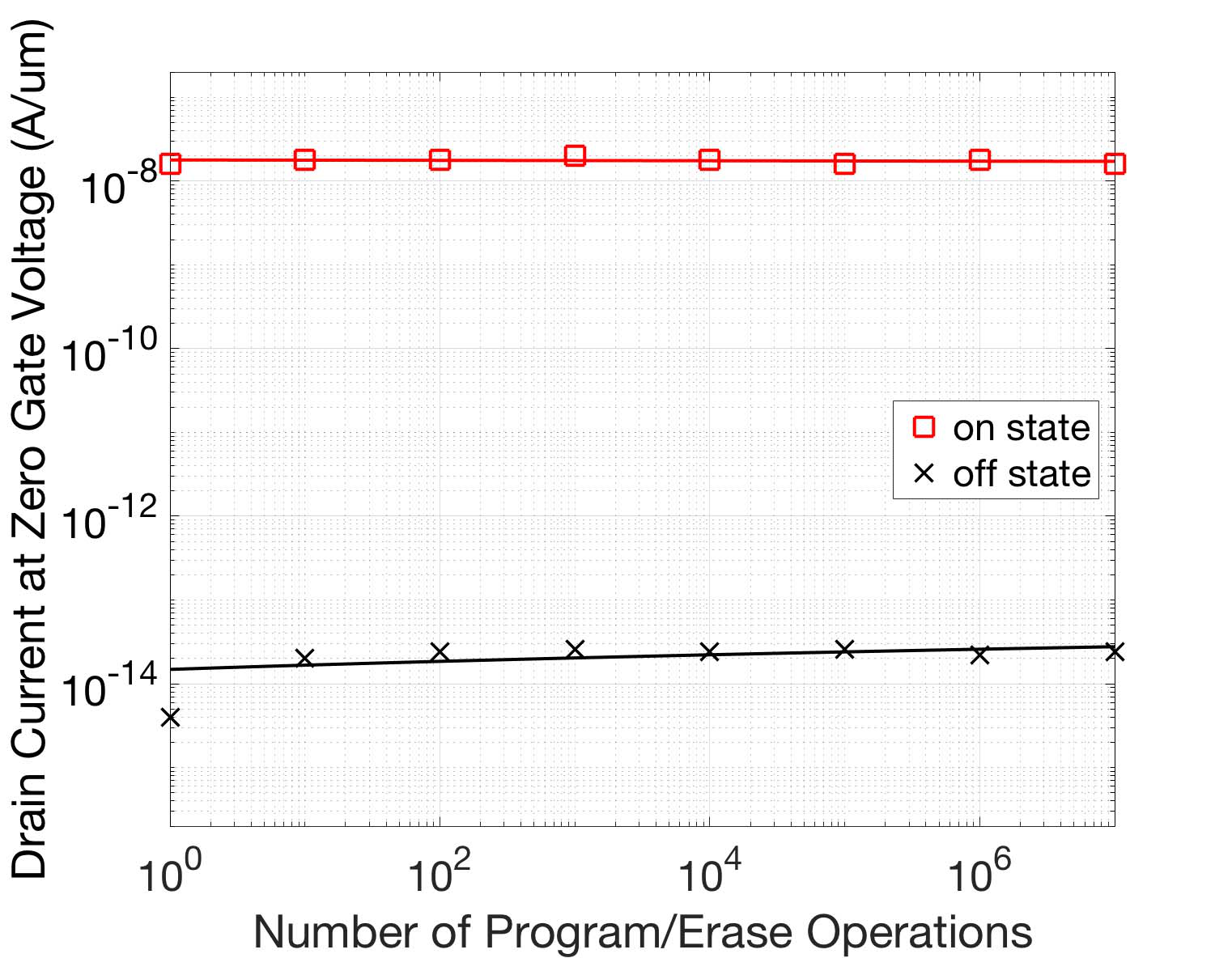
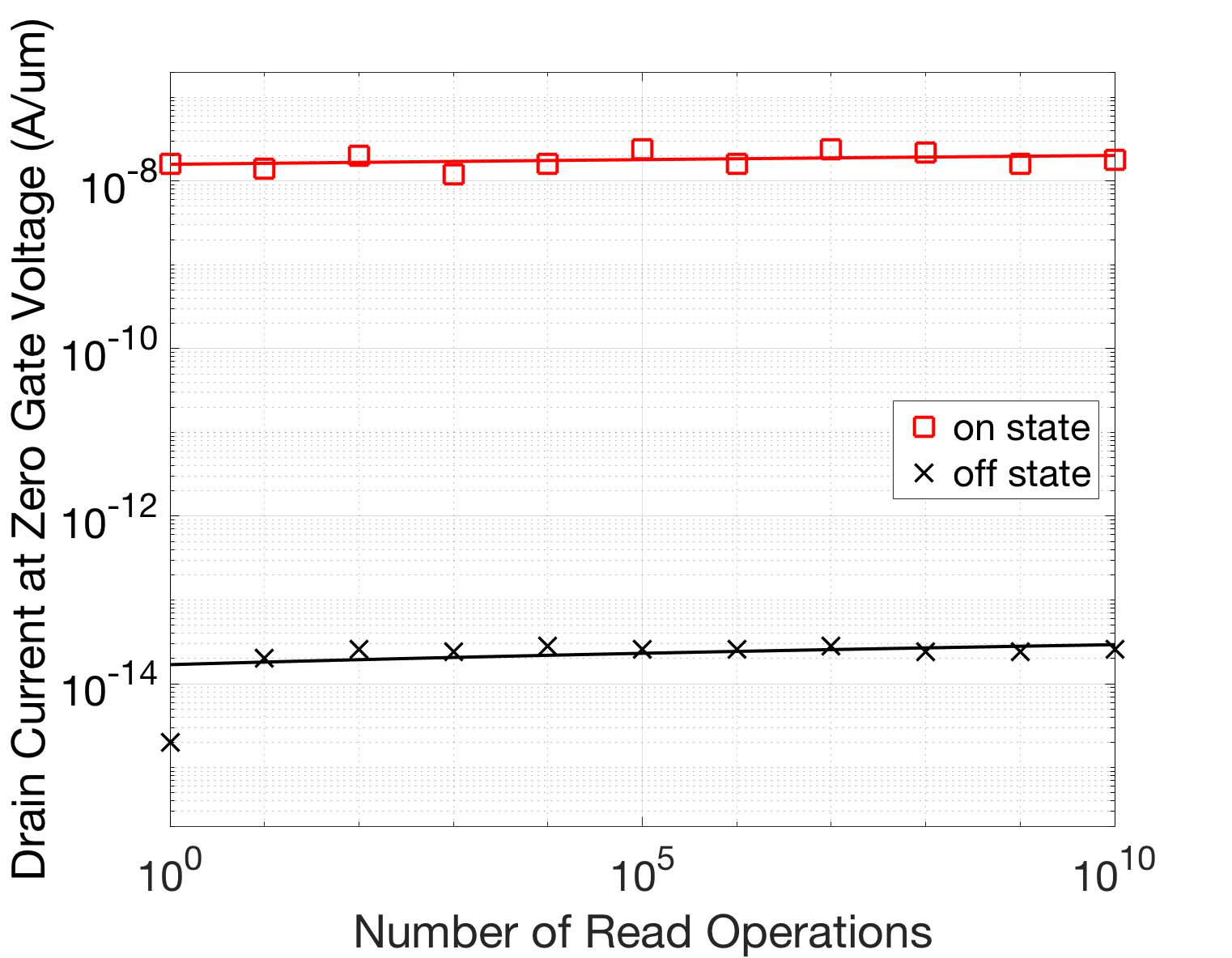
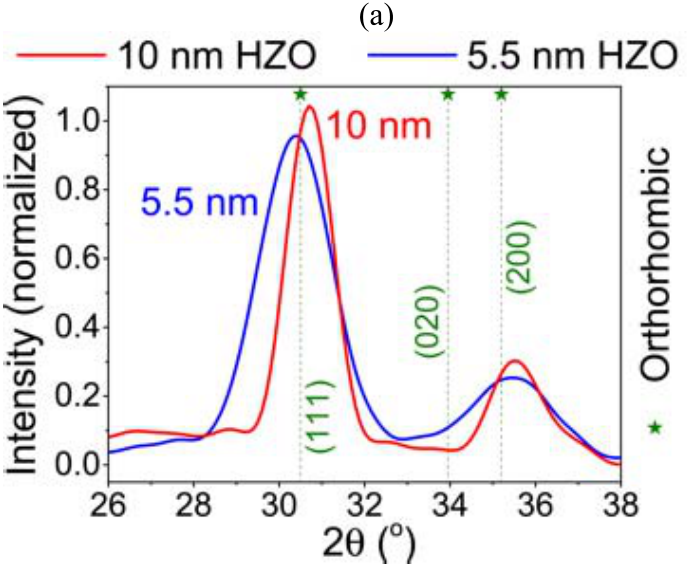
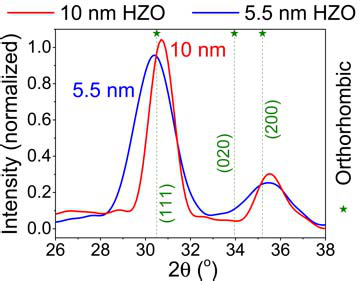
Fig. 1. Process flow for the FET. (a) 12 nm thermal SiO2 and 150 nm a-Si sacrificial gate were deposited. (b) Active area was patterned and etched down to buried oxide (BOX) which was followed by dummy gate pattern-ing. (c) After As ion implantation, CVD oxide was deposited and CMP. (d) Sacrificial gate is removed. Real gate consisting of SiO2, HZO, and TiN are deposited with ALD and sputtering, respectively. (e) Gate patterning. (f) ILD deposition, contact hole formation and metallization.

ferroelectric gate devices with thin ferroelectric layers. This provided our motivation to explore single transistor memory devices with a scaling-compatible ferroelectric layer. Because the ferroelectric properties depend strongly on annealing con-ditions, we opted to use a gate last process to minimize the number of thermal steps after gate deposition. Here we demonstrate, for the first time, such a memory device with 5.5 nm Hf0*.*8Zr0*.*2O2 layer.

II. DEVICE FABRICATION

The n-type transistors shown in figs. 1 and 2a are fabricated using a self-aligned, replacement gate process [5], [6] on SOI. After thinning the device layer to 30 nm, the sacrificial layer consisting of 12 nm thermal SiO2 and 150 nm polycrys-talline Si is deposited using chemical vapor deposition (CVD) (fig. 1a). Next, the active region is defined, and exposed regions are etched down to the buried oxide. The gate is then patterned and ion implantation is performed on the exposed source/drain areas (fig. 1b). Following dopant activation, low temperature SiO2 is deposited. Chemical mechanical polish-ing (CMP) removes the SiO2 on top of the gate, exposing the sacrificial stack (fig. 1c), which is removed by reactive ion etching (RIE) and diluted hydrofluoric acid.

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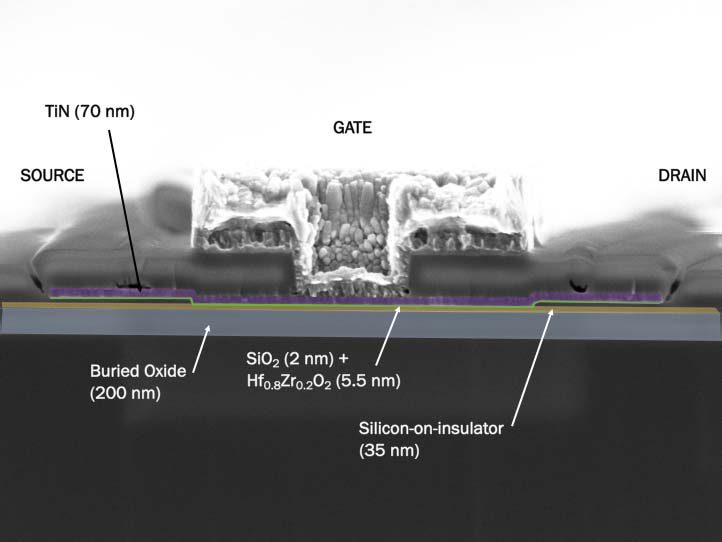




Fig. 2. (a) Cross-sectional SEM image of the fabricated FET with false color indicating the buried oxide (BOX) in blue, silicon-on-insulator (SOI) in orange, interfacial SiO2 and HZO in green, and TiN in purple. (b) X-Ray diffraction measurement at 0.35° of 5.5 nm and 10 nm films of HZO indicating orthorhombic phase.

The gate stack is fabricated by formation of a 2 nm SiO2 in a rapid thermal anneal (RTA) chamber followed by 5.5 nm of Hf0*.*8Zr0*.*2O2 by ALD (fig. 1d). The thick SiO2 is due to ramp rate limitations of the RTA. The deposition cycle consists of 4 cycles of HfO2 followed by 1 cycle of ZrO2. This is repeated 11 times to yield a 5.5 nm film. Its composition is chosen to yield slightly below maximum remanent polarization, and is characterized in [7]. Subsequently, TiN is sputtered and an RTA at 500 °C for 30 sec in N2 ambient is performed to form the orthorhombic phase in Hf0*.*8Zr0*.*2O2 [2]. Grazing incidence X-ray diffraction is performed at a grazing incidence of 0.35°to confirm the phase of the Hf0*.*8Zr0*.*2O2 and is depicted in fig. 2b.

After the final gate patterning of fig. 1e, 400 nm of SiO2 is deposited using a plasma enhanced CVD at 200 °C as an interlayer dielectric, and finally the metal contacts of sputtered TiN/Ti/Al are defined with via etching in the oxide, sputtering, lithography, and RIE metal etching (fig. 1f). Devices reported here have a channel length of 1 *µ*m and a width of 50 *µ*m. A scanning electron microscope (SEM) micrograph of the finished device with false color showing the various device layers is shown in fig. 2a.

III. DEVICE CHARACTERIZATION

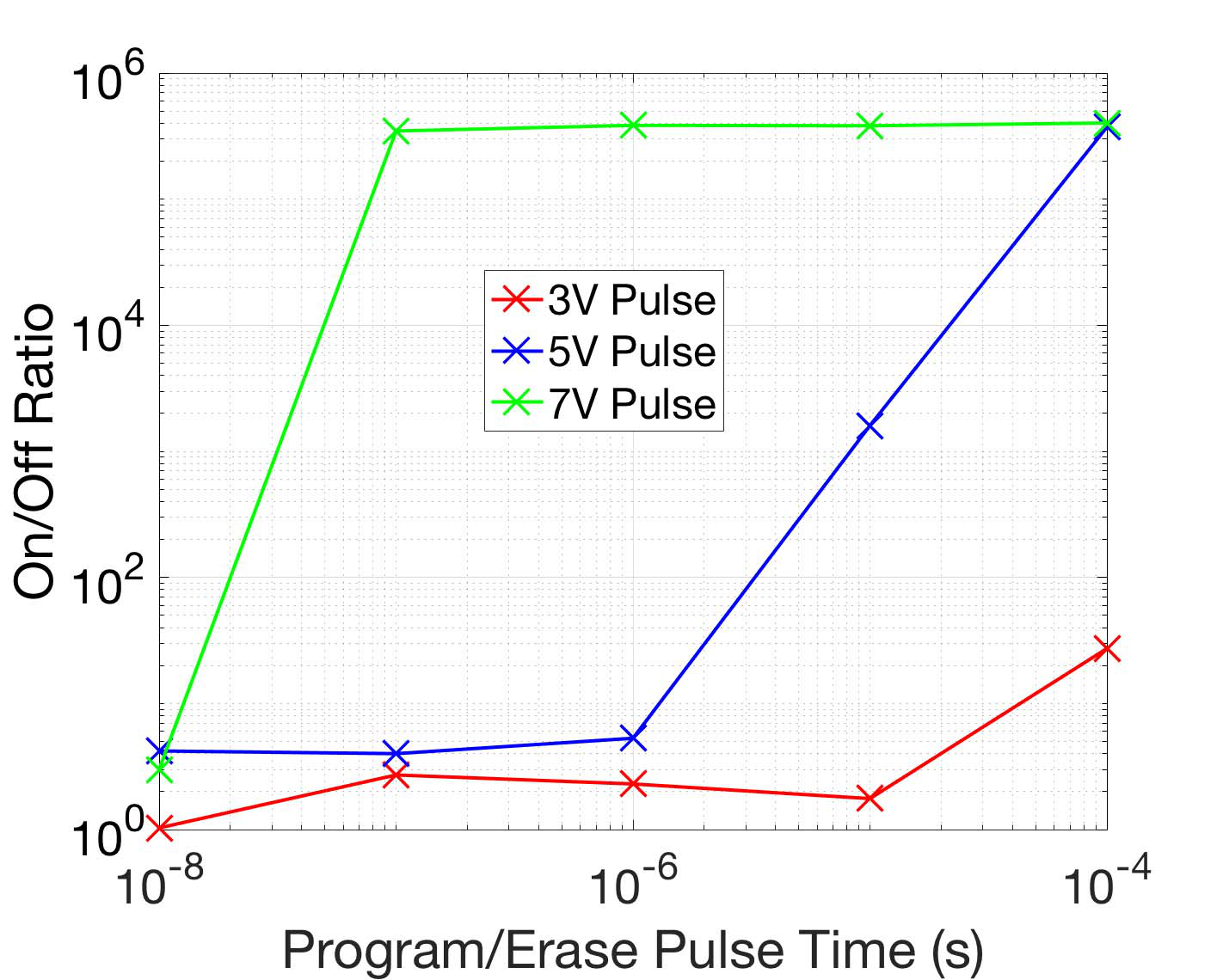
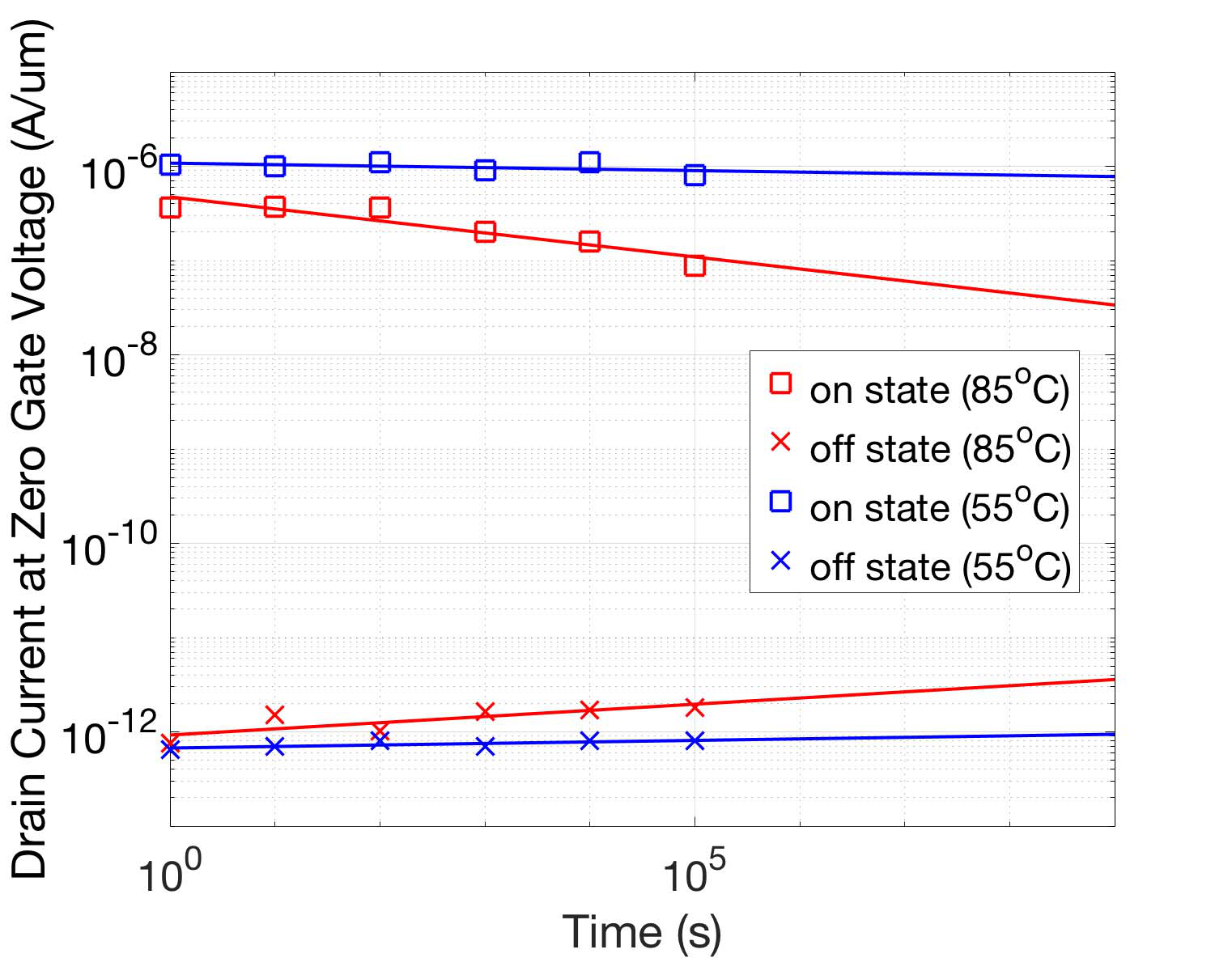
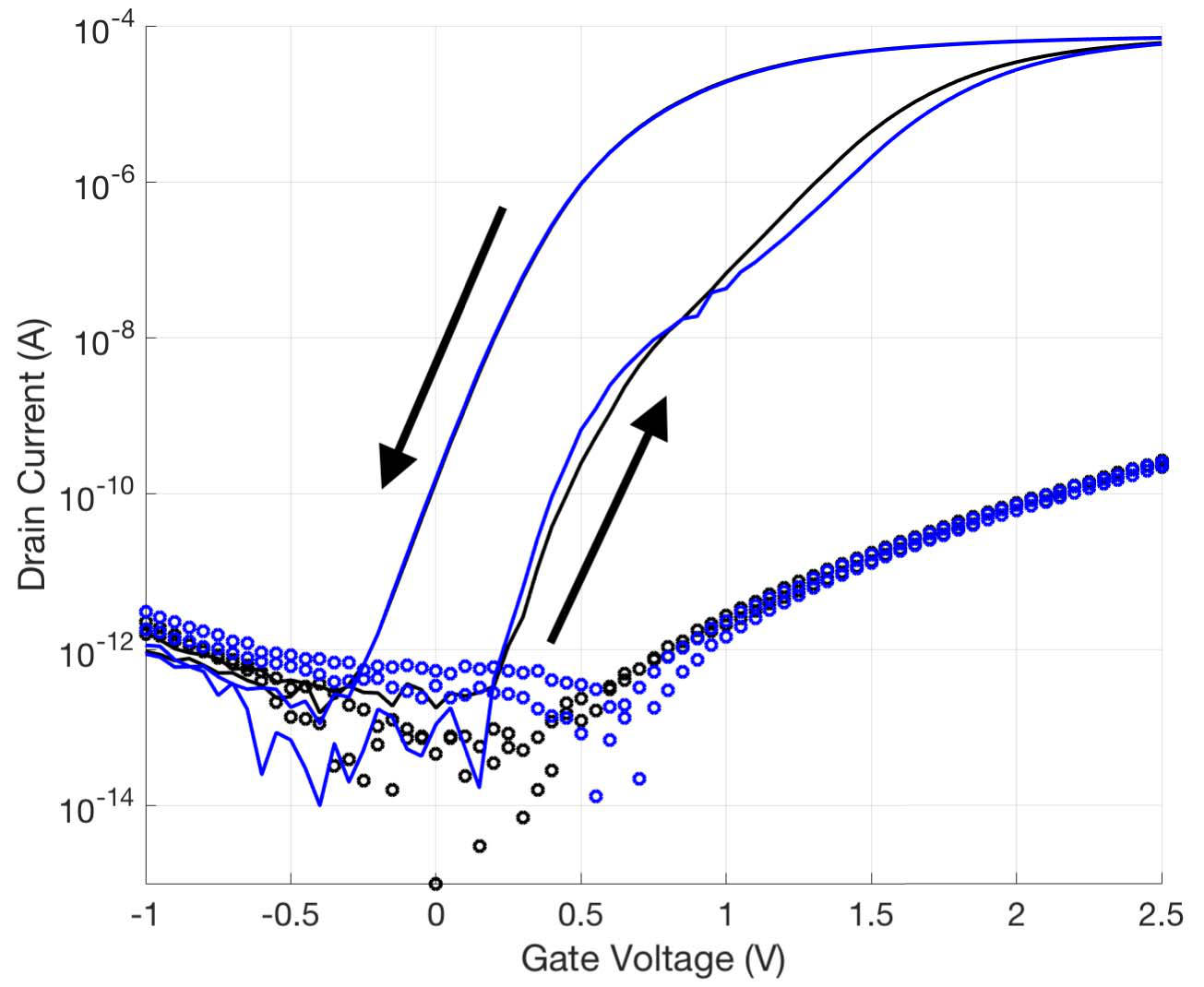
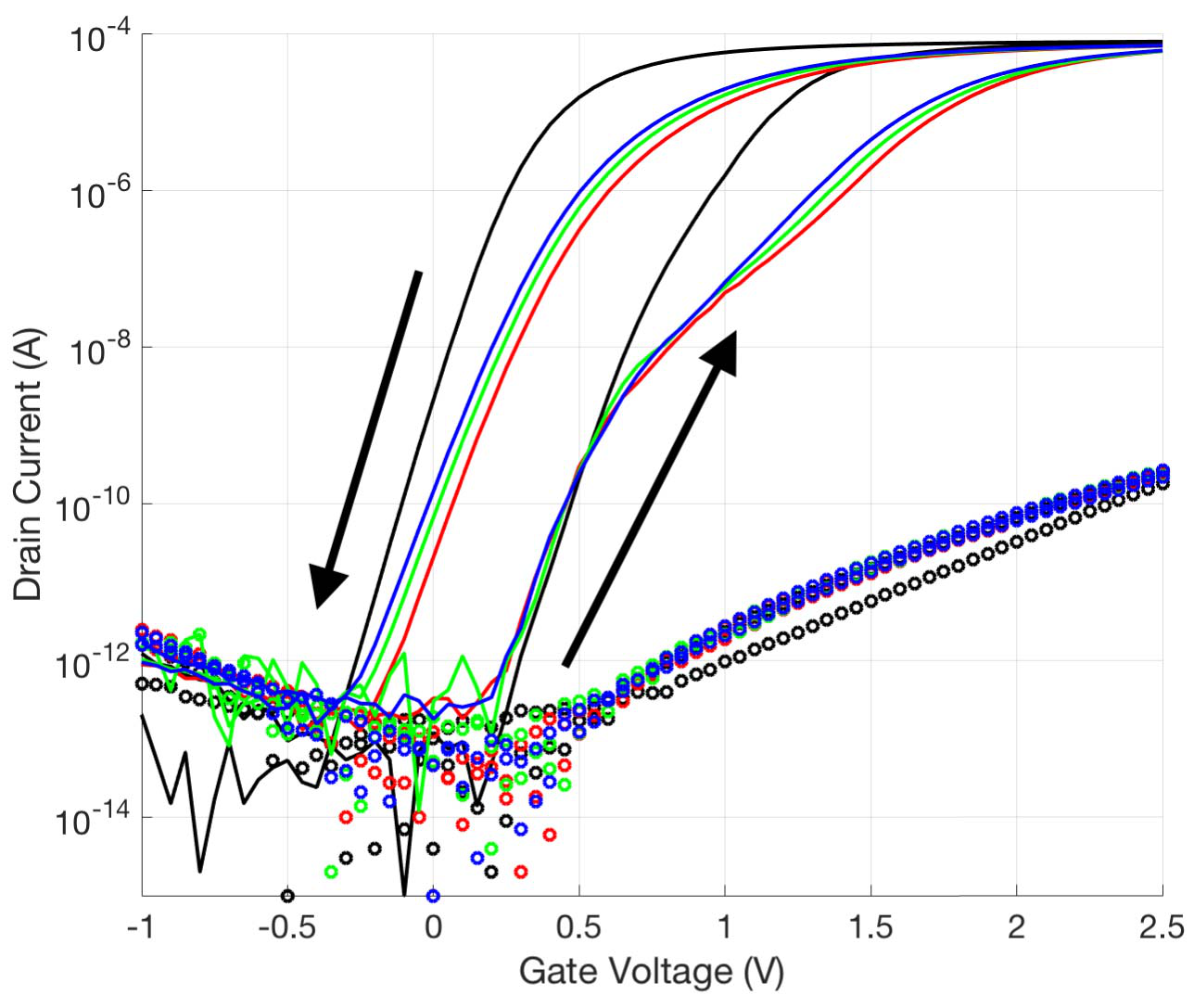
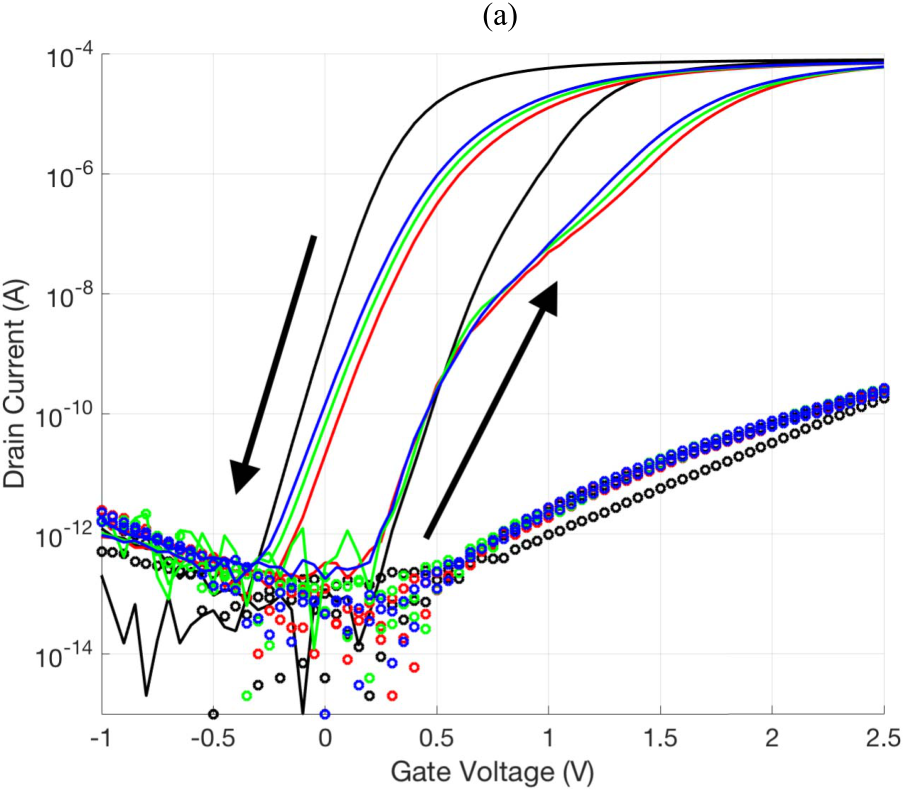
Device characteristics are obtained with a Keysight B1500A semiconductor device analyzer. Pulses for endurance mea-surements are applied with a Keysight 81150A Waveform



Fig. 3. (a) ID (at VGS = 0 and VDS = 50 mV) for the “on” and “off” states as a function of the number of read operations. (b) ID (at VGS = 0 and VDS = 50 mV) for the “on” and “off” states as a function of the number of P/E operations.

Generator. 100 mV drain voltage is used to read the drain current (*ID)* at 0 V gate voltage (*V*GS*)*. *ID* remains stable over *>* 1010read operations (Fig. 3a). Program/erase (P/E) operations consist of 100 *µ*s pulses of +/- 5 V at the gate, which switch the polarization of the ferroelectric. Based on Fig. 3b, *I*D*,*ON and *I*D*,*OFF values remain stable over 107cycles of P/E. In addition, there is negligible change in transfer characteristics after 107P/E cycles, as shown in Fig. 4a. Charge trapping is found to originate from the channel, opposing the ferroelectric hysteresis. This is inferred from the reduction of *I*ON/*I*OFF when DC sweeps are used instead of pulses, and from the clockwise hysteresis in small sweeps. Values in Fig. 3 are obtained from small sweeps near VGS = 0 V to read the drain current. Breakdown of the devices happens typically beyond 107cycles. Remarkably, however, the devices can recover after a few hours of rest. Fig. 4b shows the recovery of the gate oxide 24 hours after breakdown.

Such recovery from breakdown indicates soft breakdown of the oxide layers. We hypothesize that repeated switching of the ferroelectric oxide breaks down the interfacial SiO2 due to large electric fields and the recovery may be due to charge trapping in HZO at the localized soft breakdown spot. Breakdown recovery may have significant practical benefit in increasing the endurance cycle at which the number of



CHATTERJEE et al.: SELF-ALIGNED, GATE LAST, FDSOI, FERROELECTRIC GATE MEMORY DEVICE 1381



Fig. 6. ION/IOFF as a function of program/erase pulse time for pulse   
amplitudes of 3 V (red), 5 V (blue), and 7 V (green).

Retention is also measured for 0 V *V*GS and 50 mV drain   
voltage (*V*DS*)* bias at both 55 °C and 85 °C by applying a   
+*/*− 5 V pulse at the gate to program the memory and periodically measuring the drain current at *VG* Retention is measured for up to 105sec and extrapolated to = 0 V.

109sec (Fig. 5). Some reduction in the ON-OFF current ratio   
(*I*ON/*I*OFF*)* can be seen at 85 °C, though the ratio remains   
above 104at 10 years.

Finally, we examine the dependence of the memory on pro-  
gram/erase voltage and duration. Fig. 6 shows how *I*ON/*I*OFF   
increases as the P/E voltage and pulse width are increased.

IV. CONCLUSIONS

In summary, we have demonstrated robust memory opera-  
tion in a self-aligned, gate last, fully-depleted SOI (FDSOI)   
transistor with 5.5 nm ferroelectric Hf0*.*8Zr0*.*2O2 as a gate   
insulator. A sacrificial gate was used to minimize the thermal

 budget of the ferroelectric film, which was deposited as a

Fig. 4. (a) Comparison of transfer characteristics before (black) and after (blue) application of 107P/E operations with 50 mV-VDS. (b) Comparison of transfer characteristics before and after (blue) breakdown recovery. The variation of subthreshold slope is likely due to the nonlinearity of ferroelectric capacitance. The red, green, and blue curves (right to left) depict the first, second, and third sweeps after breakdown recovery, respectively.

Fig. 5. Retention of ID (at VGS = 0V and VDS = 50 mV) as a function of time at 85 °C and 55 °C. Solid lines represent extrapolation of experimental data.

defective bits exceeds the limit that the error correction circuit

replacement gate. In general, ferroelectric characteristics tend to disappear below a critical thickness. In hafnium oxide based ferroelectrics, ferroelectricity remains down to the sub-10 nm range. However, this results in a high electric field across the gate stack, making high P/E endurance challenging. It is worth noting that these devices are operated purely as memory elements, despite using similar ferroelectric films as proposed negative capacitance FETs [8]. The novelty in our work is in the use of thinnest ferroelectric (5.5 nm) to date [9]–[14] and the gate last process.

Our devices show endurance of ∼ 107cycles and large

cycling breakdown, a recovery is possible after a few hours *I*ON/*I*OFF at *V*GS = 0 V. We also show that following the

of non-operation. This provides insight into the breakdown mechanism. Optimization of the interfacial characteristics is expected to improve subthreshold slope, increase the mem-ory window and *I*ON/*I*OFF ratio by reducing defect state-induced clockwise hysteresis, which opposes the ferroelectric hysteresis. As breakdown in HZO thin films is thought to be an interfacial phenomenon [15], the P/E endurance should increase as well. The observed robust operation, even in the absence of interface engineering, with 5.5 nm-thick dielectric indicates that such memory devices should be scalable to ultra-

is designed to detect and correct. small channel lengths.

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