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A Study of Endurance Issues in HfO2-Based

Ferroelectric Field Effect Transistors: Charge

Trapping and Trap Generation

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***Abstract— Recent***  ***demonstration***  ***of***  ***aggressively scaled HfO2-based ferroelectric field effect transistors (FE-HfO2-FETs) has illustrated a pathway to fabricate FeFETs that enjoy COMS-compatibility, low power, fast switching speed, scalability, and long retention. One potential issue of this promising technology is its limited endurance, which has been attributed to the degradation of gate stack before the fatigue of polarization in the ferroelectric***  ***HfO2***  ***layer.***  ***Some***  ***associated***  ***work***  ***has identified charge trapping and trap generation as key villains, but a clear understanding of two aforementioned underlining mechanisms is still missing. In this letter, we initiated this letter to investigate the roles of charge trapping and trap generation in causing endurance failure of FE-HfO2 FETs.***

***Index Terms— HfO2-based FeFETs, endurance, charge trapping, trap generation.***

I. INTRODUCTION   
**T** commercialization of FErrolelectric Dynamic Random HE lack of suitable ferroelectric materials has impeded

Access Memory (FEDRAM) for over one decade [1]. The

recent demonstration of HfO2 based field effect transistors (FE-HfO2 FETs) using 28nm technology has shown the pos-sibility of fabricating aggressively scaled FeFETs that are

CMOS compatible, and offer attractive features such as low

power, fast switching speed, and scalability [2]. In addition,

both experimental and theoretical studies have indicated that

aggressively scaled FE-HfO2 FETs are able to possess 10-year extrapolated retention time, making it a suitable non-volatile

memory (NVM) candidate [2], [3]. On the other hand, limited

endurance performance of FE-HfO2 FETs requires a clear understanding of its root cause to develop a strategy of

improvement. Some recent work in this field has indicated that

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| the endurance failure is due to the degradation of gate stack |

before fatigue of polarization in the HfO2 ferroelectric layer

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| set in, and identified charge trapping and trap generation as |

primarily causes for the endurance failure [4], [6]. We believe a clear understanding of the roles of these two aforementioned underlining mechanisms is needed to find possible strategies for enhancing the endurance.

In this letter, we will investigate the roles of charge trap-ping and trap generation during the endurance test of a FE-HfO2FET. The underlying mechanisms and associated impact on the endurance failure of FE-HfO2 FETs are also discussed.

II. EXPERIMENTAL

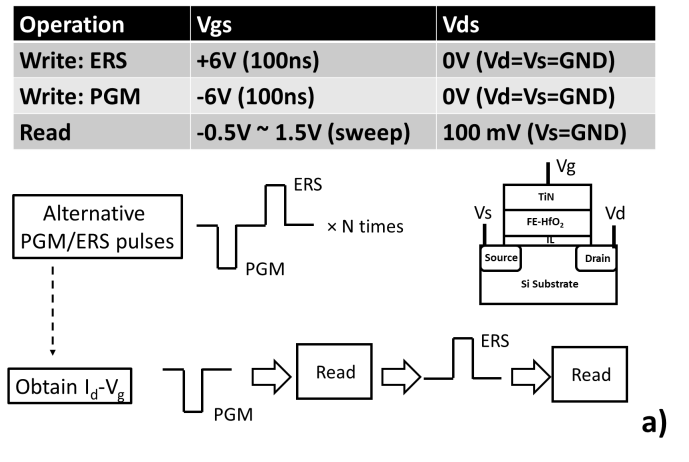
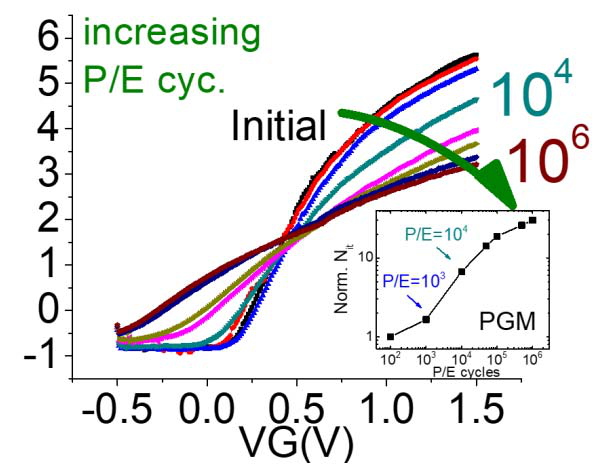
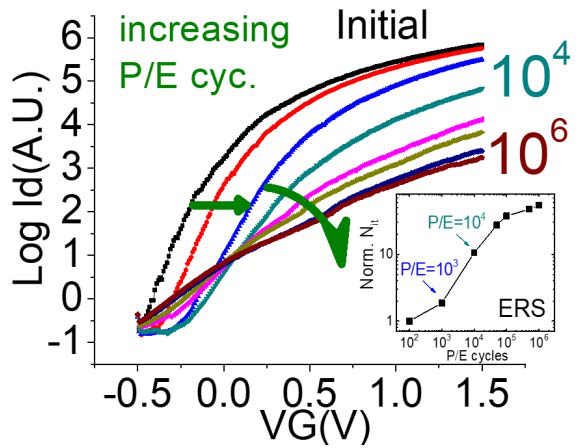
Fabricated by a leading-edge foundry, the FeFETs studied in this paper include gate stack of 8nm TiN, 9nm Si-doped HfO2 (3.8%) and 1.2nm Interfacial layer (IL) on top of Silicon substrate. The endurance measurements on the device-under-test (DUT) are performed using Keithley 4200 Semiconductor Characterization System at room temperature. The operating conditions are listed in Fig. 1.a. Alternating program/erase pulses (−*/*+6V, 100ns) are applied to the DUT, and read operation is immediately performed using Id-Vg sweep. The read condition (Vgs from −0.5V to 1.5V, Vds is set at 100mV) is chosen in order to eliminate disturb to the polarization state in the ferroelectric layer.

III. RESULTS AND DISCUSSION

Typical endurance characteristics of the DUT are shown in Fig. 1.b. The ERS/PGM read current ratio [i.e., the read current after “+” erase pulse (ERS) over the one after “−” program pulse (PGM)] drops from ∼4 orders initially to *<*1 order after 105accumulated PGM/ERS (P/E) cycles, and finally completely diminishes after 106P/E cycles. These endurance results are consistent with previously reported endurance char-acteristics of Si:HfO2-based FeFETs that have similar device parameters [4], [5].

In order to investigate the underlying mechanisms that lead to endurance failure, we looked into the evolution of Id-Vg curves after alternating P/E cycles. As one can see from Fig.2, both significant shift and slope degradation happen as a function of ERS/PGM cycles. In particular, it is worth pointing out that the ERS cycling (Fig.2a) initially gives rise to nearly parallel Vth shift before 103cycles, indicating electron trapping in the gate stack, and the slope starts to degrade after 104cycles, indicating generation of “interface

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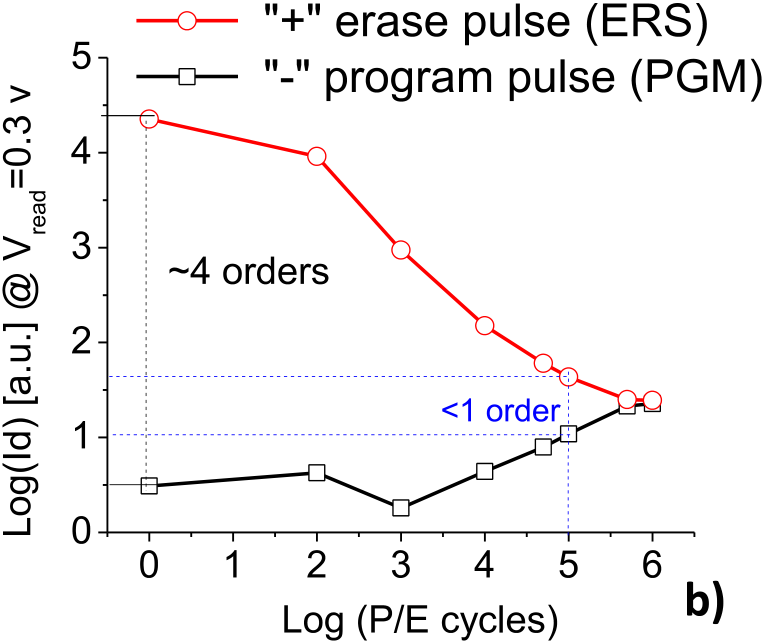


Fig. 1. a) Illustration of device-under-test (DUT) and associated opera-tion conditions during endurance test. Read operation is performed after write (PGM/ERS). b) Typical endurance characteristics of HfO2 based FeFETs. Ion/Ioff in pristine device is about 4 orders, and gradually drops to less than 1 order after 105alternative P/E cycles, and finally memory window vanishes after 106P/E cycles.

traps”, although “interface traps” here should include “border traps” [7] in HfO2 that are influenced by the Si Fermi level during the Id-Vg measurement. In contrast, the PGM cycling (Fig. 2b) causes nearly no Vth shift nor slope change before 103cycles, and after 104cycles significant slope degradation is clearly observed, consistent with generation of “interface traps”. According to [8], subthreshold slope degradation is corelated to generation of “interface traps” as described in the following formula:

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| *S* =*kT* ln*(*10*)* | *Nit ,* | (1) |

whereS is change of subthreshold swing, k is Boltzmann constant, T is absolute temperature, Cox is insulator capaci-tance, and Nit is “interface trap” density. According to Eq. (1), we extracted Nit as a function of P/E cycles (normalized to the value when P/E cycles are 102, insets of Fig.2, a) and b) for ERS and PGM respectively). One could observe significant increase of Nit after 104P/E cycles.

The aforementioned observation tells us that endurance failure in this DUT is caused by both charge trapping and trap generation. Charge trapping may also be affected by the polarity of pulse and polarization in HfO2, and trap

Fig. 2. Id–Vg curves of the DUT during endurance test: a) ERS state (after “+” ERS pulse) shows parallel Vth shift up to 1000 P/E cycles, followed by slope degradation, and b) PGM state (after “−” PGM pulses) shows slope degradation. Both a) and b) have inset to depict normalized Nit v.s. P/E cycles, which are calculated according to Eq.(1).

generation contributes significantly after certain P/E cycles (in this specific test, the critical P/E cycles appeared to be 104*)*. To understand the underlying reason, we use the band diagram drawing tool [9] to plot band diagram of the system under write pulse conditions (ERS, and PGM). It is worth pointing out that the band diagram corresponds to the case that polarization is already reversed under the write pulse. The reason is that typical polarization switching time in a FE-HfO2 is much shorter than the 100ns that we used in endurance test [10]. As such, DUT after polarization reversal would be the one that causes severe charge trapping and trap generation. From Fig. 3.a, it could be observed that during the +6v/100ns ERS pulse (Fig.3a), electrons tunnel through the IL layer and enter the HfO2 region where they start to lose energy and some of them may get trapped; the lost energy could be used to generate border traps near the HfO2/IL interface. On the other hand, during the -6v/100ns PGM pulse (Fig.3b), electrons flow through HfO2 either by Fowler-Nordheim (FN) tunneling or by trap-assisted conduction, and remain “hot” upon entering the Si interface, where some may cause generation of interface traps while losing energy.

It should be mentioned that, because of the large coer-cive field (Ec, ∼1MV/cm [3], [6]) of the FE-HfO2, one

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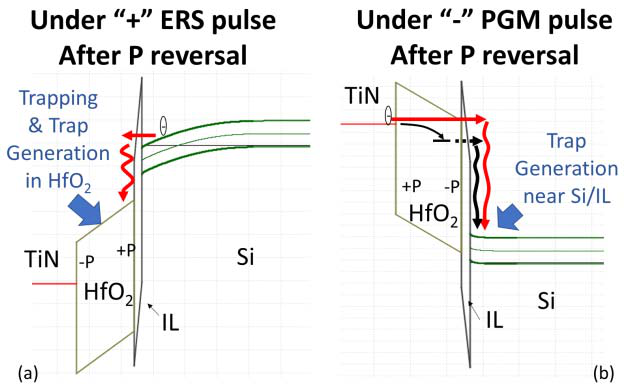


Fig. 3. Band diagrams [using ref.9] under ±- 6v, 100ns ERS/PGM pulses: a) + “ERS” pulse tends to cause charge trapping and generation of border traps in HfO2 near the IL layer, and b)− “PGM” pulse tends to cause more interface trap generation at the IL/Si interface.

must use sufficiently large ERS/PGM voltages to switch the FeFET, which induces very high electric field in the IL due to dielectric constant difference between FE-HfO2 and IL. In addition, the ferroelectricity in HfO2 could also enhance the electric field in IL compared with the case that HfO2 is non-ferroelectric [6]. Such high electric field forces the thin IL into the FN tunneling regime that leads to injection of “hot” electrons that in turn cause severe charge trapping and generation of traps, depending on the pulse polarity.

For fair comparison, in this work we just choose to compare the Id-Vg curves from ERS (PGM) states, although it is worth pointing out that here the ERS/PGM pulses are alternately applied to the DUT before each read operation, and it should be emphasized that the degradation is not only due to each individual ERS (PGM) pulse but due to the interaction between ERS and PGM pulses. From what was reported in Ref. 4,

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| one can clearly see that unipolar stress (i.e., only apply |

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| PGM or ERS pulse) does not cause severe damage to the |

FeFETs, but alternating ERS/PGM pulses (i.e., bipolar stress), cause significant endurance failure [4]. In other words, in our endurance test, the damage to the DUT is largely due to the interaction between alternating ERS and PGM pulses, as is shown in Fig.1.

It is also worth pointing out that the generated traps during the endurance test will diminish both the memory window and the retention time. Retention time in a FeFET is affected by the leakage followed by trapping, which is more severe if the trap concentration is higher [1], [3]. As a result, the increased trap concentration during the endurance test suggests faster retention loss. Similar observation has already been reported in Ref. 12, which clearly shows that the retention characteristic in a HfO2 based FeFET will be adversely affected after the endurance test [12].

From the reliability point of view, both charge trapping and generation of interface traps (including border traps) contribute to endurance failure of the DUT. As is shown in Fig. 4, one can clearly see that charge trapping induced parallel Vth shift and trap generation induced slope degradation will both contribute to diminished ratio of the read current. The memory window

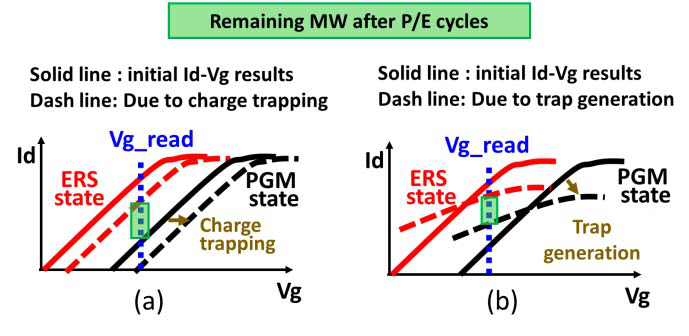


Fig. 4. Two contributions to the drop of memory window: a) Charge trapping induces Vth shift, which could be recovered after detrapping, and b) generation of interface/border traps induce slope degradation. Both mechanisms contribute to degradation of memory window.

reduction due to charge trapping alone may be recovered by de-trapping, while the interface traps (and border traps), once generated, are not reversible by electrical means. Based on this understanding, one would expect that, merely by electrical means (e.g. by use of de-trapping pulse, or increasing delay time between write pulses [11]), one could only alleviate memory window reduction at early stages (e.g. P/E cycles *<*103in this work), but could not fully improve endurance performance after the generation of significant amount of traps. In other words, developing strategies to minimize trap gener-ation would be the best approach for improving endurance performance of HfO2-based FeFETs.

IV. SUMMARY   
 The objective of this work is to understand the endurance failure mechanisms in HfO2-based FeFETs. We have found that the memory window of the device-under-test (DUT) decreases with increased number of program/erase cycles, and vanishes by 106cycles. We have also found that two different mechanisms, charge trapping and generation of interface traps (including border traps), both contribute to the failure, where positive erase pulses tend to cause charge trapping-induced threshold shift up to 103cycles, followed by generation of bor-der traps up to 106cycles, while negative program pulses tend to cause generation of interface traps after 103cycles. Based on our understanding of these two different mechanisms, we would not expect that, merely by electrical de-trapping means, will we adequately improve the endurance performance, due to the irreversible trap generation mechanism, which will dominate later stage of endurance failure (in this work, P/E cycles *>* 104*)*. As such, one needs to develop a strategy to minimize trap generation to improve endurance, which will help the commercialization of HfO2-based FeFET memory technology.

REFERENCES

[1] T. P. Ma and J.-P. Han, “Why is nonvolatile ferroelectric memory field-effect transistor still elusive?” *IEEE Electron Device Lett.*, vol. 23, no. 7, pp. 386–388, Jul. 2002, doi: [10.1109/LED.2002.1015207](http://dx.doi.org/10.1109/LED.2002.1015207).

[2] J. Müller, E. Yurchuk, T. Schlösser, J. Paul, R. Hoffmann, S. Müller, D. Martin, S. Slesazeck, P. Polakowski, J. M. Czernohorsky, K. Seidel, P. Kücher, R. Boschke, M. Trentzsch, K. Gebauer, U. Schröder, and T. Mikolajick, “Ferroelectricity in HfO2 enables nonvolatile data storage in 28 nm HKMG,” in *Proc. IEEE VLSI Technol.*, Jun. 2012, pp. 25–26, doi: [10.1109/VLSIT.2012.6242443](http://dx.doi.org/10.1109/VLSIT.2012.6242443).

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[3] N. Gong and T.-P. Ma, “Why is FE–HfO2 more suitable than PZT or SBT for scaled nonvolatile 1-T memory cell? A retention perspective,”*IEEE Electron Device Lett.*, vol. 37, no. 9, pp. 1123–1126, Sep. 2016, doi: [10.1109/LED.2016.2593627](http://dx.doi.org/10.1109/LED.2016.2593627).

[4] E. Yurchuk, S. Mueller, D. Martin, S. Slesazeck, U. Schroeder,

[7] D. M. Fleetwood, “‘Border traps’ in MOS devices,” *IEEE Trans.*

*Nucl. Sci.*, vol. 39, no. 2, pp. 269–271, Apr. 1992, doi: [10.1109/23. 277495](http://dx.doi.org/10.1109/23.277495).

[8] W. Zhu, “Hafnium oxide and hafnium aluminum oxide for CMOS appli-cations,” Ph.D. dissertation, Dept. Elect. Eng., Yale Univ., New Haven,

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| T. Mikolajick, | J. | Müller, | J. | Paul, | R. | Hoffmann, | J. | Sundqvist, | CT, USA, 2003. |

T. Schlösser, R. Boschke, R. van Bentum, and M. Trentzsch, “Origin of the endurance degradation in the novel HfO2-based 1T ferroelectric non-volatile memories,” in *Proc. IEEE IRPS*, Jun. 2014, pp. 2E.5.1–2E.5.5, doi: [10.1109/IRPS.2014.6860603](http://dx.doi.org/10.1109/IRPS.2014.6860603).

[5] E. Yurchuk, J. Müller, S. Müller, J. Paul, M. Peši´c, R. van Bentum, U. Schroeder, and T. Mikolajick, “Charge-trapping phenomena in HfO2-based FeFET-type nonvolatile memories,” *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3501–3507, Sep. 2016, doi: [10.1109/TED. 2016.2588439](http://dx.doi.org/10.1109/TED.2016.2588439).

[6] J. Müller, P. Polakowski, S. Müller, H. Mulaosmanovic, J. Ocker, T. Mikolajick, S. Slesazeck, S. Müller, J. Ocker, T. Mikolajick, S. Flachowsky, and M. Trentzsch, “High endurance strategies for hafnium oxide based ferroelectric field effect transistor,” in *Proc. IEEE Non-Volatile Memory Technol. Symp. (NVMTS)*, Oct. 2016, pp. 1–7, doi: [10.1109/NVMTS.2016.7781517](http://dx.doi.org/10.1109/NVMTS.2016.7781517).

[9] *Multi-Dielectric Energy Band Diagram Program*. [Online]. Available: http://nano.boisestate.edu/research-areas/multi-dielectric-energy-band- diagram-program/   
[10] J. Müller, T. S. Boscke, U. Schröder, R. Hoffmann, T. Mikolajick, and L. Frey, “Nanosecond polarization switching and long retention in a novel MFIS-FET based on ferroelectric HfO2,” *IEEE Electron*  *Device Lett.*, vol. 33, no. 2, pp. 185–187, Feb. 2012, doi: [10.1109/LED.](http://dx.doi.org/10.1109/LED.2011.2177435)  [2011.2177435](http://dx.doi.org/10.1109/LED.2011.2177435).

[11] E. Yurchuk, “Electrical characterisation of ferroelectric field effect transistors based on ferroelectric HfO2 thin films,” Ph.D. dissertation, Namlab, Dresden, Germany, 2015.

[12] S. Mueller, S. Slesazeck, T. Mikolajick, J. Müller, P. Polakowski, and S. Flachowsky, “Next-generation ferroelectric memories based on FE-HfO[2](http://dx.doi.org/10.1109/ISAF.2015.7172714),” in *Proc. IEEE ISAF-ISIF-PFM*, May 2015, pp. 233–236, doi: [10.1109/ISAF.2015.7172714](http://dx.doi.org/10.1109/ISAF.2015.7172714).