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 **Strategy Toward HZOBEOL-FeRAM with Low-Voltage Operation (≤1.2 V),**  **Low Process Temperature, and High Endurance by Thickness Scaling**  1K. Tahara, 1K. Toprasertpong, 2Y. Hikosaka, 2K. Nakamura, 2H. Saito, 1M. Takenaka, and 1S. Takagi 1Department of Electrical Engineering and Information Systems, the University of Tokyo, Tokyo, Japan, 2Technology Div., Fujitsu Semiconductor Memory Solution Limited, Kanagawa, Japan   
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**Abstract** The potential of thickness scaling in ferroelectric Hf0.5Zr0.5O2 (HZO) is investigated by a systematic study on MFM capacitors with HZO thickness from 9.5 nm down to 2.8 nm. We establish the thickness-temperature mapping indicating a clear tradeoff between the thickness scaling and crystallization temperature, which has to be taken into account in the implementation as back-end-of-line (BEOL) FeRAM. Utilizing the thickness scaling and high-field wake-up without reliability loss, we demonstrate 4-nm-thick HZO having low crystallization temperature (500ºC), excellent ferroelectricity (2*Pr*>25 C/cm2), low operating voltage (0.7-1.2V), and high read/write endurance (projected to 1014).

**Introduction** HfO2-based ferroelectric thin films [1-2] have triggered a great interest in ferroelectric memory toward VLSI integration owing to their high CMOS compatibility and scalability. In particular, low crystallization temperature around 400ºC of HZO [3-4] enables the application to BEOL memory integration, where the process temperature needs to be as low as possible, at least below 500ºC [5-6]. On the other hand, their large coercive field *EC* (> 1 MV/cm) and typical thickness of 10 nm lead to high operating voltage (> 2 V) that becomes challenging for the implementation in advanced technology nodes. One promising approach to reduce the operating voltage is to scale down the film thickness for reducing the coercive voltage needed for polarization reversal. However, a lack of systematic studies on how the thickness scaling impacts on the optimal process, the ferroelectric properties, and the memory-device reliability (**Fig. 1**) makes it difficult to understand the real potential of thin-film HZO toward BEOL FeRAM. In this study, we systematically investigate the tendency of required annealing temperature in thin HZO, examine the possibility of low-voltage operation (≤ 1.2 V), and demonstrate the significant improvement of read/write endurance with thickness scaling.

**Device preparationFig. 2(a)** shows the process flow of TiN/HZO/TiN MFM capacitors employed in this study. HZO layers with a wide range of thicknesses of 2.8-9.5 nm were prepared by ALD (TEMAH, TEMAZ, and H2O) before being crystallized by rapid thermal annealing in a temperature range of 300-600ºC for 30 s after top TiN deposition. TEM images of 4.0 nm/500ºC and 4.6 nm/450ºC HZO in **Fig. 2(b)-(c)** show that HZO is well crystallized after annealing.

**Strong-field wake-up effect** In thick HZO, clear ferroelec-tric hysteresis loops can be observed with only small wake-up effect. On the other hand, HZO films thinner than 5 nm show AFE-like double hysteresis loops for the pristine state, agreeing with [7], and exhibit clear ferroelectricity with 2*Pr*> 25 C/cm2 after 106 wake-up cycling (**Fig. 3**). After strong-field (4 MV/cm) cycling, the ferroelectricity is activated and thin HZO films exhibit clear hysteresis loops even at operating field much lower than the cycling field (<< 4 MV/cm), while the low-field cycling is insufficient to obtain hysteresis loops with wide memory window (**Fig. 4**).

**Thickness-temperature mapping** The *P-E* characteristics of HZO with various thicknesses and annealing temperatures (**Fig. 5**) illustrate that higher annealing temperature is required for effectively crystallizing the ferroelectric phase in thin HZO: 400ºC, 450ºC, and 500ºC for 9.5-nm, 4.6-nm, and 4.0-nm HZO, respectively. The annealing temperatures and the HZO thicknesses that provide 2*Pr*>10C/cm2 are summarized and mapped in **Fig. 6**, indicating that there is a clear tradeoff between the thickness scaling and ferroelectric-phase crystallization temperature. **Fig. 7** shows a schematic diagram to describe this thickness-temperature tradeoff: more thermal budget is required to crystallize thinner films. The similar diagram has been introduced in [8] to describe doped HfO2 with thickness larger than 10 nm, implying that this diagram is applicable to other HfO2-based ferroelectrics in a wide thickness range. After phase stabilization by annealing, field cycling can boost the transition to the ferroelectric phase,

which has been reported to be reservable [9]. The following examinations focus on MFM capacitors near the boundary of this thickness-temperature mapping (lowest annealing temperature at a given thickness), 500ºC for 4.0-nm, 450ºC for 4.6- and 5.6-nm, and 400ºC for thick HZO, since lower thermal budget is preferable for the BEOL implementation. **Low-voltage operationFig. 8** shows the switching polarization *P*sw (= 2*Pr* for saturation loops) of HZO with various thicknesses for given read/write voltages. At high operating voltage, thicker HZO films are preferred owing to their better ferroelectric phase stability. On the other hand, at low operating voltage, thinner HZO films are favorable to achieve sufficient field against *E*C for polarization reversal. While thick HZO cannot perform well at applied voltage below 1.2 V, 4.0-nm and 4.6-nm HZO films exhibit excellent ferroelectric hysteresis loops down to 0.7 V and 1.0 V, respectively (**Fig. 9**), suggesting the potential of thin HZO in advanced technology nodes. This also results in comparatively better data retention in thin HZO under low-voltage operation (**Fig. 10**). At 1.2 V and 1.0 V read/write operations, much superior same-state (SS) data retention can be found in thin HZO because of higher read/write field. The opposite-state (OS) test, which reflects the imprint behavior, shows comparable tendency to reported literatures [9-10], indicating that the imprint issue still exists in scaled HZO.

*J-E* measurements were **Endurance improvement**   
conducted to investigate the breakdown characteristics (**Fig. 11**). The electrical breakdown of HZO occurs at larger electric field in thinner HZO: *E*BD is 3.5 MV/cm in 9.5-nm HZO and reaches 6 MV/cm in 4.0-nm HZO (**Fig. 12(a)**). This is attributable to lower applied voltage that decreases the energy of electrons flowing through and the damages to the HZO layer, which is similar to the well-known phenomenon in the SiO2/Si MOS system having improved breakdown tolerance with thinning oxide [11-12]. The increase of *E*BD with thickness scaling helps improve the *E*C/*E*BD ratio (**Fig. 12(b)**) and results in the improvement of device reliability especially endurance performance (**Fig. 13**). 4.0-nm HZO with a capacitor area of 3600 m2 shows endurance performance as high as 1010 under the high cycling field of 4 MV/cm at 100 kHz while keeping 2*Pr*>20 C/cm2. When reducing the cycling field to 3 MV/cm (1.2 V operation) after wake-up, the 4.0-nm HZO does not experience breakdown within the experimental time (> 1010 endurance, **Fig. 14(c)**). The endurance of 4.0-nm HZO is projected to be more than 1014 considering the improvement by decreasing field to 3 MV/cm and increasing cycling frequency to 10 MHz (**Fig. 15**), and additional >1000 improvement is further expected by area scaling [5]. The fatigue-limited endurance is also extrapolated to over 1014 thanks to high write field even at 1.2 V. Notable endurance even after wake-up at 4 MV/cm for 106 cycles suggests that the high-field cycling helps improving the ferroelectricity in ultra-thin HZO without reliability penalty. **Conclusion** We show that while the thickness scaling of HZO results in higher crystallization temperature, it enables low-voltage operation (≤1.2 V) and improves the low-voltage data retention as well as the read/write endurance. With a careful consideration of the thickness-temperature tradeoff, the thickness scaling of HZO down to 4 nm suggests the strong potential of ferroelectric HZO toward the highly-reliable, low-voltage operating BEOL FeRAM application.

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| 40 20 Pristine    **Fig. 1** Advantages and challenges in  -20   0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | (a) **4.0 nm** | | | | | | (b) **4.6 nm** | | | | | | (c) **9.5 nm** | | | | | | |  | | | | | |  | | | | | |  | | | | | | |  | | | | | |  | | | | | |  | | | | | | | |  |  | | --- | --- | |  | Pristine  After wake-up | | | | | | |  | | | | | | 10 kHz | | | | | |   -10  -20  0   |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | |  |  |  |  |  |  | | | |
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