Direct Observation of Interface Charge Behaviors in FeFET by Quasi-Static Split C-V and Hall Techniques: Revealing FeFET Operation

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***Abstract*—**A quasi-static split *C-V* technique is proposed as a novel method to monitor ferroelectric polarization and charge distribution in FeFETs. In contrast to conventional split *C-V*, which is not applicable to FeFETs, the proposed technique successfully detects charges induced by *Vg* at the ferroelectric-semiconductor interfaces and extracts real *P*-*Vg* and *Q*-*Vg* characteristics of FeFETs. Through a combination with Hall measurements, responses of minority/majority carriers and trapped charges associated with polarization switching in FeFETs are experimentally obtained for the first time. It is found that trapped carriers, which screen ferroelectric polarization, is a key factor in the device operation of MFIS-FeFET. Our method, extracting *Q*-*Vg* loops directly from FeFET structures, is a powerful tool to understand the real operation and device physics of FeFETs including the memory window and the NC effect.

**I.**  **INTRODUCTION**   
 Ferroelectric-gate field effect transistors (FeFET) have been continuously studied toward a number of applications such as non-volatile memory and in-memory computing [1,2]. Ferro-electric-gate negative-capacitance (NC) FETs have also been investigated as promising steep-slope devices [3]. The ferro-electric technology has been particularly boosted by the dis-covery of ferroelectricity in CMOS-compatible doped HfO2 [4].

In spite of intense studies on FeFETs, charge behaviors during the device operation is still not fully understood. Most studies so far have analyzed charge behaviors in FeFETs indirectly through *Id*-*Vg* characteristics, which is the output affected by many complicated mechanisms (Fig. 1). A typical way widely used to predict the characteristics of FeFETs is to extract the polarization-voltage (*P-V*) properties of the ferroelectric layer from separately prepared MFM (M: metal, F: ferroelectric) or MFS+ (S: semiconductor, +: high doping concentration) structures, and slightly modify the standard model of MOSFETs using Gauss’ law [5,6]. In this conventional approach, charges equivalent to the ferroelectric polarization is considered to be induced in the semiconductor. However, there has been no experimental report that large polarization *P* in typical ferroelectric materials, in the order of 10 μC/cm2 equivalent to more than 1014 cm-2 of surface charge density, can induce such a high inversion carrier density *Ns* in FETs, which must result in MOSFETs with extremely-high *I*ON. It should be noted here that a split *C-V* measurement, a well-known method to evaluate *Ns* in MOSFET channels, is not applicable to FeFETs. Therefore, an alternative approach is required to reveal charge distributions in actual FeFETs.

In this study, we propose a systematic approach with a combination of a novel *P-V-*measurement-inspired *quasi-static split C-V* and *Hall measurements* to evaluate the polarization switching and inversion charge behaviors in FeFETs. This method is applied to Hf0.5Zr0.5O2/Si-based MFIS-FeFET (I: insulator) to clarify, for the first time, the behaviors of electrons, holes, and trapped charges in MFIS interfaces and their roles in the operation of FeFETs.

**II.QUASI-STATIC SPLIT C-VTECHNIQUE**   
*A. Concept*   
 Split *C-V* is a classic method to evaluate the inversion charges in a MOSFET (Fig. 2). A small sinusoidal signal is applied to obtain the small-signal gate-channel capacitance *Cgc*, and the inversion charge density *Qs* is obtained by integrating *Cgc*. In FeFETs, however, spontaneous polarization responses only to the first *Vg* step (Fig. 3). Smaller capacitance is

measured by small-signal *C-V* (Fig. 3 (*ii*) to (*iii*)), hindering us from obtaining the actual *Qs*-*Vg* characteristics (Fig. 3 (*i*) to (*ii*)).

Here, we propose a quasi-static (QS) split *C-V* technique to evaluate the *Qs*-*Vg* relation in FeFETs (Fig. 4(a)). Triangular-shape *Vg* covering a full voltage range of interest (Fig. 4(b)) is applied to obtain large-signal *Cgc* through the relation *C* = *I*/(d*V*/d*t*) (Fig. 4(c)). Since the *Vg* scan is kept in one direction until it reaches maximum or minimum, the ferroelectric polarization does not fall into small-signal minor loops and the actual *Qs*-*Vg* relation can be obtained (Fig. 4(d)). Note that, similar to the conventional split *C-V*, trapped charges may be included in the obtained *Qs*. Due to the principle similar to ferroelectric *P-V* measurements, applying triangular voltages to measure total charges, it is interesting to note that a commercial *P-V* measurement setup can be employed for the proposed QS split *C-V* technique (Fig. 5). If S/D and back contacts are both connected to the current/charge measurement terminal, total charges in/out of the semiconductor when *Vg* is applied can be measured. On the other hand, if only the S/D (back) contact is connected while the other is grounded, the contribution from minority carriers (majority carriers) can be separately evaluated.

*B.Sample Preparation*   
 The fabrication process flow is shown in Fig. 6. A p-Si substrate (*NA* = 4×1015 cm-3) was cleaned and chemically oxidized to form a thin SiO2 IL. 10-nm-thick ferroelectric Hf0.5Zr0.5O2 was then stacked by ALD before capped by TiN electrode. After the FET fabrication process, the device was annealed at 400°C for 30 seconds in N2 atmosphere to form the ferroelectric phase in Hf0.5Zr0.5O2.As a reference, a non-ferroelectric MOSFET was also prepared by the same process except that 10-nm Hf0.5Zr0.5O2 was replaced by 10-nm HfO2. Fig. 7 shows TEM images of both samples, indicating 0.7-nm SiO2 IL at the Si interfaces.

*C.Experimental Results*   
 Fig. 8(a)-(b) shows *Id*-*Vg* characteristics of the HfO2 MOSFET and Hf0.5Zr0.5O2 FeFET in the range of *Vg* ≤ 2 V with the S.Smin (subthreshold swing) values of 63.6 and 66.4 mV/dec shown in Fig. 8(d)-(e), respectively, suggesting the good MOS interfaces. When the FeFET is applied with a wider *Vg* range of -2 V to 3.5 V, *Id*-*Vg* characteristics with ferroelectric hysteresis (Fig. 8(c)) can be observed. No S.S. below 60 mV/dec due to the transient NC effect appears with a slow *Vg* scan rate of 0.1 V/s, which is close to the QS condition [7].

Fig. 9 shows the current response of the non-ferroelectric HfO2 MOSFET from QS *C-V* using 200-Hz triangular *Vg* with S/D and back contacts connected. The gate capacitance *Cg* can be determined using *C* = *I*/(d*V*/d*t*) as shown by the thick red line in Fig. 10(a). QS split *C-V* measurements for *Cgc* and *Cgb* (gate-bulk capacitance) were performed in the same condition and the results are shown in Fig. 10(b)-(c). The relation *Cg* = *Cgc* + *Cgb* is confirmed as shown in Fig. 11, verifying the most important assumption in QS split *C-V* measurement.

To validate the obtained capacitance values, Fig. 10(a)-(c) also compares *Cg*, *Cgc*, and *Cgb* of the HfO2 MOSFET measured from QS split *C-V* and conventional split *C-V*. It can be seen that, except different electron trap behaviors due to different measurement frequencies, both techniques give consistent values of capacitances for this non-ferroelectric MOSFET, resulting in similar *Ns* = *Qs*/*q* obtained from both the two techniques (Fig. 12(a)). We have also confirmed the same results in a standard pure-SiO2 MOSFET as shown in Fig. 12(b).

On theother hand, conventional *C-V* has to be replaced by QS *C-V* for investigating FeFETs. While *C-V* and QS *C-V* give

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similar capacitance values when the FeFET is operated in a small *Vg* range, where the spontaneous polarization does not response (Fig. 13), prominent discrepancy between both capacitance values can be clearly observed when polarization switching occurs (Fig. 14).

The capacitance, i.e. displacement current, peaks indicating polarization switching can be observed from *Cg* in Fig. 14(a). As mostly-full two polarization switching peaks appear, we can say that this device well operates as a hysteretic FeFET in this voltage range. By integrating *Cg* and compensating the influence of the DC gate leakage current *I*DC (Fig. 15), we demonstrate, for the first time, that the polarization-gate voltage (*P*-*Vg*) hysteresis loop can be directly measured in FeFET structures by employing the measurement setup of Fig. 5(left), as shown in Fig. 16(b).

Integration of *Cgc* and *Cgb*, denoted by *Q*SD and *Q*B respectively, provides the contribution of minority and majority carriers in the current flowing in/out of Si when the FeFET operates along the *P*-*Vg* trajectory in Fig. 16(b). *Q*SD and *Q*B in/out of FeFET are shown in Fig. 16(a). One interesting behavior can be seen from the open loop of *Q*SD that, unlike typical MOSFETs in Fig. 10-12, most of electrons flowing from S/D of the MOSFET do not come out through the same route. (Note that *Q*SD and *QB* obtained by capacitance integration gives the charge increment Δ*Q*, not the remaining charges.) Instead, they flow out into the back contact through the p-Si substrate. The schematic is illustrated in Fig. 16(c), suggesting that electrons induced at high positive *Vg* are emitted into the substrate and recombine with holes. Moreover, *Q*SD exhibits surprisingly large *Ns*, which includes both inversion layer charges and trapped charges, in the order of 1014 cm-2 (Fig. 17).

**III.HALL MEASUREMNET**   
 In order to understand these unusual charge behaviors in the FeFET, the Hall measurement was performed in the non-ferroelectric HfO2 MOSFET and the Hf0.5Zr0.5O2 FeFET. The device size is *W*/*L* = 100/280 mm with a Hall bar structure as shown in Fig. 18. These test devices were fabricated on the same substrates as devices described in Section II.

To minimize the electrical stress induced from applied large DC voltage, the Hall voltage *VH* was measured during a *Vg* scan with a rate of 0.1 V/s. Fig. 19-20 show *Id*-*Vg* and *VH*-*Vg* of the HfO2 MOSFET and Hf0.5Zr0.5O2 FeFET. The surface carrier densities *Ns* extracted from *VH*, with the influence of *Ig* compensated by a method in [8] and the Hall factor assumed to be one, are plotted as triangle symbols in Fig. 12(a) for the HfO2 MOSFET, Fig. 12(b) for the standard SiO2 MOSFET, and Fig. 17 for the Hf0.5Zr0.5O2 FeFET. While a good agreement among *Ns* from Hall, split *C-V*, and QS split *C-V* measurements can be confirmed in the non-ferroelectric MOSFETs, *Ns* from the Hall measurement (mobile charges; *Q s* Hall ) of the FeFET is more than

one order of magnitude lower than *Ns* from QS split *C-V* (total charges; *Q*total), implying that a large portion of minority carriers in the FeFET are trapped and do not contribute to the channel current. Under the assumption that trapped charge *Q*trap is given by *Q*total - *Q s* Hall , *Q*trap and the *Q*trap / *Q s* Hall ratio are plotted in Fig. 21. This finding is consistent with the result observed in Fig. 16(c): most electrons flowing from S/D are trapped somewhere in the gate oxide, and subsequently are released and recombined with holes in the substrate.

Since the actual *Ns* can be obtained in this study, we are able to extract the inversion layer mobility of the Hf0.5Zr0.5O2 FeFET. Compared to the typical Hall mobility μH extracted from the HfO2 MOSFET (Fig. 22), μH in the Hf0.5Zr0.5O2 FeFET fabricated with the same process significantly degrades in a low-field region (Fig. 23), suggesting that a Coulomb scattering-like process dominates channel electron conduction. Since acceptable S.S. in the FeFET at low *Vg* is obtained (Fig. 8(e)) and the similar μ*H* reduction is not observed in the HfO2 MOSFET even at high *Vg*(Fig. 22(b)), the μH degradation in the

FeFET is attributed to the characteristics inherent to ferroelectric Hf0.5Zr0.5O2. It is interesting to point out the hysteretic μ*H*-*Ns* relation of the FeFET in Fig. 24. This suggests that μ*H* is not a simple function of *Ns* as expected in conventional MOSFETs, but also dependent on the ferroelectric polarization state, implying the existence of a possible polarization-enhanced scattering process in FeFET channels.

**IV.ANALYSIS OF FEFETOPERATION**   
 Based on the above analysis, a plausible charge distribution in FeFETs when the spontaneous polarization is saturated at the ON state is shown in Fig. 25. To verify our model, the theoretical *P*-*V* characteristics of FeFETs without *Q*trap is calculated using the linear-scaling model for minor loops [9] and depicted in Fig. 26. Here, the bias condition in each diagram corresponds to the labels shown in Fig. 16. When there is no *Q*trap, large polarization in the ferroelectric layer results in large *E*IL in IL, higher than 10 MV/cm in this case (Fig. 27(a)). This causes significant voltage drop across IL, reduces voltage *V*FE across the ferroelectric layer, and limits the polarization to be in a small minor loop unless extremely large *Vg* is applied. Note that theoretical coercive gate voltage difference *Vg* (*P*→ = 0)−*Vg* (*P*← = 0), estimated for this structure, amounts to ~8 V.

On the other hand, our experimental results indicate that the large polarization in the ferroelectric layer is screened by trapped charges to limit the field *E*IL in IL, similar to the phenomenon reported in MFIM structures [10]. In MFIS-FeFETs, polarization screening consequently limits carriers *Ns* in the inversion layer (Fig. 27(b)). Trapped charges cannot be easily de-trapped until *E*IL changes its direction, and eventually, emitted into the Si substrate and recombine with holes in the substrate when the spontaneous polarization is switched to the opposite direction. The charge movement observed during the subthreshold region, which should be suppressed theoretically in FeFETs (thin solid line in Fig. 26), is an evidence that a significant amount of trapped charges are released when the Si surface potential is modulated. With screening due to trapped charges, voltage drop across IL is expected to be suppressed, which is consistent with the clear polarization switching current peaks in Fig. 14 with a small peak-to-peak gap of 3.6 V.

Our proposed approach can effectively explore the charge behaviors in FeFETs and clarify the operation mechanism. In the present demonstration, the measurement condition has been limited to the quasi-static operation to avoid any complications induced by the ferroelectric transient effect. On the other hand, we can also apply this powerful method to judge whether a specific FeFET whose S.S. is below 60 mV/dec is boosted by the quasi-static or transient NC effects. Here, quasi-static NCFETs should give non-hysteretic *P-Vg* loops and the same gate capacitances between small-signal split *C-V* and QS split *C-V* measurements.

**V.**  **CONCLUSION**   
 We have proposed the quasi-static split *C-V* measurement as a novel method to reveal interface charge responses induced by polarization switching in FeFETs. This “split” technique allows us to separately evaluate minority and majority carriers accumulated at the ferroelectric-semiconductor interfaces. Our technique provides a new approach to studying device physics of a wide range of FeFETs, including MFIS-FeFETs, MFMIS-FeFETs, NCFETs, and other complicated FeFETs.

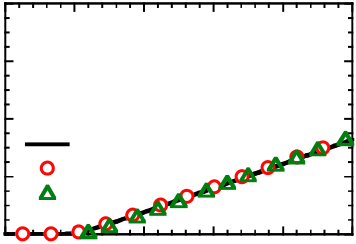
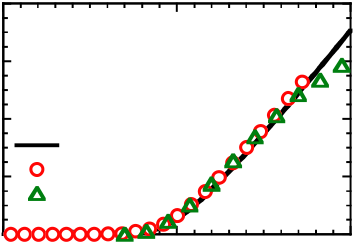
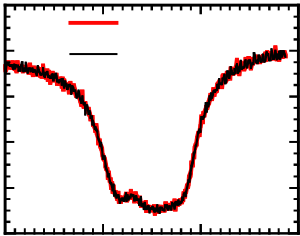
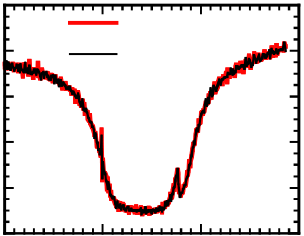
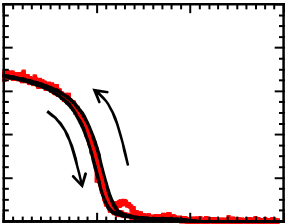
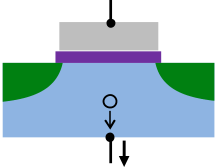
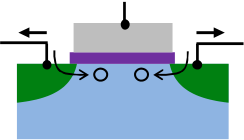
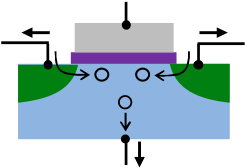
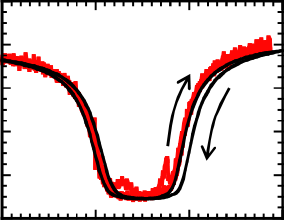
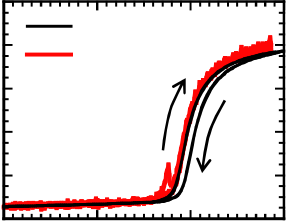
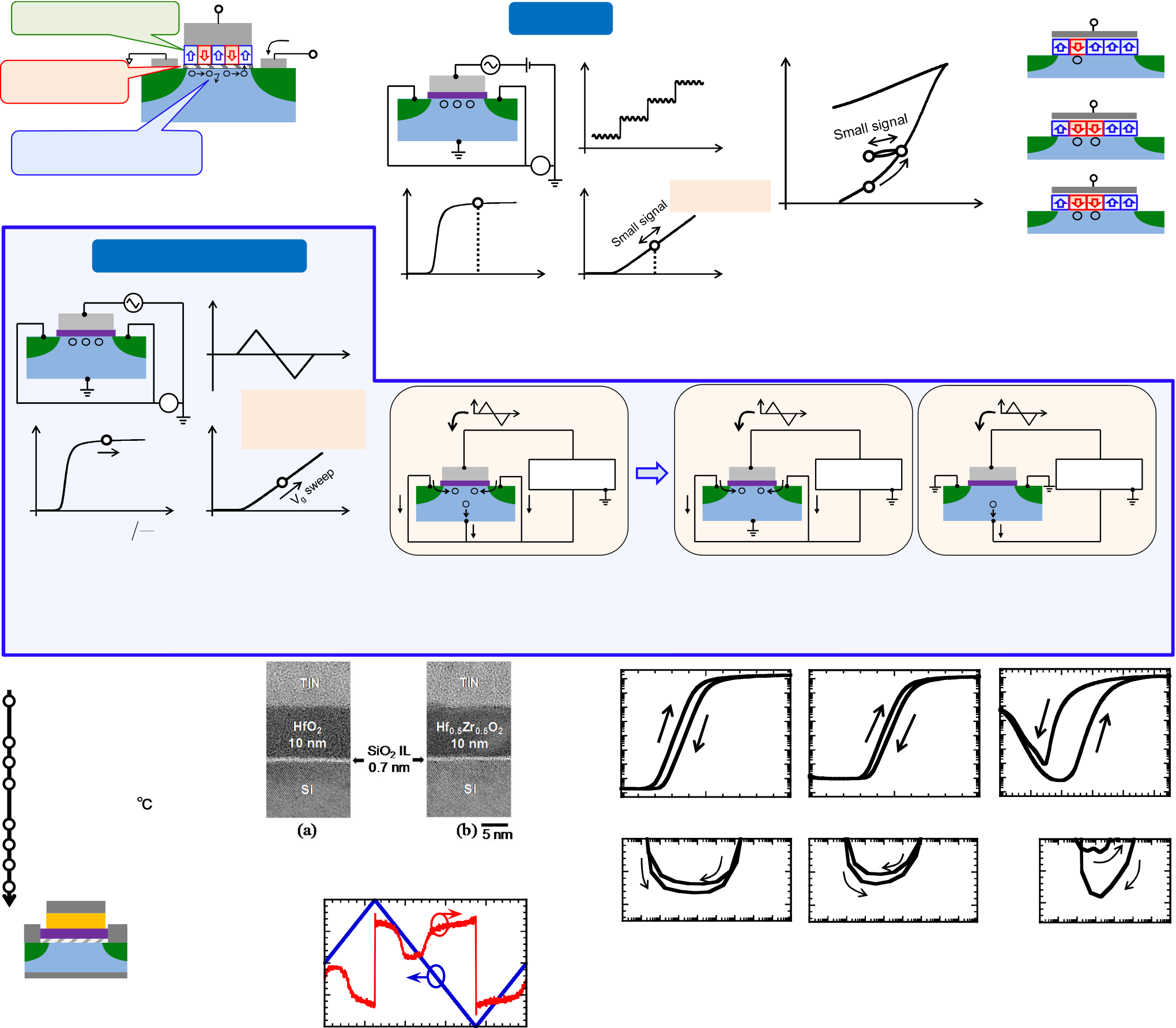
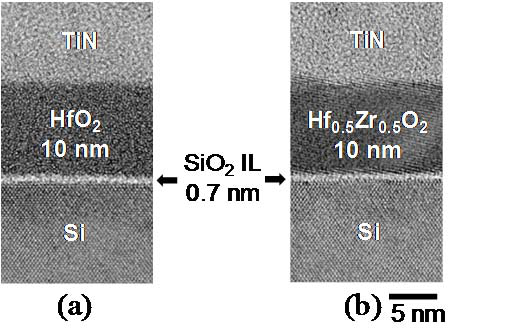
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• Polarization switching

**G**  *Id*  **Split C-V**  (*i*) *V*1

•

•  
 Charge trapping

Voltage drop   
 **S**  
 - - - -

**D**   
 (a)

**G**   
 *v*AC *V*bias (b)

*Vg* input   
 *Qs*

**S** - **D**

**S**

**S** --- **D**  (*ii*) *V*2

• Carrier depletion / inversion (*ii*) **S** - - **D**

Fig. 1 Schematic of FeFET operation.   
 • Charge conduction

(c)

*C*gc   
 A (d)

*Qs*  *Q s* = *C*   
 *t*

*gc dV g*   
 (*iii*)

(*i*)   
 (*iii*) *V*1

*Vg*  **S** - - **D**

**Quasi-static split C-V**  Fig. 3 Small signal response of FeFET. Charge

(a) *Vg*  (b)

*Vg* input   
 *V*bias *Vg*  *V*bias *Vg*  increment during the *Vg* scan from (*i*) to (*ii*)

should be extracted, whereas small-signal *C-V*

**G**  Fig. 2 (a) Conventional split *C-V* technique. measurement considers charge in/out at the

**S**

**S**  
 --- **D**

*t*   
 (b) *Vg* input signal. (c-d) Procedure to obtain

inversion charge density *Qs*.   
 (*ii*)-(*iii*) loop.

(c) (*Id* + *Is*) or *C*gc A (d)

*Qs Q s* =*C* ( *I*

*gc*   
*d* +

*dV*   
*I s*

*g*   
) *dt*   
 *V*

*t*   
 *V*

*t*   
 *V*

*t*

**Split**

*Vg* sweep *P-V*  *P-V*  *P-V*

**G**  measurement **G**  measurement **G**  measurement

**S** - - **D**  **S** - - **D**  **S**  **D**

+ +

( *C* gc = ( *I d* + *I s* ) *dV*

*dt* ) *Vg*  *Vg*  *Is*  *Ib*  *Id*  *Is*  *Id*  *Ib*

Fig. 4 (a) Proposed quasi-static split *C-V*

technique. (b) Triangular waveform as *Vg*  Fig. 5 Quasi-static split *C-V* technique using a standard ferroelectric *P-V* measurement setup.

input. Procedure to obtain (c) *Cgc*-*Vg* and (Left) If S/D and back contacts are all connected, the total charge moves in/out of the MOS

(d) *Qs*-*Vg*. interface is obtained. (Right) By connecting only S/D or back contact to the system, total

electrons and holes in/out of the semiconductor side can be separately evaluated.

100 (a) (b) (c)

***Id* [**μ**A/**μ**m] S.S. [mV/dec]**   
Substrate cleaning 10-2

• *p*-Si, *Na* = 4x1015cm-3

S/D implantation and activation 10-4

HfO2

SiO2 IL growth with SC2 10-6 W/L= 100/5 μm Hf0.5Zr0.5O2 Hf0.5Zr0.5O2

**Hf0.5Zr0.5O2 or HfO2 10 nm**  10-8 Vd = 0.1 V 0 V ↔ 2 V -2 V ↔ 3.5 V

**by ALD at 300**℃ 0 1 2 0 1 2-2 -1 0 1 2 3

TiN 60 nm / Al 400 nm ***Vg* [V]**  ***Vg* [V]**  ***Vg* [V]**

**S.S. [mV/dec]** Annealing at 400℃, 30 s   
Gate patterning

S/D contact   
 Fig. 7 TEM images of MOS interfaces

of (a) HfO2 and (b) Hf0.5Zr0.5O2 on Si   
 80

70   
 (d) (e)   
 160

120 (f)

**Al**  2

***Id***+***Is****+****Ib***  0.2 60 S.Smin = 63.6 mV/dec S.Smin = 66.4 mV/dec 80 S.Smin=87.3 mV/dec

**TiN**

**Al HZO or HfO2**

SiO2 **Al**  1 0.1 10-810-610-410-2100 10-810-610-410-2100 10-810-610-410-2

**S**

Si   
 **D**

0 0 ***Id* [**μ**A/**μ**m]**  ***Id* [**μ**A/**μ**m]**  ***Id* [**μ**A/**μ**m]**  ***Vg* [V]**   
**Al**  ***Vg***  Fig. 8 *Id*-*Vg* of (a) HfO2 MOSFET and (b-c) Hf0.5Zr0.5O2 FeFET at

Fig. 6 Process flow of -1

HfO2  
 -0.1

narrow and wide *Vg* ranges when *Vd* = 0.1 V. (d-f) Corresponding S.S.

FeFET with Hf0.5Zr0.5O2 -2 *W*/*L* = 100/50 μm -0.2 Forward scan Backward scan

0 1 2 3 4 5 100 100

and reference MOSFET **Time [ms]**  *Cg*  *Cg*

with HfO2 Fig. 9 *Vg*-*t* and *I*-*t* profiles during 80 *Cgc*+*Cgb*  80 *Cgc*+*Cgb*

***Cg* [pF]**   
 ***Cg* [pF] *Ns* [1012 cm**-**2]** QS *C-V* measurement at 200 Hz. 60 60

40 40

*Is*

**S** -  
 **G**

- **D**   
 *Id*  *Is*

**S** -  
 **G**

- **D**   
 *Id*

**S**   
 **G**

**D**   
 20

0   
 HfO2 (a)   
 20

0   
 (b)

+ + -1 0 1 2 -1 0 1 2

***Vg* [V]**  ***Vg* [V]**

*Ib*  *Ib*  Fig. 11 Comparison of *Cg* and sum of split *Cgc* and *Cgb*

100

80 HfO2 *W*/*L* = 100/50 μm   
 100

80   
 Split *C-V*

QS split *C-V*   
 100

80   
 in SQ split *C-V* on HfO2 MOSFET for (a) forward and

(b) backward scans.

***Cgb* [pF]**   
 ***Cgc* [pF]**   
***Cg* [pF]**   
 60 60 60 8 8

40 40 40

6 HfO2 MOSFET 6 *Standard*

***Ns* [1012 cm**-**2]** 20

0

-1 0

***Vg* [V]**   
 1   
 (a)

2   
 20

0-1 0

***Vg*[V]**   
 1   
 (b)

2   
 20

0-1   
 (c)

0

***Vg* [V]**   
 1 2   
 4

2   
 Split C-V

QS split C-V   
 4

2   
 Poly-Si/SiO2(25 nm)/Si

MOSFET

Split C-V

QS split C-V

Fig. 10 *C*-*V* characteristics of HfO2 MOSFET obtained by split *C-V* (10 kHz) Hall

(a)   
 Hall

(b)

and QS split *C-V* (200 Hz) techniques for (a) *Cg*, obtained from Fig. 9. (b) *Cgc*  0

0 1 2   
 0

0 1 2 3 4 5

(S/D connected). (c) *Cgb* (back connected). A good agreement of results from ***Vg* [V]**  ***Vg* [V]**

both techniques can be confirmed in HfO2 MOSFET. Electron-trap hysteresis Fig. 12 (a) *Ns* of the HfO2 MOSFET estimated from split *C-*

in split *C-V* is due to comparatively slow *Vg* scan rate, and small peaks in SQ *V*,QS split *C-V* (Fig. 10(b)), and Hall measurements (Fig.

split *C-V* is due to response of trap states. 19). (b) Similar relations for a standard SiO2 MOSFET.

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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 100 | | ***Cg*** | ***Cgc*** | | | ***Cgb*** | | 1,000 | | ***Cg*** | Polarization switching | ***Cgc*** | ***Cgb*** | |
| ***C* [pF]** | 80 | Hf0.5Zr0.5O2 | | (a) | Split *C-V* | (b) | (c) | ***C* [pF]** | 800 | (a) | Interface trap | (b) | Split *C-V* | (c) |
| *W*/*L* = 100/50 μm | | QS split *C-V* | QS split *C-V* |
| 60 | 600 |
| 40 | 400 |
| 20 | | 200 | | | | | | | | | | | | |
| 0  0 0.5 1 0 0.5 1 0 0.5 1 0  -2 -1 0 1 2 3 -2 -1 0 1 2 3 -2 -1 0 1 2 3  ***Vg* [V]**  ***Vg* [V]**  ***Vg* [V]**  ***Vg* [V]**  ***Vg* [V]**  ***Vg* [V]**  Fig. 13 (a) *Cg*, (b) *Cgc*, and (c) *Cgb* of Hf0.5Zr0.5O2 FeFET for a small Fig. 14 (a) *Cg*, (b) *Cgc*, and (c) *Cgb* of Hf0.5Zr0.5O2 FeFET for a wide  *Vg* range obtained by split *C-V* (10 kHz) and QS split *C-V* (200 Hz) *Vg* range that polarization switching can be observed.  techniques. Both forward and backward scans are plotted but mostly 120  overlapped. 1 15 (c) (I) *I*SD 100 Hf0.5Zr0.5O2 FeFET (a)  0.1  10  1  0.1 Hz -0.5  -1  0   |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | |  |  |  |  |  |  |  | | | | | | | | | | | | | | | |
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