IEEE ELECTRON DEVICE LETTERS, VOL. 33, NO. 2, FEBRUARY 2012 185

Nanosecond Polarization Switching and Long Retention in a Novel MFIS-FET Based on Ferroelectric HfO2

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***Abstract*—We report the fabrication of completely CMOS-compatible ferroelectric field-effect transistors (FETs) by stabi-lization of a ferroelectric phase in 10-nm-thin Si : HfO2. The program and erase operation of this metal–ferroelectric–insulator–silicon FET (MFIS) with poly-Si/TiN/Si : HfO2/SiO2/Si gate stack is compared to the transient switching behavior of a TiN-based metal–ferroelectric–metal (MFM) capacitor. Polarization reversal in the MFM capacitor follows a characteristic time and field dependence for ferroelectric domain switching, leading to a higher switching speed with increasing applied field. Similar observa-tions were made for the material when implemented into an MFIS structure. Nonvolatile switching was observed down to 20-ns pulsewidth, yielding a memory window (MW) of 1.2 V. Further increase in gate bias or pulsewidth led to charge injection and degradation of the MW. Retention measurements for up to 106s suggest a retention of more than ten years.**

***Index Terms*—Hafnium oxide, metal–ferroelectric–insulator–semiconductor (MFIS) FET, nonvolatile memory.**

I. INTRODUCTION

**A** [1] first proposed a nonvolatile memory concept based on LMOST half a century has passed since Moll and Tarui

a single transistor (1T) whose gate insulator had been replaced

by a ferroelectric material. Since then, various material combi-

nations and gate stack configurations have been investigated. In

the course of a slow-moving progress, low data retention caused

by insufficient interfacial charge screening and gate leakage

current was predicted to be a persistent road blocker for this

technology [2]. However, recent results on MFIS stacks have

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proven otherwise. With the use of high-*k* dielectrics as insu-lating buffer (e.g., HfO2 based) and ferroelectrics with a rather low dielectric constant (e.g., SBT or polymer ferroelectrics), low voltage operation and low depolarization fields are within reach and are no longer keeping the device from becoming the ultimate memory device it was thought to be [3]–[5]. However, in addition to these promising results, the temperature stability of organic ferroelectrics in a standard CMOS flow remains questionable, and the commonly used perovskite-based ferroelectrics such as SBT and PZT [6] require special inte-gration schemes due to the sensitivity of the materials toward hydrogen [7] and the large physical height of the gate stack. Additionally, their composing elements as well as the required noble metal electrodes may pose contamination risks to con-ventional CMOS and are therefore rarely qualified in large-scale IC manufacturing. Recently, however, it has been shown that crystallization of Si : HfO2 in the presence of a mechanical confinement, e.g., titanium nitride metal gate (TiN-MG), leads to a noncentrosymmetric orthorhombic phase, which, in turn, produces a spontaneous polarization [8]. Ferroelectricity in HfO2, a material that, so far, was only considered as insulating buffer layer in MFIS-FETs [3]–[6], now offers the opportunity to form highly scaled ferroelectric FET and capacitor devices. Great benefit can be drawn from the efforts that have already been made in the field of conventional high-*k*/metal gate and DRAM storage capacitor integration using HfO2-based HKs and TiN-MG.

In this letter, we report on the polarization switching kinetics of Si : HfO2-based MFM capacitors and superimposed charge injection phenomena in the related MFIS structure. Tran-sient pulsing schemes were applied to deduce conditions for optimized memory operation. Retention measurements were conducted to validate memory functionality for short pulse program and erase.

II. EXPERIMENTS

TiN/Si : HfO2/TiN capacitors (5000–50 000 *μ*m2) and gate-first long channel (*L* = 0.35–20 *μ*m) poly-Si/TiN/Si : HfO2/SiO2/p-Si FETs were prepared using 300-mm manufac-turing equipment. Si : HfO2 films were grown by ALD using the metal–organic precursors tetrakis(ethylmethylamino)hafnium (TEMAH) and tetrakis(dimethylamino)silane (4DMAS) with ozone. A film thickness of 10 nm was defined by the deposi-tion cycles and controlled by spectral ellipsometry and TEM

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186 IEEE ELECTRON DEVICE LETTERS, VOL. 33, NO. 2, FEBRUARY 2012

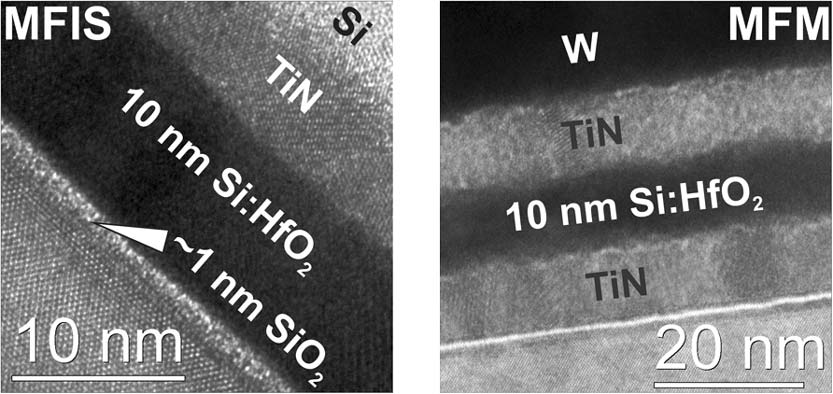


Fig. 1. TEM micrographs of ferroelectric Si : HfO2 integrated into (right) a TiN-based MFM capacitor and into (left) the MFIS gate structure of a FeFET.

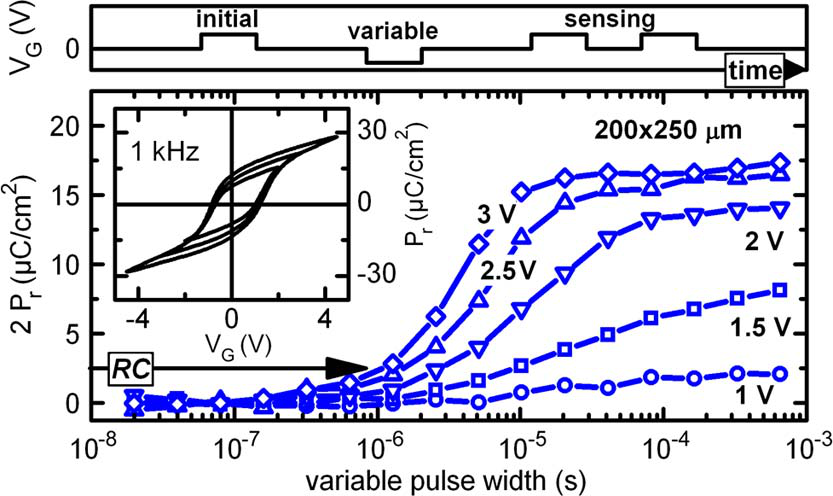


Fig. 2. Polarization hysteresis measurements of a TiN/Si : HfO2/TiN capaci-tor reveal a characteristic subloop to saturation behavior with (inset) increasing bias sweep. A transient PUND characterization shows the time/voltage depen-dent polarization switching of the capacitor. With increasing applied field, faster polarization reversal is observed. However, absolute switching times are largely dominated by the *RC* delay of the measurement setup.

(Fig. 1), whereas the SiO2 content in HfO2 was tuned by the 4DMAS/TEMAH cycle ratio and confirmed by XPS to be around 5 mol%. The TiN-MG for the MFM structure as well as for the MFIS gate stack was formed in a CVD process from TiCl4 and NH3. The CVD process temperature was adjusted below the crystallization temperature of the Si : HfO2 thin film, while crystallization was induced in a downstream postmet-allization anneal at 650*◦*C. For the transfer of the 10-nm ferroelectric layer to an MFIS-type gate stack, a slightly higher Si content was chosen to account for the activation anneal at 1000*◦*C during transistor fabrication. This measure was found to be necessary to obtain equally behaved ferroelectrics at dif-ferent thermal budgets and is possibly caused by Si segregation.

III. RESULTS AND DISCUSSION

Polarization hysteresis measurements of an MFM capacitor are shown in the inset of Fig. 2. When the applied voltage is swept sufficiently high, in this case above *±*3 V accounting for three times the coercive field *Ec* of 1 MV/cm, fully saturated hysteresis loops can be recorded. Remanent polarization *Pr* for this saturated polarization loop is estimated to be 11 *μ*C/cm2, whereas for smaller bias sweeps, a typical subloop behavior of incomplete polarization reversal is observed. Similar to commonly known ferroelectrics, this minor hysteresis loops lead to a drop of *Pr* and a slightly lower *Ec*. Those subloops are of great importance in MFIS-FETs since they are preferably accessed to avoid high interfacial fields and switching voltages. To gain further insight into the switching kinetics of the ferroelectric Si : HfO2 thin films, a modified positive up neg-

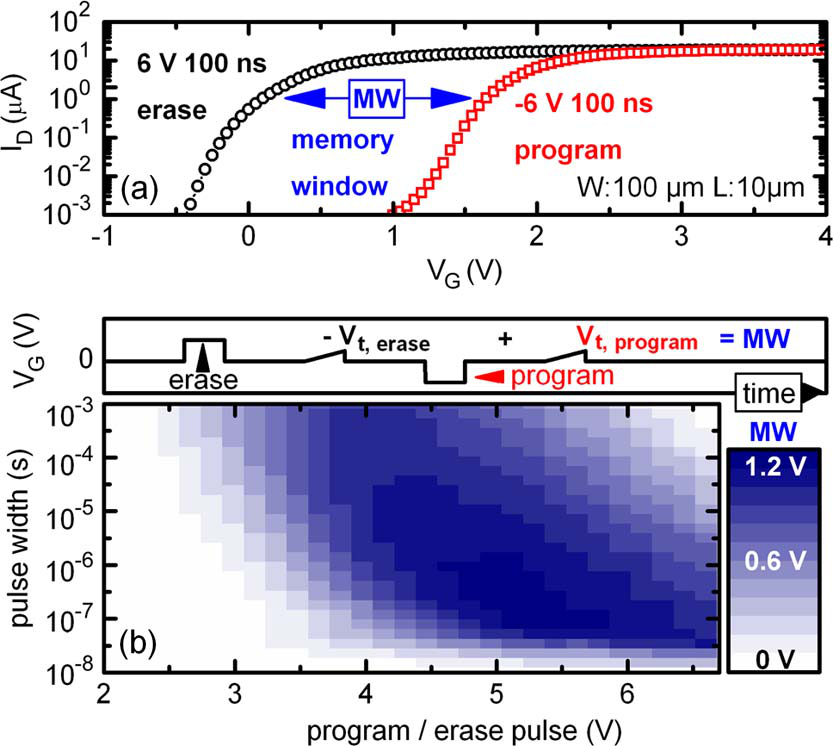


Fig. 3. (a) *Id*–*Vg* measurements of a Si : HfO2-based MFIS-FET after a 100-ns +6-V program and *−*6-V erase pulse. As expected from ferroelectric polarization switching, a counterclockwise threshold voltage hysteresis is ob-served. (b) Transient program/erase matrix (10 ns–1 ms, 2–6.6 V) reveals an MW evolution depending on ferroelectric switching kinetics and superimposed charge injection at high field and pulsewidth.

ative down (PUND) [9] methodology was applied (Fig. 2). Following a +3-V initialization pulse, a variable negative pulse was applied to the MFM capacitor. The charge switched by the variable pulse was then evaluated by the comparison of two consecutive +3-V sensing pulses, recording the polarization reversal and the linear contribution of the capacitor. A steep increase in *Pr* and an early saturation can be observed for voltages well above *Ec*, whereas for pulses slightly above or even at *Ec*, only slow polarization reversal occurs. Different from the subloop behavior observed at a fixed frequency and voltage ramp rate, this pulsed characterization shows that, given time, a saturated polarization level even at low fields can still be achieved. The general trend to faster switching speeds with increasing voltage is frequently observed in ferroelectrics and shows that polarization reversal is a statistical process strongly accelerated when exceeding certain activation fields [10]. For the FeFET, this leaves the opportunity of fast program/erase at high electric field and slow program/erase at low electric field. When integrating the ferroelectric transistor into a memory matrix, this behavior defines the possible array architectures.

Erase at positive gate bias, defined as lowering the nFET threshold voltage, and program at negative gate bias, turning off the transistor by increasing the threshold voltage, were similar like for the MFM structure realized by a single burst from a pulse generator connected to the gate. Fig. 3(a) shows the char-acteristic response of a ferroelectric Si : HfO2-based transistor to a 100-ns *±*6-V program/erase pulse. The counterclockwise hysteresis, as opposed to the clockwise hysteresis observed for charge trapping devices, clearly shows the ferroelectric switching behavior of the transistor.

A transient program and erase pulse train, schematically shown in Fig. 3, was applied to investigate the switching time and voltage behavior of the device. The resulting MW matrix reaching from 2 to 6.5 V for 10 ns–1 ms pulsewidth is shown in Fig. 3(b). Just as expected from MFM data on switch-ing kinetics, the time and voltage dependence of polarization

MÜLLER *et al.*: NANOSECOND POLARIZATION SWITCHING AND LONG RETENTION 187

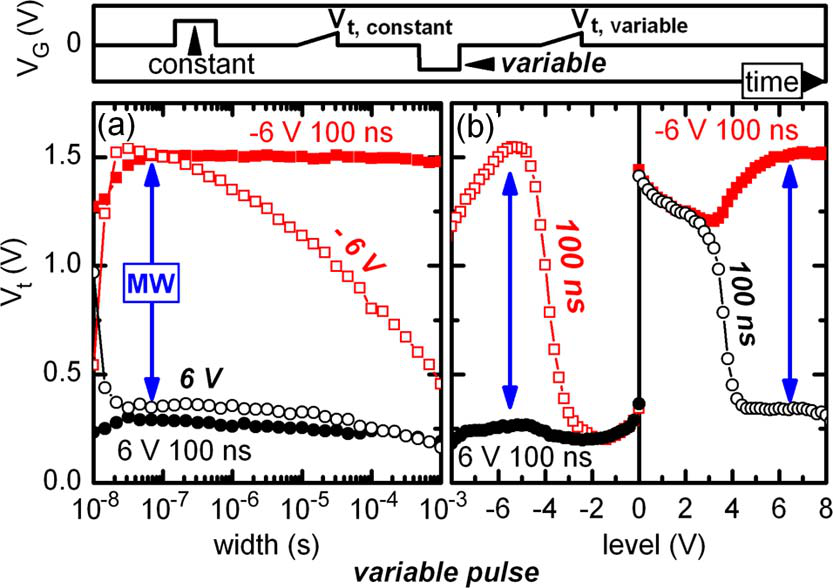


Fig. 4. Asymmetric time and voltage (a) program (fixed erase, variable pro-gram) and (b) erase (fixed program, variable erase) reveal an MW degradation caused by charge injection for high program voltage and pulsewidth.

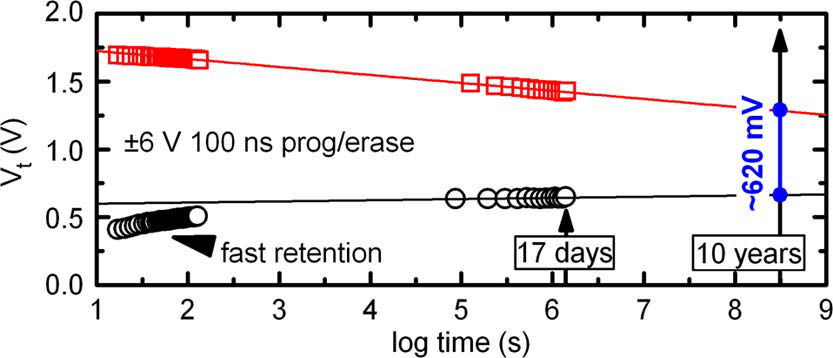


Fig. 5. Retention of a Si : HfO2-based FeFET. Despite an initially fast retention loss, extrapolation yields an MW of 620 mV after ten years.

is strongly field dependent, it shows a saturating behavior with decreasing depolarization field. On a scale of days, this eventually leads to a moderate retention loss and therewith to a stable MW of 780 mV after 17 days. Based on the fairly linear retention loss on the logarithmic time scale, as suggested by the data, a simple extrapolation yields a residual MW of 620 mV after ten years.

IV. CONCLUSION

In summary, a completely CMOS-compatible MFIS-FET has been fabricated by implementing ferroelectric Si : HfO2 thin films in conjunction with a TiN-MG. A characteristic field and time dependence of ferroelectric polarization reversal was ob-served for MFM capacitors as well as for the MFIS gate stacks. Limited only by the measurement setup, switching speeds down to 20 ns were observed, opening up an MW of about 1.2 V. However, for a high program voltage and pulsewidth, charge injection was found to limit the influence of the ferroelectric polarization onto the threshold voltage shift. Additionally, a stable MW was demonstrated after 17 days. A simple linear extrapolation of retention data predicts a residual MW of 620 mV after ten years.

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| reversal is clearly reflected in the formation of the ferroelectric MW. Planes of equally high MW are stretched toward lower | REFERENCES |

voltages with increasing pulsewidth. Superimposed on this trend, however, charge injection starts to dominate the MW for high voltages and increasing pulsewidth. This charge trapping having a qualitatively similar time and voltage dependence shifts the threshold voltage in the opposite direction, until for the highest voltages and longest pulses applied the ferroelectric MW has completely vanished.

To further investigate the degradation of the MW, asymmetric program and erase schemes were applied. As shown in Fig. 4, a variable erase at fixed program conditions leads to a stable MW up to the maximum voltage and pulsewidth applied, whereas a variable program operation shows clear indications of charge injection at higher voltage and longer pulsewidth. For the device being in strong accumulation during erase operation, this threshold voltage shift being opposed to the ferroelectric influence can only be explained by hole injection from the substrate or electron detrapping that extends into the bulk of the Si : HfO2 film with increasing time and voltage. Similar observation for TiN/HfO2/SiO2/p-Si gate stacks has already been made by Lu *et al.* who claimed hole injection from the substrate to be the dominant reason for threshold voltage instabilities at negative voltage stress [11].

Room temperature retention measurements of the MFIS-FETs were conducted to validate the stability of the memory state for fast pulsing schemes (Fig. 5). For the erase state, a fast retention loss is observed within the first minutes. We assume that this fast loss of MW is caused by depolarization-field-enhanced electron trapping. However, since this process

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