

IEEE ELECTRON DEVICE LETTERS, VOL. 42, NO. 9, SEPTEMBER 2021 1295



Wakeup-Free and Endurance-Robust

Ferroelectric Field-Effect Transistor Memory

Using High Pressure Annealing

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***Abstract— Wakeup-free and endurance-robust HfZrO2 (HZO)***  ***ferroelectric***  ***field-effect***  ***transistor***  ***(FeFET)***  ***was fabricated on a silicon-on-insulator substrate. After a high-pressure forming gas annealing as the last alloy step, the performance and endurance of the FeFETs were sig-nificantly improved by trap states reduction, polarization enhancement, and wake-up elimination. As the result, the FeFETs show superior endurance exceeding1010cycles and robust retention behavior at program/erase biases of*±*3.5V and pulse width of 100 ns. These results indicate that appropriate thermal treatment for the interlayer and ferroelectric material could substantially improve FeFET performance and reliability.***

***Index***  ***Terms— Ferroelectric***  ***FET***  ***(FeFET),***  ***HZO, endurance***  ***characteristics***  ***of***  ***FeFET,***  ***high-pressure annealing.***

I. INTRODUCTION   
**F** been studied recently for future low-power nonvolatile ERROELECTRIC field-effect transistors (FeFETs) have

memory application thanks to their potential for single transis-tor operation and non-destructive, fast read operation [1]–[6]. Especially, since thin doped HfO2 (*<*5 nm) compatible with CMOS process is ferroelectric in the orthorhombic phase

Manuscript received June 17, 2021; revised June 30, 2021; accepted July 7, 2021. Date of publication July 12, 2021; date of current ver-sion August 26, 2021. This work was supported in part by INHA University Research Grant, in part by the Brain Korea 21 Plus Project in 2021, in part by the Future Semiconductor Device Technology Development Program funded by the Ministry of Trade, Industry and Energy (MOTIE) and the Korea Semiconductor Research Consortium (KSRC) under Grant 10067739 and Grant 20010847, and in part by the National Research Foundation (NRF) funded by the Korean Ministry of Science and ICT under Grant 2020M3F3A2A01081670 and Grant 2020M3F3A2A01081666. The review of this letter was arranged by Editor U. Schroeder. (Manh-Cuong Nguyen, Sihyun Kim, and Kitae Lee contributed equally to this work.) (Corresponding authors: Rino Choi; Daewoong Kwon.)   
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Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LED.2021.3096248.

Digital Object Identifier 10.1109/LED.2021.3096248

and remanent polarization (Pr*)*/coercive field (Ec*)* of these films can be adjusted by doping concentration, annealing conditions, and capping layer [7]–[14], FeFETs having doped HfO2 ferroelectric layer (FE) as a gate dielectric has been extensively researched. However, despite these advantages, the HfO2-based FeFETs has shown poor endurance (*<*106cycles) because of the degradation by charge trapping and defect generation [15]–[17]. Typically, an interlayer (IL) with *<*1 nm equivalent oxide thickness (EOT) should be used in FeFETs to suppress depolarization field and to maximize voltage drop across FE.

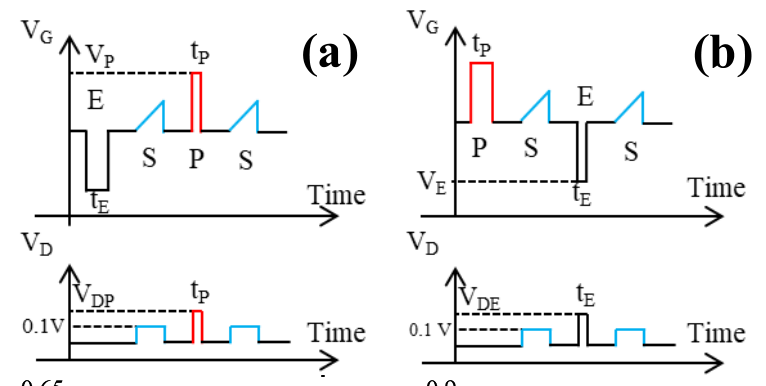
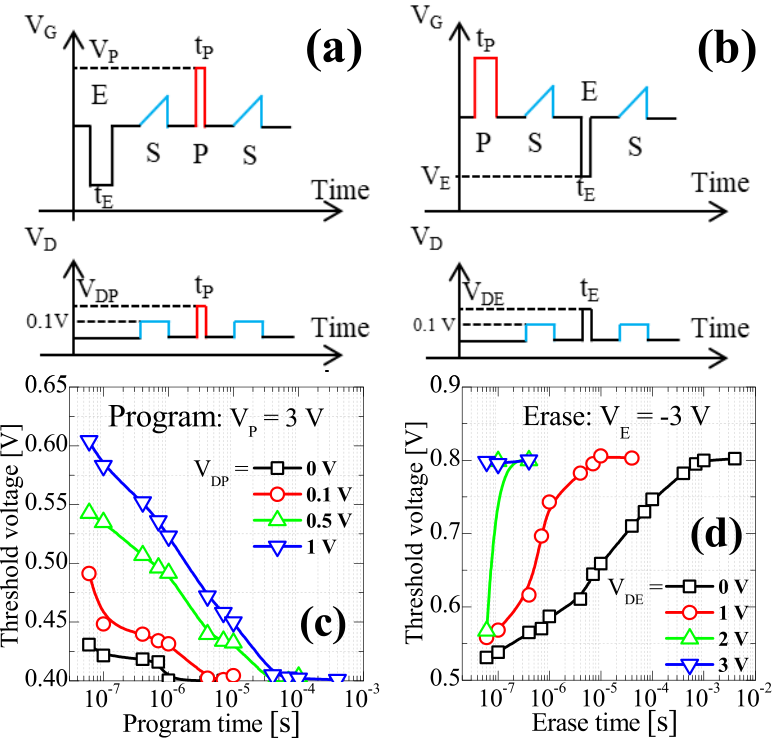
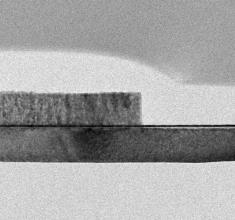
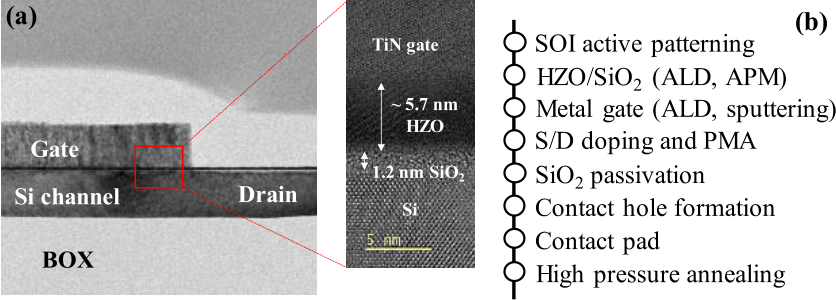
As IL is thinner, a higher electric field is applied across IL, which limits the endurance due to IL degradation. Thus, a high-quality IL with *<*1 nm EOT is required to secure endurance robustness. In this study, to achieve a ∼1 nm thick SiO2 high-quality IL without sacrificing HZO polarization, high-pressure forming gas annealing (HPA) was adopted as the last alloy step. Performance and endurance improvements after the HPA were experimentally verified and the physical origin of the improvements was rigorously investigated.

II. FABRICATION PROCESS

The FeFETs were fabricated on a 100-nm-thick silicon-on-insulator (SOI) wafer. After the active patterning, the gate stack was fabricated with SiO2 IL, Hf0*.*5Zr0*.*5O2 (HZO), and TiN. The SiO2 was formed by chemical oxidation using an APM solution (NH4OH:H2O2:H2O = 1:1:5). Next, HZO was deposited using ALD. The deposition cycle consists of 1 cycle of HfO2 followed by 1 cycle of ZrO2. This was repeated 30 times to yield a 6 nm HZO film. Subsequently, 3 nm ALD TiN was deposited and 100 nm TIN was sputtered sequentially on the HZO as a gate metal. Here, the 3 nm ALD TiN plays the role of a blocking layer to prevent the sputtering damage which degrades the HZO and IL (thus, degraded endurance). Gate region was patterned and ion (arsenic) implantation was performed on the exposed source/drain areas with the dose of∼1020and the energy of 15 keV. An RTA at 500◦C for 30 s in N2 ambient was performed as a post-metal annealing (PMA) to activate dopants and to form the orthorhombic phase (O-phase) in HZO. SiO2 was deposited as an interlayer dielectric and the metal contacts of sputtered TiN/Ti/Al were formed. Fig. 1(a) shows the TEM cross-sectional gate stack image where the thicknesses of the SiO2 IL and HZO are confirmed to be 1.2 nm and 5.7 nm, respectively.

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Fig. 1. (a) TEM images of fabricated HZO FeFET and enlarged gate stacks. (b) Summarized process flow of the device.

Fig. 2. Dependence of the threshold voltage on the program and erase conditions (bias and timing): (a) voltage setup and (b) experimental data for the program. (c) Voltage setup and (d) measured data for the erase.

III. RESULTS AND DISCUSSION

To optimize the operating conditions of the fabricated FeFET, the dependences of the program (P) and erase (E)

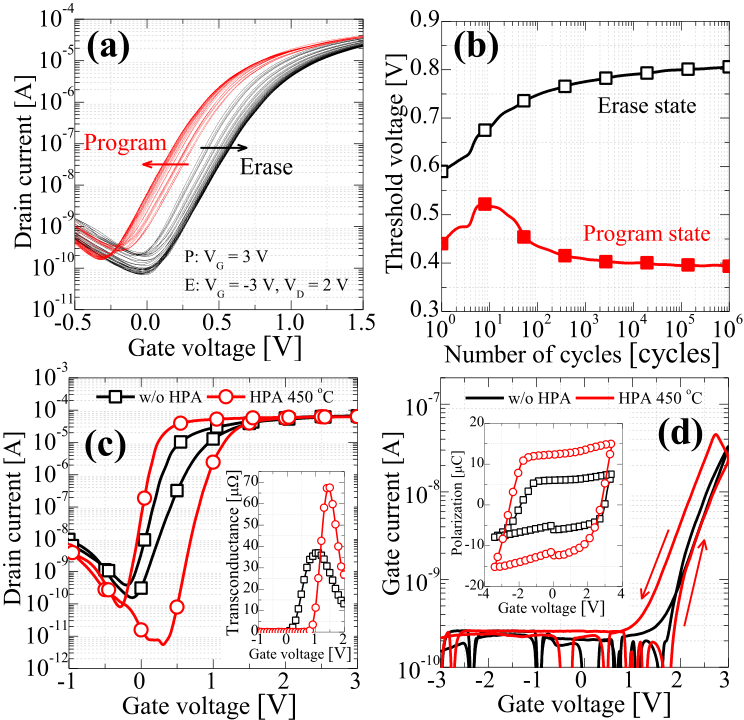


Fig. 3. Endurance characteristics of the FeFET under the selected stress condition summarized in (a) transfer characteristics and (b) threshold voltage. Effects of high pressure annealing on the device performance: (c) hysteretic transfer characteristics and corresponding transconduc-tance. (d) Hysteretic gate current and P-V characteristics by PUND.

the generated holes by GIDL are injected into the floating body, the polarization swathing by VE gets enhanced by the accumulated holes [11], and erasing speed becomes faster. Thus, to erase the FeFET at VE = −3 V less than 100 ns, VDE of 2 V is selected.

Figs. 3(a) and (b) show the endurance characteristics of the FeFET under the selected stress condition (VP = 3 V / VDP = of 100 ns between VP and VE*)*. Note that few hundred cycles 0 V, VE = −3 V / VDE = 2 V, tP = tE = 100 ns, delay time are needed to wake up the device. Though the FeFET can work over 106cycles without serious degradation, the MW is small (0.4 V) and an undesirable wake-up is required.

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| operations on | the | voltage | and | time | were | investigated. | To improve the electrical characteristics of the FeFET, |

Figs. 2(a) and (b) illustrate the bias and timing diagrams for the program, erase, and sense (S). The sense condition (gate voltage was swept from −0.5 V to 1.5 V while drain voltage was kept at 0.1 V) was chosen to sense threshold voltage (VT*)* but without affecting the polarization of the ferroelectric layer. The width (W) and length (L) of the FeFET under tests are 80 *μ*m and 1 *μ*m. The threshold voltage was extracted at The program voltage (VP*)* and the erase voltage (VE*)* were ID = 10−7∗W/L.

selected to maximize the memory window (MW) since it is determined by an interplay between charge trapping and ferroelectric switching. With the VP of 3 V, the dependences of VT on the program time (tP*)* and the drain voltage (VDP*)* are summarized in Fig. 2(c). The higher VDP results in a longer program time because the drain-side energy band becomes higher than the source-side by the smaller gate-to-drain volt-age (VGD*)* and thus VT is determined by the drain-side energy barrier [11]. As a result, it is confirmed that tP *<* 100 ns can be obtained by VP = 3 V and VDP = 0 V for sufficient programming. With the VE of −3 V, the dependence of VT on the erase time (tE*)* and the drain voltage (VDE*)* was shown in Fig. 2(d). It is observed that the faster erasing is achievable with the larger VDE. This phenomenon can be explained by the combined effects of the larger VGD and gate-induced drain leakage (GIDL) on erasing. For the n-type SOI FeFETs, there are hardly any holes in the body and therefore VE is ineffectual to apply any meaningful voltage across HZO. However, when

high pressure (20 atm) annealing (HPA) was performed at 450◦C for 30 minutes under the forming gas (Ar 96 %, H2 4 %) ambient after the metal contacts formation. It is clearly observed that the FeFET has the steeper subthreshold swing (SS), higher transconductance (gm*)*, and wider MW after the HPA (Fig. 3(e)). To verify the origin of the wider MW, the ferroelectric switching current was directly extracted from the FeFET [19] to evaluate the ferroelectricity (polariza-tion) before/after the HPA through positive-up negative-down (PUND) measurement method by excluding displacement and leakage current components. The inset of Fig. 3(d) shows that Pr is enhanced after the HPA because the HPA might help the additional O-phase transition (strongly related to Pr*)* of the HZO from the tetragonal phase (T-phase). This hypothesis is supported by the gate current (IG*)* change in Fig. 3(d) where the IG is diminished and the clear counter-clockwise hysteretic IG appears after the HPA, which is the strong indicator of both the trap density reduction and the Pr enhancement.

The enhancement of endurance characteristics by the HPA were confirmed under the re-optimized stress condition, VP = 3.5 V, VE = −3.5 V, VDE = 2 V, tP = tE = 100 ns, delay time of 100 ns between VP and VE (Figs. 4(a) and 4(b)). Fig. 4(c) demonstrates that the FeFET can have an endurance exceeding be deteriorated and especially the E state shows more serious 1010cycles. From ∼108cycles, both the P and E states start to degradation; yet the separation of the VT retains a margin of 0.6 V until 1 × 1010cycle which is comparable with the

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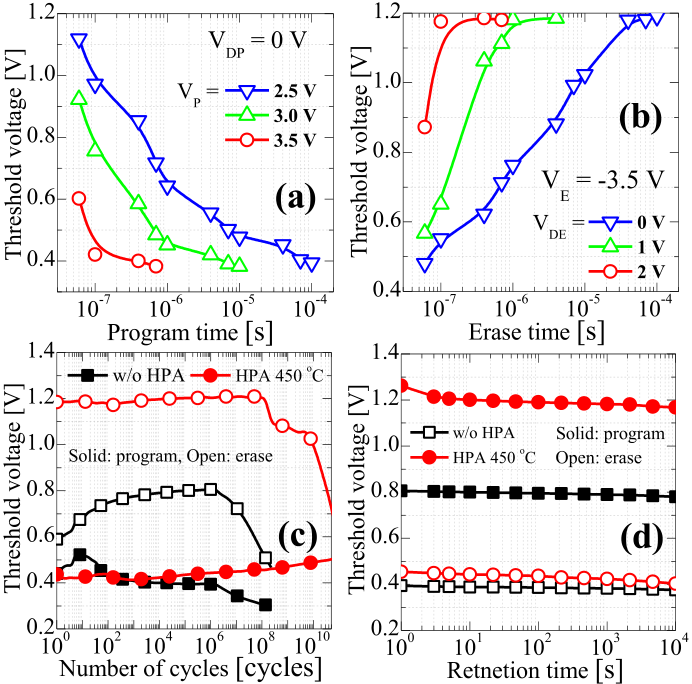


Fig. 4. Threshold voltage dependence on (a) program and (b) erase conditions. (c) Endurance and (d) retention (300 K) characteristics before and after HPA.

FeFET using a SiNx interlayer [20] or channel last FeFETs without any IL [21], [22]. Notably, the undesirable wake-up is not needed, which is consistent with the increasing O-phase (namely, T-phase reduction) after the HPA because it has been reported that the wake-up is strongly related to cycling-induced phase transition from T-phase to O-phase [23]. In addition, the retention behavior was checked after 106P/E cyclings during 104seconds at 300 K and 385 K. Fig. 4(d) and 5(a) indicate that the retention looks robust even after the P/E cycling regardless of the HPA although the MWs are reduced at 385 K due to the increasing charge trapping probability and reduced polarization.

To understand which mechanism dominates the endurance degradations after the HPA, the oxide trap density (Nox*)* and the interface trap density (Nit*)* were extracted using the pulsed ID–VG method and the subthreshold swing method, respectively. The inset in Fig. 5(b) presents the transient drain current recorded by applying a gate pulse of 2 V (lead edge of 1 *μ*s, width of 5 ms) and a constant drain voltage of 0.1 V. The current reduction over time is correlated with the oxide trap density. Therefore, Nox could be extracted using the following equation [24]

*Nox* =*κH Z O* ∗ *ε*0∗*VT ,*  (1)

*Nox* =*κH Z O* ∗ *ε*0∗*ID q* ∗ *gm*  (2)

where *κ*HZO, *ε*0, xHZO,VT, and q are HZO relative dielectric constant (16), vacuum permittivity, defect location (from the gate interface), threshold voltage shift, and elementary charge, respectively. The oxide trap states are assumed to be located at the border between the HZO and SiO2, so that Eq. (1) could be described as Eq. (2) where tHZO andID are the HZO thickness and the drain current reduction. Meanwhile, the Nit and the interface trap density increase (Nit*)* during the endurance test could be simply extracted using the following

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| equations [25], [26]   *Nit* =*Cox*�*kT* ln *(*10*)*− 1 *q* ∗ *SS* � *Nit* =*Cox* ∗*SS* | *,* | (3) |
| (4) |

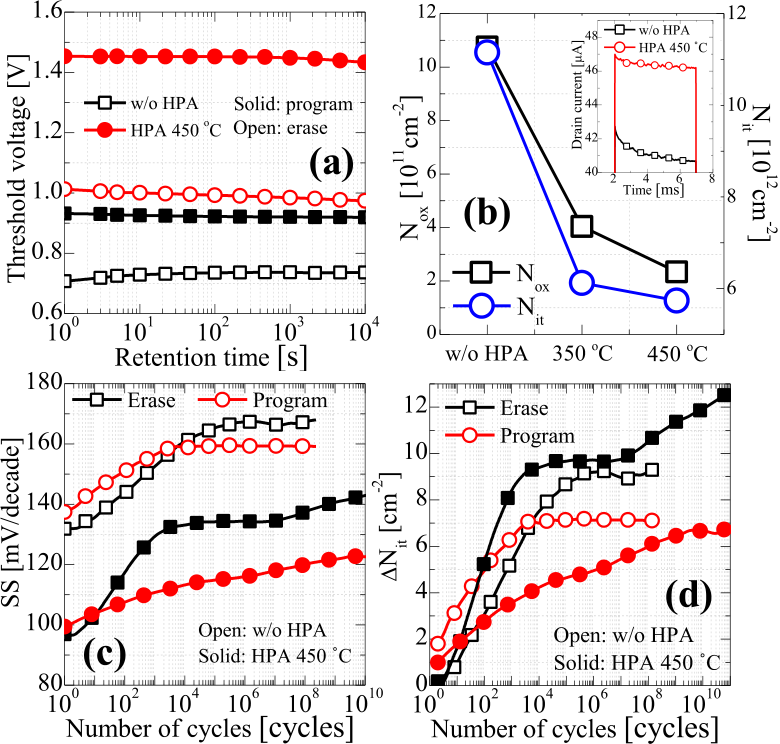


Fig. 5. (a) Retention characteristics (385 K) before and after HPA. (b) Trap reduction of the FeFET after HPA. Inset shows the transient drain current characteristics. (c) SS and (d) interface trap generation calculated at P and E states with respect to the number of P/E cycling.

where Cox,SS, k, and T are oxide capacitance, SS degra-dation, Boltzmann constant, and ambient temperature, respectively.

Fig. 5(b) shows the significant reduction of Nit and Nox after the HPA and these reduction should contribute to the memory window enhancement and improved endurance characteristics. Two degradation phenomena are observed during the P/E stress: an SS degradation (Fig. 5(c)), and a systematic leftward shift (Fig. 4(c)) of both the VTs of the E and P states (the E state shifts more substantially). While the interface trap density gets saturated and then the VTs start to be leftward-shifted for both the P and E states in the FeFET without HPA, both the SSs of the E and P states are continuously deteriorated until 1 ×1010cycle (especially, the E state shows more serious degradation in Fig. 5(c) and 5(d)) with the simultaneous VT shift only for the E state from ∼108cycle in the FeFET with HPA. Therefore, the SS degradation and VT shift can be explained by the damage-induced trap generation and hole trapping respectively, which result from the injections of the GIDL-induced holes and the holes generated by the hot electrons from the gate into the gate dielectric.

IV. CONCLUSION   
 The wakeup-free and endurance-robust FeFETs are demon-strated using high-pressure forming gas annealing. By mon-itoring the changes of the electrical characteristics after the HPA, it is found that HPA contributes significantly to the performance and endurance improvements through trap states reduction, polarization enhancement, and wakeup elimination. After optimizing the biases and timings for program/erase operations, the FeFETs successfully show larger than 1010 endurance cycles. To reveal the endurance limiting factors and to further improve the endurance, the degradation mechanisms were rigorously analyzed by measuring the VT/SS changes of P and E states with respect to the number of cycling. As a result, it is proved that the VT shift and SS degradation mainly result from the injections of the GIDL-induced holes and the holes generated by the hot electrons from the gate into the gate dielectric.

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REFERENCES

[1] K. Ni, P. Sharma, J. Zhang, M. Jerry, J. A. Smith, K. Tapily, R. Clark, S. Mahapatra, and S. Datta, “Critical role of interlayer in Hf0*.*5Zr0*.*5O2 ferroelectric FET nonvolatile memory performance,” *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2461–2469, Jun. 2018, doi:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| [10.1109/TED.2018.2829122](http://dx.doi.org/10.1109/TED.2018.2829122). | | S. Müller, | M. Noack, | J. Müller, |
| [2] H. Mulaosmanovic, | J. Ocker, |

P. Polakowski, T. Mikolajick, and S. Slesazeck, “Novel ferroelectric FET based synapse for neuromorphic systems,” in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. T176–T177, doi: [10.23919/VLSIT.2017.7998165](http://dx.doi.org/10.23919/VLSIT.2017.7998165).

[3] K. Chatterjee, S. Kim, G. Karbasian, D. Kwon, A. J. Tan, A. K. Yadav, C. R. Serrao, C. Hu, and S. Salahuddin, “Challenges to partial switching of Hf0*.*8Zr0*.*2O2 gated ferroelectric FET for multilevel/analog or low-voltage memory operation,” *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1423–1426, Sep. 2019, doi: [10.1109/LED.2019.2931430](http://dx.doi.org/10.1109/LED.2019.2931430).

[4] M. Jerry, P. Chen, J. Zhang, P. Sharma, K. Ni, S. Yu, and S. Datta,“Ferroelectric FET analog synapse for acceleration of deep neural network training,” in *IEDM Tech. Dig.*, Dec. 2017, pp. 6.2.1–6.2.4, doi: [10.1109/IEDM.2017.8268338](http://dx.doi.org/10.1109/IEDM.2017.8268338).

[5] C. Jin, T. Saraya, T. Hiramoto, and M. Kobayashi, “On the physical mechanism of transient negative capacitance effect in deep subthreshold region,” *IEEE J. Electron Devices Soc.*, vol. 7, pp. 368–374, Feb. 2019, doi: [10.1109/JEDS.2019.2899727](http://dx.doi.org/10.1109/JEDS.2019.2899727).

[6] B. Obradovic, T. Rakshit, R. Hatcher, J. A. Kittl, and M. S. Rodder,“Modeling transient negative capacitance in steep-slope FeFETs,” *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 5157–5164, Nov. 2018,

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| doi: [10.1109/TED.2018.2868479](http://dx.doi.org/10.1109/TED.2018.2868479). | | | | | | Z. | Hong, | P. | García-Fernández, |
| [7] A. | K. | Yadav, | K. | X. | Nguyen, |

P. Aguado-Puente, C. T. Nelson, S. Das, B. Prasad, D. Kwon, S. Cheema, A. I. Khan, C. Hu, J. Íñiguez, J. Junquera, L.-Q. Chen, D. A. Muller, R. Ramesh, and S. Salahuddin, “Spatially resolved steady-state negative capacitance,” *Nature*, vol. 565, no. 7740, pp. 468–471, 2019, doi: [10.1038/s41586-018-0855-y](http://dx.doi.org/10.1038/s41586-018-0855-y).

[8] P. D. Lomenzo, Q. Takmeel, S. Moghaddam, and T. Nishida, “Annealing behavior of ferroelectric Si-doped HfO[2 thin films,](http://dx.doi.org/10.1016/j.tsf.2016.07.009)” *Thin Solid Films*, vol. 615, pp. 139–144, Sep. 2016, doi: [10.1016/j.tsf.2016.07.009](http://dx.doi.org/10.1016/j.tsf.2016.07.009).

[9] K. Katayama, T. Shimizu, O. Sakata, T. Shiraishi, S. Nakamura, T. Kiguchi, A. Akama, T. J. Konno, H. Uchida, and H. Funakubo,“Growth of (111)-oriented epitaxial and textured ferroelectric Y-doped HfO2 films for downscaled device[s,”](http://dx.doi.org/10.1063/1.4962431) *Appl. Phys. Lett.*, vol. 109, no. 11, Sep. 2016, Art. no. 112901, doi: [10.1063/1.4962431](http://dx.doi.org/10.1063/1.4962431).

[10] M. H. Park, C. C. Chung, T. Schenk, C. Richter, M. Hoffmann, S. Wirth, J. L. Jones, T. Mikolajick, and U. Schroeder, “Origin of temperature-dependent ferroelectricity in Si-doped HfO2,” *Adv.*

*Electron. Mater.*, vol. 4, no. 4, Apr. 2018, Art. no. 1700489, doi: [10.1002/aelm.201700489](http://dx.doi.org/10.1002/aelm.201700489).

[11] P.-J. Sung, C.-J. Su, S.-H. Lo, F.-K. Hsueh, D. D. Lu, Y.-J. Lee, and T.-S. Chao, “Effects of forming gas annealing and channel dimen-sions on the electrical characteristics of FeFETs and CMOS inverter,”*IEEE J. Electron Devices Soc.*, vol. 8, pp. 474–480, Apr. 2020, doi: [10.1109/JEDS.2020.2987005](http://dx.doi.org/10.1109/JEDS.2020.2987005).

[12] P. Sharma, K. Tapily, A. K. Saha, J. Zhang, A. Shaughnessy, A. Aziz, G. L. Snider, S. Gupta, R. D. Clark, and S. Datta, “Impact of total and partial dipole switching on the switching slope of gate-last negative capacitance FETs with ferroelectric hafnium zirconium oxide gate stack,” in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. T154–T155, doi: [10.23919/VLSIT.2017.7998160](http://dx.doi.org/10.23919/VLSIT.2017.7998160).

[13] A. J. Tan, A. K. Yadav, K. Chatterjee, D. Kwon, S. Kim, C. Hu, and S. Salahuddin, “A nitrided interfacial oxide for interface state improvement in hafnium zirconium oxide-based ferroelectric transistor technology,” *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 95–98, Jan. 2018.

[14] H. Bae, S. G. Nam, T. Moon, Y. Lee, S. Jo, D.-H. Choe, S. Kim, K.-H. Lee, and J. Heo, “Sub-ns polarization switching in 25 nm FE FinFET toward post CPU and spatial-energetic mapping of traps for enhanced endurance,” in *IEDM Tech. Dig.*, Dec. 2020, pp. 31.3.1–31.3.4, doi: [10.1109/IEDM13553.2020.9372076](http://dx.doi.org/10.1109/IEDM13553.2020.9372076).

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| [15] E. | Yurchuk, | J. | Muller, | S. | Muller, | J. | Paul, | M. | Pesic, |

R. van Bentum, U. Schroeder, and T. Mikolajick, “Charge-trapping phenomena in HfO2-based FeFET-type nonvolatile memories,” *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3501–3507, Sep. 2016, doi: [10.1109/TED.2016.2588439](http://dx.doi.org/10.1109/TED.2016.2588439).

[16] A. J. Tan, M. Pešic, L. Larcher, Y.-H. Liao, L.-C. Wang, J.-H. Bae,

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| C. | Hu, | and | S. | Salahuddin, | | “Hot | electrons | | as | the | | domi- |
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| in | *Proc.* | *IEEE* | | *Symp.* | *VLSI* | *Technol.*, | | Jun. | 2020, | | pp. 1–2, | |

doi: [10.1109/VLSITechnology18217.2020.9265067](http://dx.doi.org/10.1109/VLSITechnology18217.2020.9265067).

[17] M. Pesic, A. Padovani, S. Slcsazeck, T. Mikolajick, and L. Larcher, “Deconvoluting charge trapping and nucleation interplay in FeFETs: Kinetics and reliability,” in *IEDM Tech. Dig.*, Dec. 2018, pp. 25.1.1–25.1.4, doi: [10.1109/IEDM.2018.8614492](http://dx.doi.org/10.1109/IEDM.2018.8614492).

[18] K. Lee, S. Kim, J.-H. Lee, D. Kwon, and B.-G. Park, “Analysis on reverse drain-induced barrier lowering and negative differential resistance of ferroelectric-gate field-effect transistor memory,” *IEEE Electron Device Lett.*, vol. 41, no. 8, pp. 1197–1200, Aug. 2020, doi: [10.1109/LED.2020.3000766](http://dx.doi.org/10.1109/LED.2020.3000766).

[19] K. Toprasertpong, M. Takenaka, and S. Takagi, “Direct observation of interface charge behaviors in FeFET by quasi-static split C-V and Hall techniques: Revealing FeFET operation,” in *IEDM Tech. Dig.*, Dec. 2019, pp. 23.7.1–23.7.4, doi: [10.1109/IEDM19573.2019.8993664](http://dx.doi.org/10.1109/IEDM19573.2019.8993664). [20] A. J. Tan, Y.-H. Liao, L.-C. Wang, N. Shanker, J.-H. Bae, C. Hu, and S. Salahuddin, “Ferroelectric HfO2 memory transistors with high-K interfacial layer and write endurance exceeding 1010 cycles,” *IEEE Electron Device Lett.*, vol. 42, no. 7, pp. 994–997, Jul. 2021, doi: [10.1109/LED.2021.3083219](http://dx.doi.org/10.1109/LED.2021.3083219).

[21] A. A. Sharma, B. Doyle, H. J. Yoo, I.-C. Tung, J. Kavalieros, M. V. Metz, M. Reshotko, P. Majhi, T. Brown-Heft, Y.-J. Chen, and V. H. Le, “High speed memory operation in channel-last, back-gated fer-roelectric transistors,” in *IEDM Tech. Dig.*, Dec. 2020, pp. 18.5.1–18.5.4, doi: [10.1109/IEDM13553.2020.9371940](http://dx.doi.org/10.1109/IEDM13553.2020.9371940).

[22] S. Dutta, H. Ye, W. Chakraborty, Y.-C. Luo, M. S. Jose, B. Grisafe, A. Khanna, I. Lightcap, S. Shinde, S. Yu, and S. Datta, “Monolithic 3D integration of high endurance multi-bit ferroelectric FET for accelerating compute-in-memory,” in *IEDM Tech. Dig.*, Dec. 2020, pp. 36.4.1–36.4.4, doi: [10.1109/IEDM13553.2020.9371974](http://dx.doi.org/10.1109/IEDM13553.2020.9371974).

[23] H. J. Kim, M. H. Park, Y. J. Kim, Y. H. Lee, T. Moon, K. D. Kim, S. D. Hyun, and C. S. Hwang, “A study on the wake-up effect of ferroelectric Hf0*.*5Zr0*.*5O2 films by pulse-switching mea- surement,” *Nanoscale*, vol. 8, no. 3, pp. 1383–1389, 2016, doi: [10.1039/C5NR05339K](http://dx.doi.org/10.1039/C5NR05339K).

[24] C. D. Young, J. H. Zhao, D. Heh, R. Choi, B. H. Lee, and G. Bersuker, “Pulsed I*d*–V*g* methodology and its application to electron-trapping characterization and defect density profiling,” *IEEE Trans.*

*Electron Devices*, vol. 56, no. 6, pp. 1322–1329, Jun. 2009, doi: [10.1109/TED.2009.2019384](http://dx.doi.org/10.1109/TED.2009.2019384).

[25] N. Gong and T.-P. Ma, “A study of endurance issues in HfO2-based ferroelectric field effect transistors: Charge trapping and trap generation,”*IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 15–18, Jan. 2018, doi: [10.1109/LED.2017.2776263](http://dx.doi.org/10.1109/LED.2017.2776263).

[26] W. Xiao, C. Liu, Y. Peng, S. Zheng, Q. Feng, C. Zhang, J. Zhang, Y. Hao, M. Liao, and Y. Zhou, “Memory window and endurance improvement of Hf0*.*5Zr0*.*5O2-based FeFETs with ZrO2 seed layers characterized by fast voltage pulse measurements,” *Nanosc. Res. Lett.*, vol. 14, no. 1, pp. 1–7, Dec. 2019, doi: [10.1186/s11671-019-3063-2](http://dx.doi.org/10.1186/s11671-019-3063-2).

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