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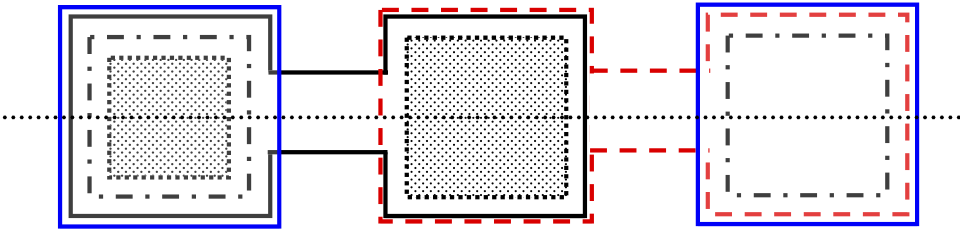
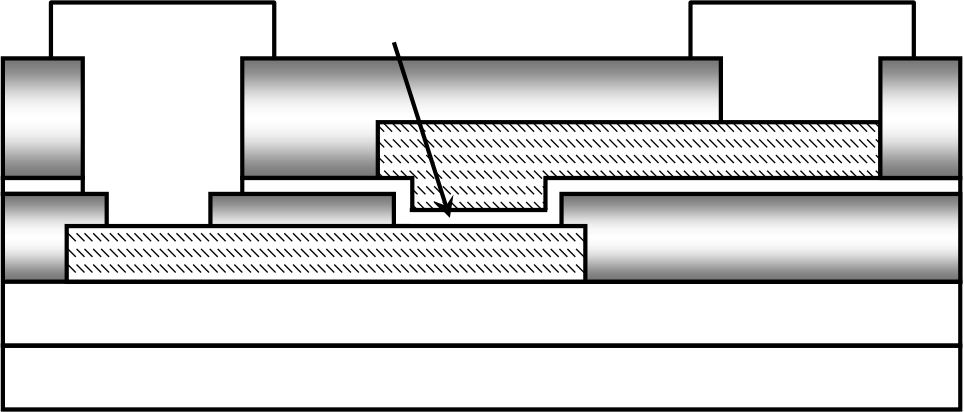
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| Japanese Journal of Applied Physics 49 (2010) 04DB16 | REGULAR PAPER |

Stability of La2O3 Metal–Insulator–Metal Capacitors under Constant Voltage Stress

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Received October 16, 2009; accepted December 25, 2009; published online April 20, 2010

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| In this study, we demonstrate the stability of high-� La2O3 metal–insulator–metal (MIM) capacitors under constant voltage stress (CVS). It was |

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| found that the variation in capacitance caused by CVS strongly depends on the injected charges regardless of stress biases. Furthermore, the |

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| quadratic voltage coefficient of capacitance (�) decreases with a logarithmic increase in dielectric loss. Charge trapping contributes to the relative |

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| capacitance variation under CVS while the reduced carrier mobility due to the stress-induced traps is responsible for the reduction of �. |

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| Additionally, high stability of 10-year lifetime is achieved for a 10-nm La2O3 MIM capacitor with an 11.4 fF/mm2capacitance density. |

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| 1. | Introduction | |  | | --- | | [DOI: 10.1143/JJAP.49.04DB16](http://dx.doi.org/10.1143/JJAP.49.04DB16) | |

Recently, metal–insulator–metal (MIM) capacitors integrat-

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| ed into the backend interconnect as passive components | | | | | | | **A** | **Cap.** | | **Al** | **A’** |
| have generated great interest for applications such as radio | | | | | | |
| frequency (RF) and analog Si integrated circuits (ICs).1–4) | | | | | | | **ILD2** | **(a)** | | **ILD2** |
| For example, MIM capacitors are widely used for RF | | | | | | |
| **Al** | **10-nm La2O3**  **ILD2** |
| bypass and decoupling capacitors and for digital-to-analog | | | | | | |
| (D/A) and analog-to-digital (A/D) converters owing to | | | | | | |
| their | highly | conductive | electrodes | and | low | parasitic |  | **TaN/Ni Top Electrode** | | **ILD1** |
| capacitance.5,6)Because the capacitor usually consumes a | | | | | | |
| large fraction of the whole chip area, MIM capacitors with | | | | | | |
| **TaN/Ta Bottom Electrode** | |
| a high capacitance density have been eagerly pursued to | | | | | | |
| **Buffer Oxide** | |
| reduce the chip size and system cost.7)However, the higher | | | | | | |
| capacitance density of MIM capacitors cannot be simply | | | | | | | **Si Substrate** | |
| achieved by further thinning the conventional silicon | | | | | | | **(b)** | |

dioxide (SiO2) or silicon nitride (Si3N4) films because of leakage and reliability issues.8)Therefore, the only viable solution is adopting high-� materials as dielectrics of MIM capacitors.

In the last few years, many high-� dielectrics, such as Ta2O5,9)HfO2,10)Al2O3,11)TiO2,12)and various compounds and laminates of these materials,13–17)have been investigated for MIM capacitors. Owing to their various superior proper-ties,18–21)such as large band gap (>5 eV), high breakdown electric field, low leakage current, and good oxide reliability, lanthanum oxide (La2O3) and La-based oxides are among

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| the | most | promising | high-� | dielectrics | for | the | future |

technology nodes. However, unlike SiO2, which is an almost ideal insulator, high-� dielectrics usually contain plenty of bulk traps and interface states, especially after electrical stress. These nonideal defects cause instability of devices during operation,22–24)which leads to the distortion of analog functions performed by the MIM capacitor and further limits the performance of RF/analog circuits. As a result, from the viewpoint of practical use, the electrical-stress-induced degradation of high-� MIM capacitors is a serious concern. Some studies25,26)have discussed the capacitance variation of SiO2 MIM capacitors under electrical stress. However, the degradation of a high-� MIM capacitor under electrical stress has not been well characterized. Therefore, in this study, the behaviors of La2O3 MIM capacitors under constant voltage stress (CVS) were investigated. The correlations among the injection charge (Qinj), the relative

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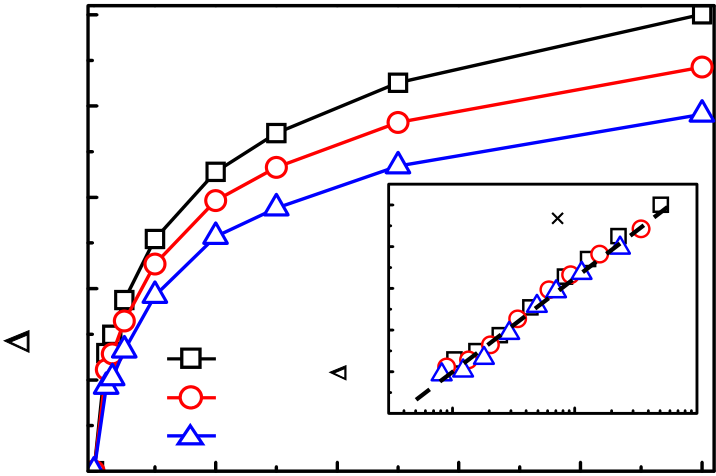
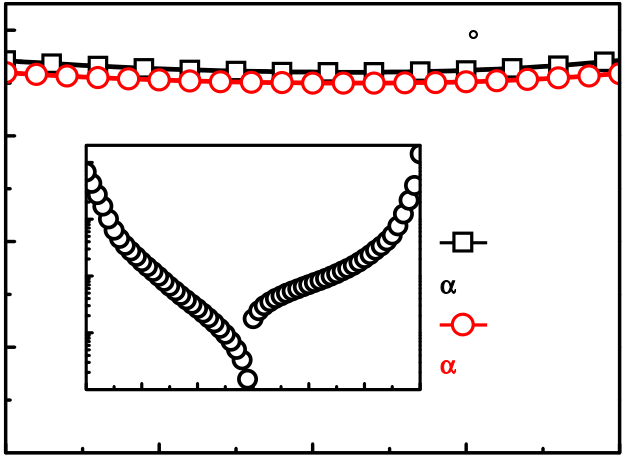
Fig. 1. (Color online) (a) Schematic layout of the La2O3 MIM capacitor. (b) Schematic cross section of the capacitor along the A–A0cutline in the layout shown in (a).

capacitance change ½�C=Cðt ¼ 0Þ�, the quadratic voltage coefficient of capacitance (�), and the dielectric loss (D) of the La2O3 MIM capacitor were discussed.

2. Experimental Procedure

A 10-nm La2O3 MIM structure with an area of 2500 mm2 was fabricated in this study. The schematic layout and cross section of the capacitor along the A–A0cutline in the layout are shown in Figs. 1(a) and 1(b), respectively. The high-�La2O3 film was deposited by electron beam evaporation and annealed in O2 ambient to improve its quality. The bilayer top (TaN/Ni) and bottom (TaN/Ta) electrodes were depos-ited by reactive sputtering. The Ta and TaN layers were used to reduce the parasitic resistance and to serve as a diffusion barrier layer, respectively. All the process temperatures during MIM capacitor fabrication were below 400�C, compatible with the backend process. The samples were then subjected to CVS in the range of �4:2 to �5 V. Afterwards, the capacitance–voltage (C–V) curves were measured at 25�C using an LCR meter at various stress time intervals, and the dielectric loss (D) was also observed simultaneously. All the electrical measurements were carried out by applying a voltage to the top electrode while the bottom electrode was grounded.

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| Jpn. J. Appl. Phys. 49 (2010) 04DB16 | | | | | | | | |  |  |  |  | **Ni/10-nm La2O3 /TaN** | | | | | S.-H. Wu et al. |
| **2) Capacitance Density (fF/**μ**m** | **11.6** | **Ni/10-nm La2O3 /TaN** | | | | **at 25**°**C** | | | **2** | Δ**C/C(t=0) (%)** | **2.5** | **0** | **-3**  **10** |
| **11.2** | **2)** | **-5 10** | | **Applied Voltage** | | **6** | **Measurement** | **2.0** | **at 100 kHz** | | | | |
| **Current Density (A/cm** |
| **10.8** | **-6 10** | | **Frequency** | **1.5** | **2.5** | | | **Y = 6.3 + 1.15** × **log X** | |
| **on Ni Electrode** | |
| **10 kHz** |
| **Stress Bias** | Δ**C/C(t=0) (%)** | **2.0** | | |
| **10.4** | **-7 10** | | **Top** | **Bottom** | α**=775 ppm/V2** | **1.0** | **1.5** | | |
| **-8 10** | | **100 kHz** | **1.0** | | |
| **Injection** | **Injection** |
| **-9**  **10-6** | | α**=671 ppm/V2** | **0.5** | **-5 V** | **0.5** | | |
| **-4** **-2**  **0**  **2**  **4**  **Applied Voltage (V)** | | **-4.8 V** | **0.0** | | **-5**  **10** | **-4**   **10**  **Qinj (C/cm 2)** |
| **0.0** | **-4.6 V** |
| **10.0**  **-2** | | | **-1** | | **0** | **1** | |
| **200** | **400** | | **600** | **800** | **1000** |
| **Applied Voltage (V)** | | | | | | | |
| **Stress Time (s)** | | | | |

Fig. 2. (Color online) C–V curve, J–V curve, and the quadratic voltage

coefficient of capacitance (�) of a typical 10-nm La2O3 MIM capacitor.

Fig. 3. (Color online) Relative capacitance variation ½�C=Cðt ¼ 0Þ� as

a function of stress time and injection charge (Qinj) at various CVS

voltages from �4:6 to �5 V.

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| 3. | Results and Discussion | out. As reported in ref. 15, a higher barrier height between |

Figure 2 shows the C–V and J–V characteristics of the 10-nm La2O3 MIM capacitor. The capacitance density at zero bias is about 11.4 fF/mm2, and the leakage current densities at �1:5 and +1.5 V are 16 and 56 nA/cm2, respectively. The leakage current density is satisfactory because the operating voltage of the RF/analog MIM capacitor is smaller than 1.5 V for the sub-65 nm technology node.15)The quadratic voltage coefficient of capacitance (�), used to depict the voltage dispersion or voltage dependency of capacitance, is obtained from fitting the C–V curves by the second-order polynomial equation:

CðVÞ ¼ C0 � ð� � V2þ � � V þ 1Þ; ð1Þ where C0 is the capacitance at zero bias. The � values of the 10-nm La2O3 MIM capacitor measured at 10 and 100 kHz are 775 and 671 ppm/V2, respectively. The positive �represents a capacitance density rise with the increase in applied voltage, which may be attributed to the high degree of electric field polarization and carrier injection.4,9,10) During the voltage sweeping, some of the injected carriers would be captured by the interface trap states existing in the dielectric near the injection electrode. These trapped charges could induce dipoles following the alternating signals with a dipole relaxation time. Moreover, the other injection carriers become excess mobile charges in the insulator, and these mobile charges also follow the small ac signals with a free carrier relaxation time that depends on the mobility and density of carriers. The dipole and free carrier relaxation time contribute to various frequency-dependent character-istics in RF/analog MIM capacitors. As the measurement frequency increases, the trapped-charge-induced dipoles and the excess mobile charges hardly follow the ac signal, corresponding to the longer relaxation times of these dipoles and mobile charges. Thus, the capacitance fluctuation due to

the electrode and the dielectric leads to the better capaci-tance stability of MIM capacitors under CVS. The higher barrier height at the metal/insulator interface reduces carrier injection and therefore results in less charge trapping in the dielectric. In our devices, Ni and TaN were in direct contact with La2O3 as top and bottom electrodes. The top injection under negative voltage stress is chosen because of the higher work function of Ni (�5 eV) than that of TaN (�4:5 eV). Figure 3 shows the relative capacitance variation ½�C=Cðt ¼ 0Þ� as a function of stress time at various CVS voltages from �4:6 to �5 V. The relative capacitance variation is defined as

Cðt ¼ 0Þ ¼ C0ðtÞ � C0ðt ¼ 0Þ ; ð2Þ

where C0ðt ¼ 0Þ is the initial capacitance at zero bias before stress, and t is the stress time. ½�C=Cðt ¼ 0Þ� increases with the CVS voltage and the stress time. On the other hand, ½�C=Cðt ¼ 0Þ� is also plotted as a function of the injected charge (Qinj) in the inset of Fig. 3. The relative capacitance variation increases with a logarithmic increase in Qinj regardless of the stress biases, which implies that the increasing charge trapping in dielectrics during CVS is responsible for the capacitance variation.27)The trapped charges in the preexisting traps and in stress-induced traps generate dipoles to increase the local permittivity and the capacitance. Among them, the stress-induced dipoles con-tribute to the relative increase in capacitance with respect to its initial condition, and that is the degradation of the capacitance.25,26)Specifically, the relative capacitance var-iation is proportional to the amount of stress-induced trapped charges. Furthermore, the trapping probability,26)the ratio of trapped charge variation, �Qtrap, to injected charge varia-tion, �Qinj, obeys a power law relation:

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| the varied applied voltages becomes smaller and results in | �Qtrap | K Qn ; | 3 |
|  |
| the lower � with increasing frequency. While both dipole | �Qinj | ¼ � inj | ðÞ |
| polarization and free carrier polarization could modulate the |

capacitance, the free carrier effect is believed to play the major role in the voltage dependence of capacitance,10)but is

negligible for the zero-biased capacitance where the carrier

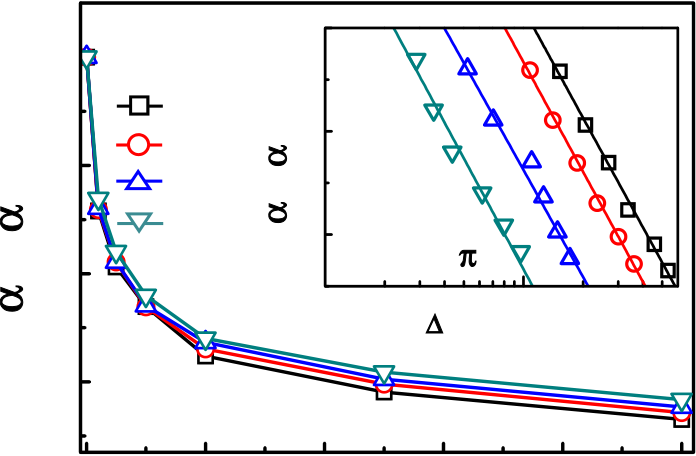
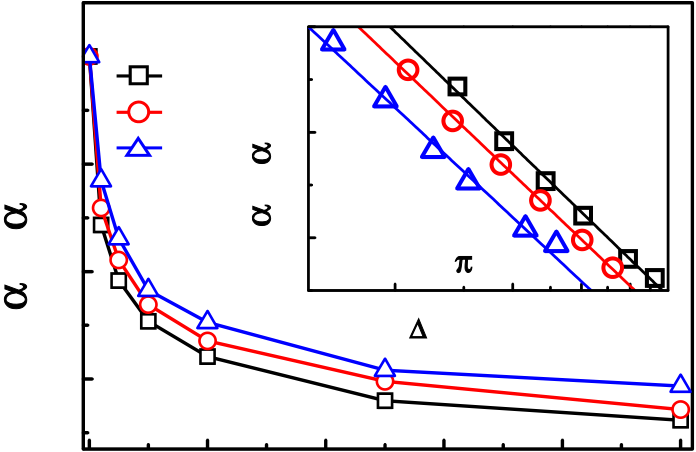
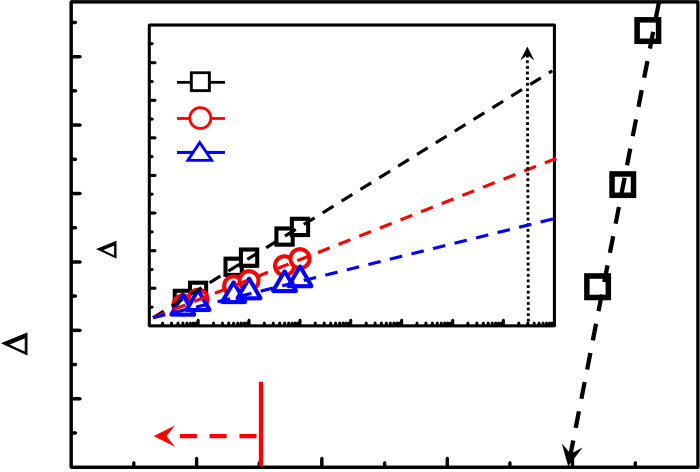
where K is the trapping efficiency as a function of the injected current density and the temperature, and the characteristic exponent n is a fraction. As a consequence,

injection ceases. the logarithmic dependence of the relative capacitance

To further investigate the stability of the La2O3 MIM capacitor under electrical stress, the CVS test was carried

variation on the injected charge is shown in the inset of Fig. 3. Moreover, the CVS conditions presented here exhibit

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| Jpn. J. Appl. Phys. 49 (2010) 04DB16 | | | | | | | | |  |  |  |  | **Stress Bias** | | **0.8** | | | | S.-H. Wu et al. |
| Δ**C/C(t=0) (%)** | **6** | Δ**C/C(t=0) (%)** | **8** | **Stress Bias** | | **10 year 10-year Degradation** | | | **-5** | α**(t)/**α**(t=0)** | **1.0** | **0** | **40 50** |
| **7** | **-5 V** | α**(t)/**α**(t=0)**   **0.6** | | **slope ~ -0.7** | | |
| **5** | **-4.6 V** | | **6.32%** | | | **0.8** |
| **6** |
| **-4.8 V** |
| **-4.4 V** | | **4.09%** | | |
| **5** |
| **-4.6 V** |
| **-4.2 V** | | **2.61%** | | |
| **4** | **4** |
| **3** |
| **3** | **2** | **0.6** | **0.4** | |
| **(-2/**π**)** | | |
| **1** | | | | | | |
| **10** | | | | **20**  **30**  Δ**D/D(t=0) (%)** | |
| **2** | **0**  **2**  **3**  **4**  **5**  **6**  **7**  **10**  **10**  **10**  **10**  **10**  **10**  **65-nm node Stress Time (s)** | | | | | **8 10** | **9**  **10** | **0.4** | **1000** |
| **1** |
| **below -1.5 V** | | | **-3.93 V** | | | | **200** | **400**  **600**  **Stress Time (s)** | | | | **800** |
| **0** | | **0** | **-1** | | **-2** **-3**  **Stress Bias (V)** | | | **-4** |

Fig. 4. (Color online) 10-year stability extraction of 10-nm La2O3 MIM

capacitors estimated by the relative capacitance variation.

Fig. 5. (Color online) Time dependence of the normalized quadratic

voltage coefficient of capacitance ½�ðtÞ=�ðt ¼ 0Þ� under CVS voltages of

�4:6 to �5 V.

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| a nearly linear relationship between Qinj and stress time | α**(t)/**α**(t=0)** | **1.0** | **0** | **Measurement** | | **0.8** | | | | **1000** |
| (not shown). The power law behavior of trapping proba- |
| **Frequency** | | | | | |
| bility brings about the slower increase in capacitance after | **0.8** | **50 kHz**   α**(t)/**α**(0)**   **0.6 100 kHz**  **200 kHz**  **500 kHz**  **0.4** | | | **slope ~ -0.7 (-2/**π**)** | | |
| long-term stress. Both the linear relationship between |
| ½�C=Cðt ¼ 0Þ� and ln Qinj and the saturation-like behavior mentioned above are similar to the flatband voltage shift of a |
| **0.6** |
| metal–oxide–semiconductor (MOS) capacitor under electri- |
| **1** | | | | **10**  Δ**D/D(t=0) (%)** | |
| cal stress that has been reported in many studies.27) |
| In considering the long-term stress behaviors of capaci- | **0.4** | **Stressed at -4.8V** | | | | | |
| tance, Fig. 4 depicts the 10-year stability extraction of a |
| **200** | **400**  **600**  **Stress Time (s)** | | | | **800** |
| fabricated 10-nm La2O3 MIM capacitor estimated by the |
| relative capacitance variation. It could be obtained from the |

extrapolated ½�C=Cðt ¼ 0Þ� versus stress time to 10 years,15) as shown in the inset of Fig. 4. The 10-year degradations of

10-nm La2O3 MIM capacitors with an 11.4 fF/mm2capaci-

tance are 6.32, 4.09, and 2.61% under CVSs of �4:6, �4:4, and �4:2 V, respectively. The operation voltage guarantee-ing 0% degradation for 10 years is extrapolated at �3:93 V. This proves that the long-term stability of the La2O3 MIM

capacitor is satisfactory for the sub-65 nm technology node,

whose operating voltage is smaller than 1.5 V.15)

The time dependence of �ðtÞ normalized to its initial value�ðt ¼ 0Þ under CVSs from �4:6 to �5 V is plotted in Fig. 5. It was found that ½�ðtÞ=�ðt ¼ 0Þ� decreases with increasing stress time for a given stress bias. In other words, CVS

improves the voltage linearity of the high-� La2O3 MIM

capacitor. This may be explained by the reduced carrier

mobility in the La2O3 dielectric due to the generation of

stress-induced trap states under CVS, thus leading to a

longer relaxation time of mobile charges.10)As mentioned

before, � is dominated by the free carrier polarization.

Furthermore, higher stress voltage causes greater damage

and more traps for the same stress time, and hence brings

about the larger changes in � compared with that of the

lower stress voltage condition. The inset of Fig. 5 shows the

dependence of ½�ðtÞ=�ðt ¼ 0Þ� on the relative variation in dielectric loss ½�D=Dðt ¼ 0Þ� during stress. The relative variation in dielectric loss caused by CVS with respect to its

initial values is acquired as

Dðt ¼ 0Þ ¼ D0ðtÞ � D0ðt ¼ 0Þ ; ð4Þ

where D0ðt ¼ 0Þ is the initial dielectric loss at zero bias. The relative variation in D of the La2O3 MIM capacitor under

CVS increases with stress time and voltage (not shown),

Fig. 6. (Color online) Time dependence of the normalized quadratic voltage coefficient of capacitance ½�ðtÞ=�ðt ¼ 0Þ� under a CVS of �4:8 V at various measurement frequencies.

similar to the trend of the relative variation in capacitance shown in Fig. 3. It is believed that the trap/detrap processes are responsible for the dielectric loss, and the increase in D under CVS is ascribed to the generation of stress-induced trap states.23) Furthermore, from the inset of Fig. 5, ½�ðtÞ=�ðt ¼ 0Þ� linearly decreases with a logarithmic in-crease in relative dielectric loss, and it maintains almost the same slope independent of the stress voltage. This linear relationship further verifies the relationship between the amount of trap generation, responsible for the dielectric loss, and the reduction of free carrier mobility, responsible for the voltage dependence of capacitance. In other words, stress-induced trap states reduce the free carrier mobility in the dielectric and therefore increase the free carrier relaxation time that decreases the � of MIM capacitors under CVS. Additionally, the time dependence of ½�ðtÞ=�ðt ¼ 0Þ� at various measurement frequencies under a CVS of �4:8 V is shown in Fig. 6, and the inset presents the dependence of ½�ðtÞ=�ðt ¼ 0Þ� on the relative variation in dielectric loss ½�D=Dðt ¼ 0Þ�. As the measurement frequency increases, the changes in ½�ðtÞ=�ðt ¼ 0Þ� become smaller. This is believed to be due to the smaller �ðt ¼ 0Þ at higher frequency. From the inset of Fig. 6, ½�ðtÞ=�ðt ¼ 0Þ� linearly decreases with a logarithmic increase in relative dielectric loss, and the slope is again independent of the measurement frequencies, and the same as that obtained in Fig. 5. In ref. 23, Takeda et al., showed that the voltage stress causes�-V curve flattening, corresponding to the decrease in �.

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| Jpn. J. Appl. Phys. 49 (2010) 04DB16 | S.-H. Wu et al. |

Meanwhile, Takeda et al. also found that changes in the frequency coefficient of capacitance (FCC) during the CVS test linearly depend on changes in D with a slope that agrees well with the value of 2=� predicted from the dielectric response model.28)As a result, one can derive that changes in � must vary linearly with changes in D as well. In this work, we further pointed out the unique relation measuring frequency and CVS voltage. The absolute value of ½�ðtÞ=�ðt ¼ 0Þ� � ln½�D=Dðt ¼ 0Þ�, independent of the of the slope between ½�ðtÞ=�ðt ¼ 0Þ� and ln½�D=Dðt ¼ 0Þ� is about 0.7, approximately equivalent to 2=�. However, the complete quantitative understanding of the slope is still under investigation.

Owing to the complex nature of defects generated during CVS, neutral and positively or negatively charged traps may be generated. The increase in the number of charged traps contributes to the dipole polarization and the increase in capacitance. The free carrier mobility, important for �, is reduced after CVS owing to the capture and emission processes in shallow traps and/or additional Coulomb scattering from the charged traps. The capture and emission processes also lead to dielectric loss, which also increases after CVS. In short, the changes in capacitance, dielectric loss, and � are all closely linked to the trap generation

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The stability of high-� La2O3 MIM capacitors under CVS has been investigated in this study for the first time. It was found that the capacitance degrades with stress, and the relative capacitance variation increases with a logarithmic increase in Qinj regardless of the stress biases. On the other hand, the normalized � decreases with a logarithmic increase in relative changes in D. Charge trapping contributes to the capacitance variation under CVS while the reduced carrier mobility due to the stress-induced traps is responsible for the reduction of �. Additionally, high stability of 10-year lifetime is achieved for a 10-nm La2O3 MIM capacitor with an 11.4 fF/mm2capacitance density. Therefore, the La-based high-� MIM capacitors are very promising passive compo-nents for RF and analog circuits demanding high precision of analog functions.

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