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Enhanced Reliability of Ferroelectric HfZrOx on

Semiconductor by Using Epitaxial

SiGe as Substrate

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***Abstract— As***  ***compared***  ***with***  ***Si***  ***as***  ***the***  ***substrate, ferroelectric (FE) HfZrOx with orthorhombic phase on Si0.56Ge0.44 substrate was found to demonstrate improved FE characteristics. Through the incorporation of Ge into the silicon substrate, remanent polarization (Pr) can be fur-ther enhanced by 58% magnitude to 15 µC/cm2. Moreover, devices on Si0.56Ge0.44 show significant reliability enhance-ment in terms of negligible Pr degradation up to 107cycles under* ±*4 MV/cm with 10-kHz bipolar stress and desirable retention up to 104s arising from smaller imprint effect against time at 85*◦*C. The major role of Ge introduction into the substrate is to suppress the formation of the interfacial layer (IL) between HfZrOx/substrate and further reinforcethe quality of the IL. The suboxide IL of the enhancedquality can be explained by the fact that it is too thin to trap charges while less vulnerable to defect generation due to stronger bonding with fewer oxygen vacancies. The results suggest that as the technology advances from Si into SiGe platform, HfZrOx-based devices possess more reliable ferroelectricity for metal–FE–semiconductor (MFS) gate-stack for the next-generation FeFET.***

***Index Terms— Fatigue, ferroelectric (FE), HfZrOx, imprint, interfacial layer (IL), reliability, retention, SiGe.***

I. INTRODUCTION   
**T** HE newly discovered HfO2-based ferroelectric (FE) material has received great interest for advanced mem-ory and logic devices because of its ferroelectricity even at

ultrathin thickness [1] and compatibility with very-large-scale integration (VLSI) technology [2]. To make FE-HfO2-based devices possible for practical applications, reliability is a major concern. According to the previous report, the relia-bility issues have been well explored and possible solutions

were proposed for metal–FE–metal (MFM) structures [3]. Nevertheless, FE-HfO2-based devices based on metal–FE–semiconductor (MFS) structure such as FeFET memory still encounters reliability issues in terms of undesirable cycling

endurance [4], which is primarily due to the degraded interface driven by charge trapping during the cycling operation [5].

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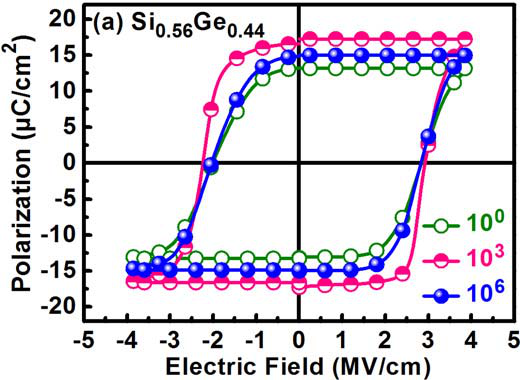
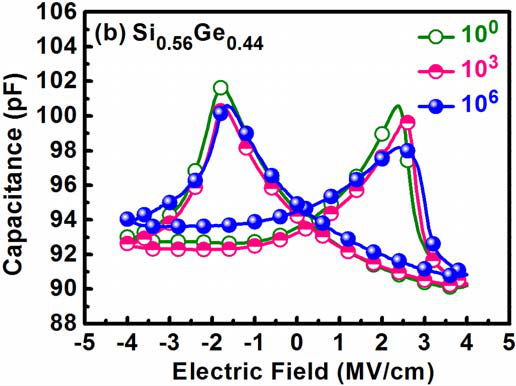
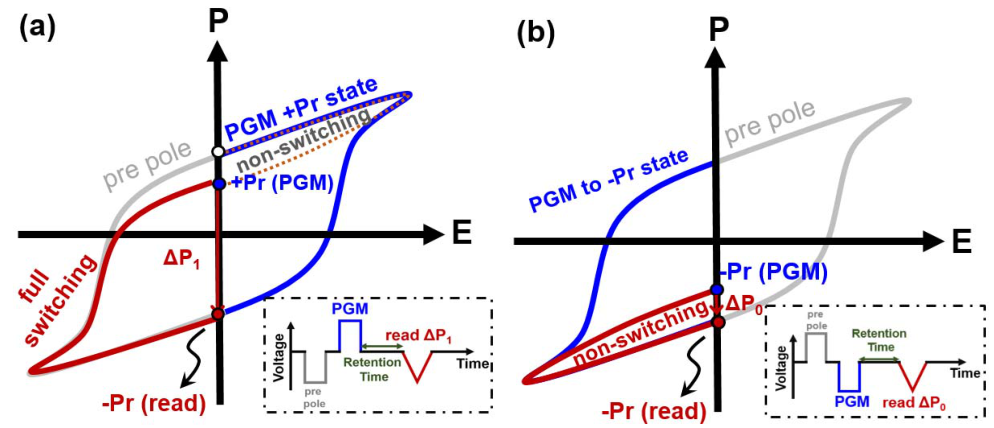
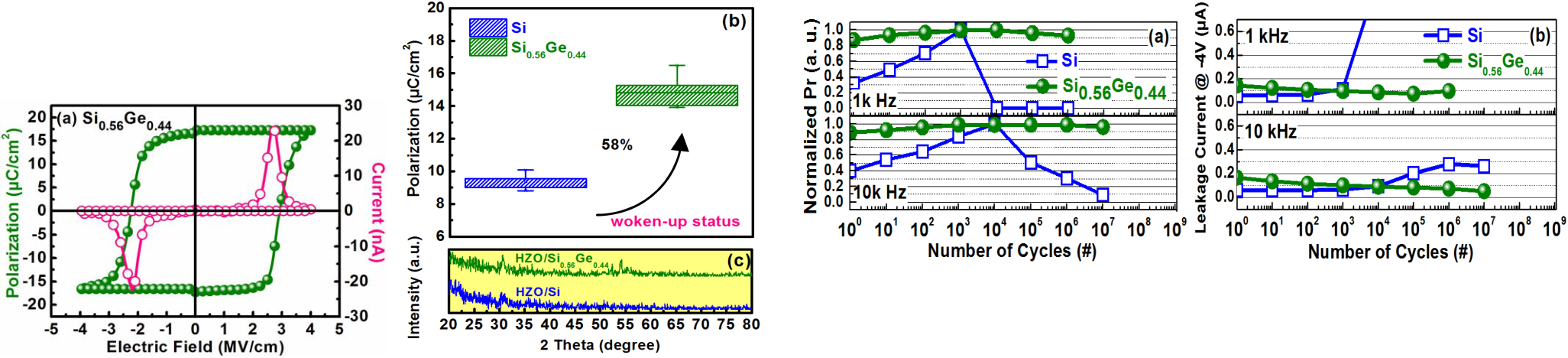
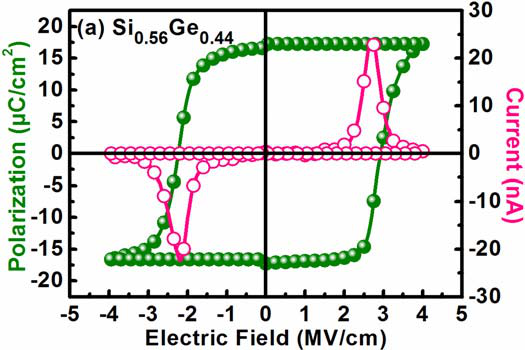
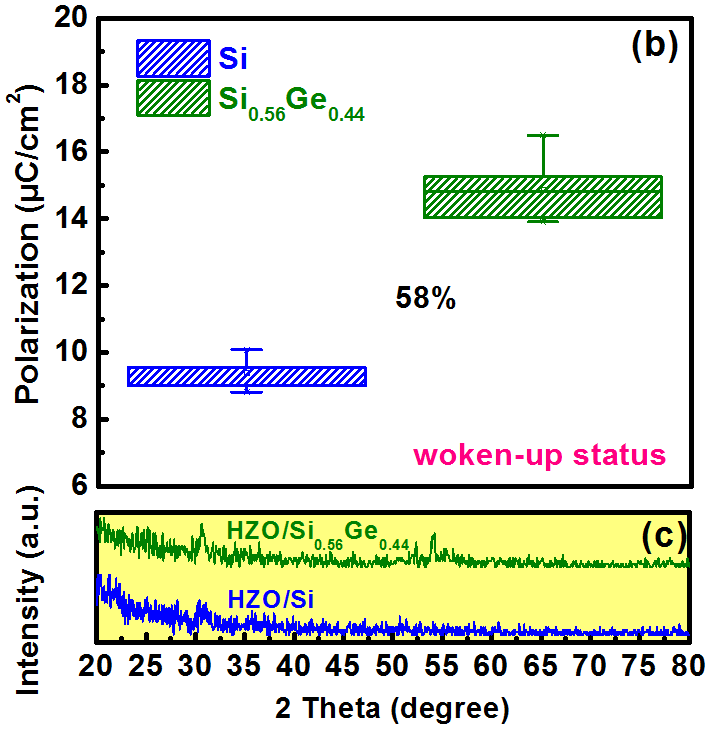
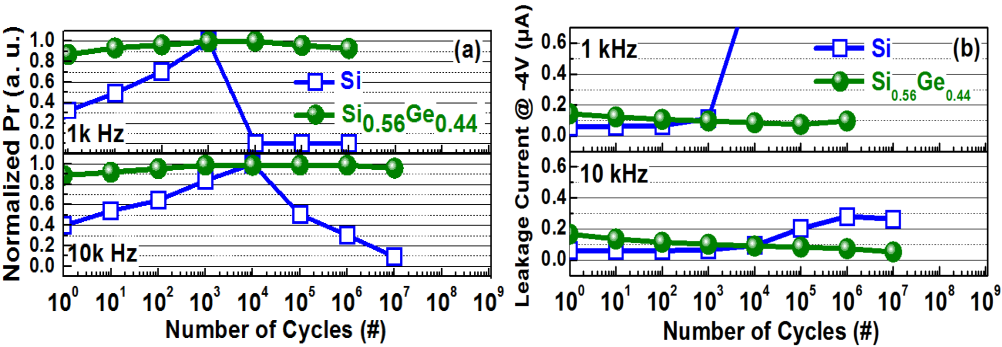
Therefore, several solutions were studied to achieve a robust FE-oxide gate-stack including inserting buffer layer [6] or replacing substrate material [7]. Although high-mobility chan-nel semiconductor Ge has been extensively studied for CMOS devices, the impact of introducing Ge into Si substrate on reliability characteristics of FE devices has been scarcely investigated. In this work, by using epitaxial Si0*.*56Ge0*.*44 film on Si substrate as the platform, based on MFS struc-ture, the reliability characteristics of FE HfZrO*x* (HZO) on Si0*.*56Ge0*.*44 were investigated. The core value of this work lies in two aspects: 1) bridging the understanding gap between FE-HZO on Si and Ge substrate and 2) pioneering the in-depth FE-HZO investigation on epitaxial SiGe film. The results indicate that as compared to conventional Si substrate, FE-HZO on Si0*.*56Ge0*.*44 corresponds to enhanced remanent polarization (*Pr)* and improved reliability in terms of more robust endurance up to 109cycles, better retention, and less imprint effect at 85◦C.

II. EXPERIMENT

The 15-nm SiGe thin film with Ge content of 44% was epitaxially grown on Si substrate. Then, 20-nm SiO2 was deposited on Si0*.*56Ge0*.*44 film by plasma-enhanced (PE) chem-ical vapor deposition process to prevent Ge atom out-diffusion from subsequent high-temperature annealing process. Next, P dopant was implanted into Si0*.*56Ge0*.*44 thin film with 15 keV/1015cm−3and then activated by 30-s RTA at 800◦C. After removing the SiO2 by dilute HF, PE-ALD HfZrO*x* of 10 nm with HfO2:ZrO2 = 1:1 cycle ratio was deposited on the n-type Si0*.*56Ge0*.*44 and *in situ* PE-ALD TiN of 30 nm was severed as the top electrode. Then, 500◦C-RTA in N2 ambient for 30 s was used to crystallize the HZO into orthorhombic phase. Finally, MFS capacitors were completed by patterning top electrode. The same substrate doping and MFS structure were also prepared on Si substrate for comparison. X-ray diffraction (XRD) was used to analyze the crystallinity of HZO while piezoresponse force microscopy (PFM), polarization–electric field (P–E), capacitance–electric field (C–E), and current–electric field (*I*–*E)* analyses were also carried out to confirm the ferroelectricity. In addition, the in-depth reliability characteristics including endurance, retention, and imprint effects were studied for HZO on Si and Si0*.*56Ge0*.*44 substrate. The endurance test was evaluated by applying bipolar ac stress (pulse train with ± 4 MV/cm and frequency from 1 to 10 kHz). The retention performance was characterized by switching and nonswitching reading processes with 4-MV/cm poling voltage.

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Fig. 3. as a function of cycling numbers with different stressing frequencies for Evolution of (a) leakage current at −4 V and (b) normalized Pr

devices on Si and Si0.56Ge0.44 substrates.

Fig. 1. on Si0.56Ge0.44. (b) Woken-up Pr dependence on Si and Si0.56Ge0.44 (a) P–E and I–E characteristics over ± 4 MV/cm for devices

substrates. (c) XRD pattern for HZO on Si and Si0.56Ge0.44 substrate.

Fig. 2. Cycling-dependent (a) P–E and (b) C–E curves with different numbers of 1-kHz fatigue pulse for devices on Si0.56Ge0.44.

In addition, transmission electron microscope (TEM), energy dispersive spectroscopy (EDS), and X-ray photoelectron spec-troscopy (XPS) were used to elucidate the mechanism of substrate-dependent reliability performance.

III. RESULTS AND DISCUSSION

A. Ferroelectricity of HfZrOx   
 Fig. 1(a) displays the *I*–*E* and *P*–*E* curves of HZO on Si0*.*56Ge0*.*44 by using bidirectional sweep over ±4 MV/cm and the electrical characteristics exhibit typical behavior of ferroelectricity. Note that both curves were obtained from Positive-Up-Negative-Down (PUND) method to achieve the intrinsic remanent polarization value without being influenced by leakage component. From *P*–*E* hysteresis, the coercive field (*Ec)* can be characterized by the current peak resulted from the polarization switching. The asymmetric *Ec* is due to a different work function for the top and bottom electrode. Furthermore, as compared to HZO on Si, *Pr* value for HZO on Si0*.*56Ge0*.*44 is enhanced by 58% as shown in Fig. 1(b). The enhanced *Pr* value for HZO on Si0*.*56Ge0*.*44 can be explained by better crystallinity of orthorhombic phase from XRD results shown in Fig. 1(c). The crystallinity can be quantized by full width at half maximum (FWHM) of the diffraction peak. The FWHM values of the orthorhombic phase peak corresponding to 30.5◦from Si and SiGe substrate are 1.10 and 0.51, respec-tively. The smaller value suggests a sharper peak and implies that HZO on SiGe substrate corresponds to better crystallinity with a larger grain size on SiGe substrate, leading to stronger ferroelectricity. It may be due to the smaller thermal expansion coefficients (*α)* as compared to Si counterpart [8], which makes higher mechanical stress on HZO during crystallization and stabilization of the FE phase.

B. Cycling-Dependent Electrical Behaviors

Fig. 2 shows the *P*–*E* and *C*–*E* characteristics of HZO on Si0*.*56Ge0*.*44 film by applying a course of continuous 1-kHz

Fig. 4. Hysteresis P–V loop and schematic of applied waveform for retention test showing the definition for (a) *Δ*P1 and (b) *Δ*P0.

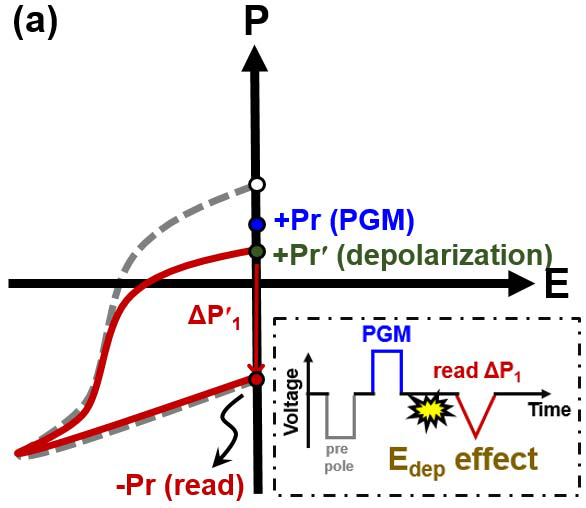
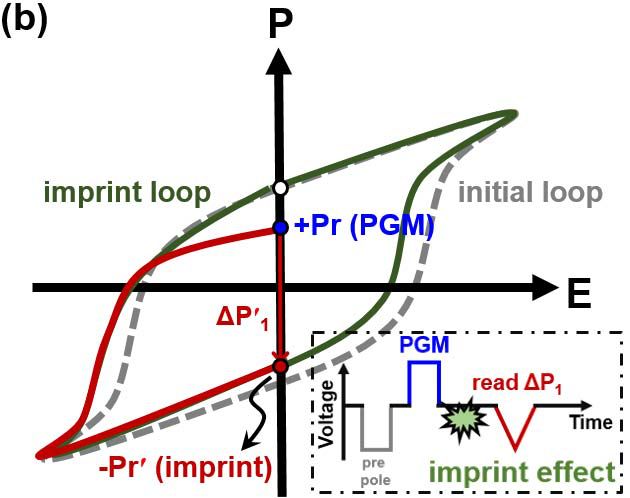
pulse up to 106cycles. As shown in Fig. 2(a), *Pr* initially increases to the maximum value at 103cycles and then it decreases as the cycles continue to 106cycles. The trend suggests that both wake-up and fatigue effects exist in HZO on Si0*.*56Ge0*.*44 film. Similar cycling-dependent butterfly-like *C*–*E* features are also observed in Fig. 2(b). Fig. 3 displays the evolution of leakage current (measured at −4 MV/cm) and *Pr* as a function of cycling number with different frequencies ranging from 1 to 10 kHz for HZO on Si and Si0*.*56Ge0*.*44. At 1 kHz, an abrupt leakage current increase is found for HZO on Si, which indicates that a large amount of oxygen vacancy (Vo)-related defects are generated and completely pin domain walls and/or make dielectric breakdown. In addition, the wake-up effect is dominant prior to dielectric breakdown. On the other hand, for HZO on Si0*.*56Ge0*.*44, slight wake-up and fatigue effect is observed without dielectric breakdown. As the frequency increases, although dielectric breakdown is no longer found for HZO on Si, there is still significant wake-up and fatigue effects. On the contrary, HZO on Si0*.*56Ge0*.*44 shows almost free from these issues up to 107cycles under 10-kHz fatigue frequency. In fact, the wake-up effect is highly dependent on defects in the FE film, especially near the interface between FE film and electrode [9]. Thus, it can be inferred that the interface between HZO/Si0*.*56Ge0*.*44 possess fewer Vo and/or better interfacial quality than that of HZO/Si.

C. Retention Performance   
 The retention measurements up to 104s were carried out at 25◦C and 85◦C. Prior to the measurement, devices were operated to woken-up state by applying 104cycles with a pulse frequency of 10 kHz. During the measurement, the reten-tion performance for*P*1 and*P*0 was evaluated where the definition of these two signals is shown in Fig. 4 which demonstrates the applied waveforms of retention measurement and the corresponding *P*–*V* loop. The retention of*P*1 can be measured by applying a positive program (PGM) voltage pulse of 4 V (4 MV/cm) to make the device at the +*Pr* state and

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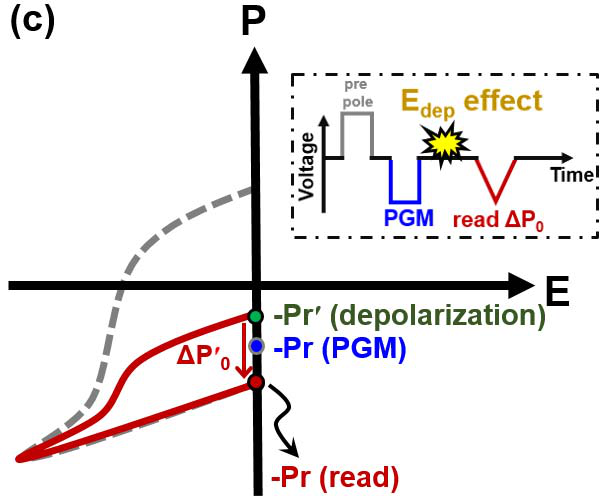
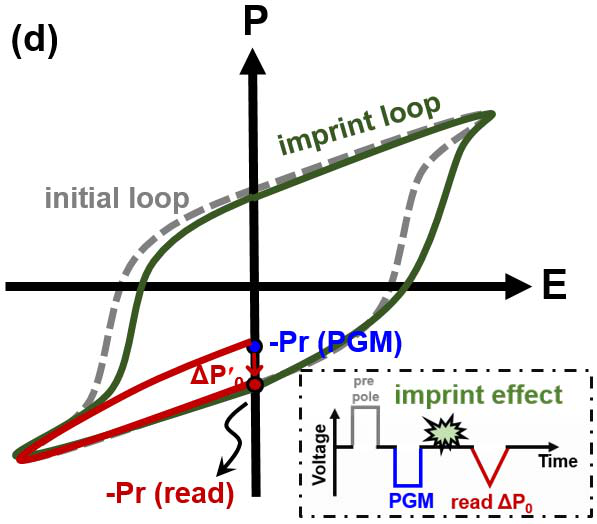
 

Fig. 5. Failure mechanism in reading *Δ*P1with sole (a) depolarization effect and (b) imprint effect. Failure mechanism in reading *Δ*P0 with sole (c) depolarization effect and (d) imprint effect.

then a negative voltage (−4 V) sweeping for a read operation is applied after a certain retention time. On the other hand, the measurement of retention of*P*0 is similar to that of

for PGM operation. From the definition,*P*1 consists of *P*1 except the negative voltage (−4 V, −4 MV/cm) sweeping

additional charge from dipole switching current since the neg-ative read operation alters the original polarization orientation. By contrast,*P*0 is composed of charge from displacement and leakage current without the dipole switching current (non-switching part) since the negative read operation does not alter its original polarization orientation, that is, the retention of *P*0 is to assess how polarization can be maintained with time without switching the dipole orientation while that of*P*1 is used to study how much polarization can be switched after certain retention time. Typically, the retention of*P*1 and*P*0 is affected by depolarization effect and imprint effect, and the latter is the root cause of the worse retention performance [10]. Detailed failure mechanism in reading*P*1 and*P*0 with sole depolarization field and imprint effect is illustrated in Fig. 5. For*P*1*,* with the sole undesirable *E*dep effect which would degrade +*Pr* (PGM) to +*Pr* (depolarization), as shown in Fig. 5(a), the polarization switching component would be reduced during the reading step and leads to*P*1, which is smaller than*P*1. On the other hand, with the sole undesirable imprint effect, *Ec* would shift toward a negative direction and makes a smaller negative polarization (absolute value) with retention time as the device is at +*Pr*. Therefore, as shown in Fig. 5(b), original −*Pr* (read) becomes −*Pr* (imprint) and consequently results in a smaller polarization switching component during the reading step, and thus*P*1, which is smaller than*P*1, is obtained. In brief,*P*1 can be employed to assess the retention performance by taking both *E*dep and imprint effect into consideration. For*P*0*,* with the sole undesirable *E*dep effect, which would degrade −*Pr* (read) to−*Pr* (depolarization), as shown in Fig. 5(c), the polarization switching component would become larger during the reading step and lead to*P*0, which is larger than*P*0. On the other hand, with the sole undesirable imprint effect, *Ec* would shift toward the positive direction but hardly affect −*Pr* (read) value

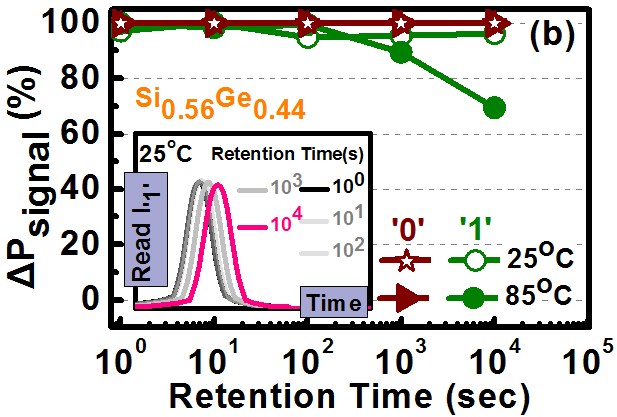
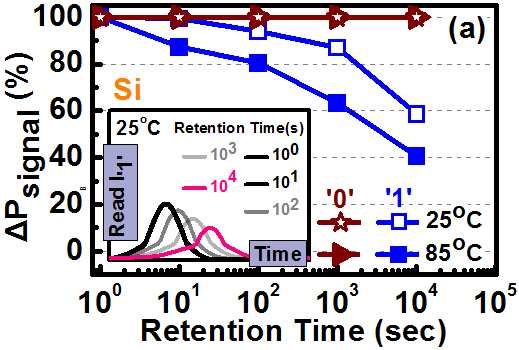


Fig. 6. Retention of *Δ*P0 and *Δ*P1 for HZO on (a) Si and (b) Si0.56Ge0.44. substrates for up to 104s at 25◦C and 85◦C. Inset is the current response with voltage sweeping time during read operation for different retention times.

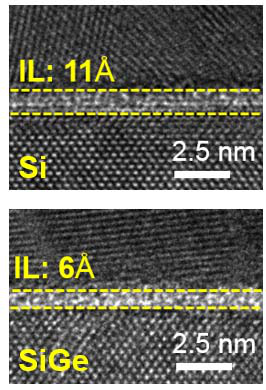
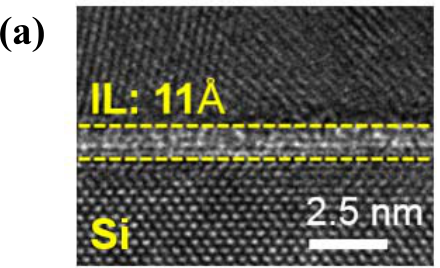
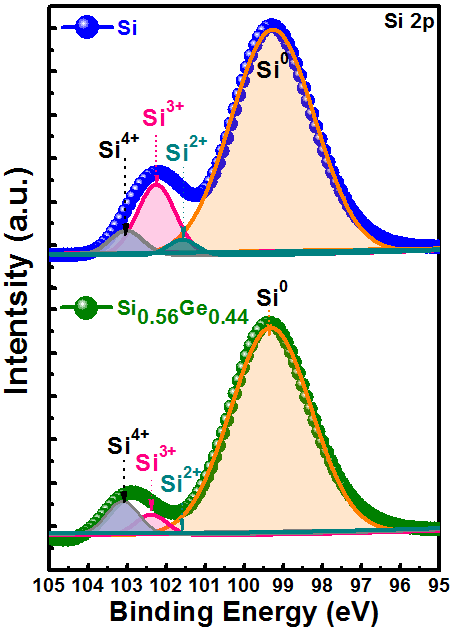
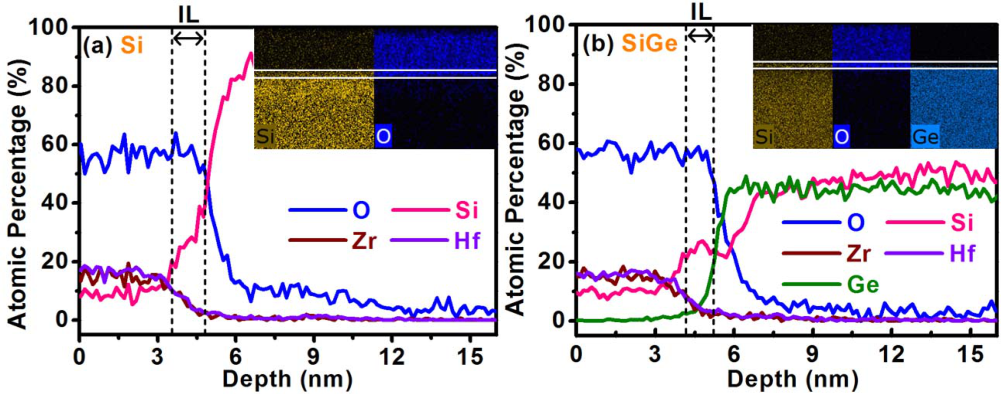
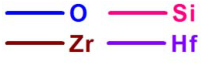
with a retention time as the device is at −*Pr*. As shown in Fig. 5(d), almost intact −*Pr* (read) value makes negligible polarization switching component during the reading step and an unchanged*P*0, that is,*P*0 cannot be used to reflect the retention degradation by imprint effect.

Fig. 6 shows the retention of*P*0 and*P*1 at 25◦C and 85◦C for devices on Si and Si0*.*56Ge0*.*44. For retention of*P*0, almost 100% polarization is maintained up to 104s retention time regardless of substrate type and measurement tempera-ture. The well-preserved*P*0 can be explained by the high immunity to depolarization effect due to the intrinsically high coercive field for HfO2-based FE material and the sufficient programming pulse to define its original polarization orienta-tion for retention measurement, which is helpful to prevent the memory state from unsaturated polarization [11]. On the other hand, for retention of*P*1, the reduction of switched polariza-tion with time occurs and much severer degradation is found for devices on Si than those on Si0*.*56Ge0*.*44. At 25◦C, almost 100% polarization can be switched for devices on Si0*.*56Ge0*.*44 at the retention time of 104s. However, at the same time, only ∼59% switched polarization can be observed for devices on Si. This much-degraded retention performance is caused by the more significant imprint effect as evidenced by the evolution of current with voltage sweeping time during read operation shown in the inset of Fig. 6. Visible current peak shift for devices on both substrates is observed, implying that the change of the coercive field arising from the occurrence of imprint effect. Since dipoles in an FE material would induce charge trapping at the interfacial layer**(**IL**)** and build internal filed across it, more pronounced current peak shift and reduced current response for devices on Si indicate more significant imprint effect. It also means that HZO on Si is more prone to dipole-induced charge trapping at IL between Si and HZO, which may be resulted from the inferior IL quality. At 85◦C, since the charge trapping effect becomes more pronounced, and therefore, devices on Si only show*P*1 of 41% at the retention time of 104s. On the contrary, those on Si0*.*56Ge0*.*44 still enjoy*P*1 of 70%.

D. Physical Analysis

It has been reported that wake-up and fatigue effect are, respectively, due to process-induced and cycling-induced charged defects that pin the domain walls [12], while reten-tion degradation for*P*1 is caused by imprint effect, which stems from the trapped charge from the internal dipole-induced electrical field [13]. The improved reliability by adopting Si0*.*56Ge0*.*44 can be explained by the thinner sub-oxide IL with higher quality as evidenced by the following

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interfacial oxide on Si0*.*56Ge0*.*44, which evidenced by EDS line

scan data shown in Fig. 7.

IV. CONCLUSION

Fig. 7. EDS line scan and element mapping for HZO on (a) Si and (b) Si0.56Ge0.44.

Fig. 8. (a) TEM image at interface of MFS for Si and Si0.56Ge0.44. (b) XPS Si 2p spectra for HZO on Si and Si0.56Ge0.44.

physical analyses. Fig. 7 shows the EDS line scan for HZO on Si and Si0*.*56Ge0*.*44, and thinner IL between HZO and substrate for Si0*.*56Ge0*.*44 can be estimated. From the depth profile for different elements, Ge shows an abrupt distribution near the HZO/ Si0*.*56Ge0*.*44 interface, whereas Si tails into IL layer. It can be explained that once O atoms diffuse into the substrate, Si is preferentially oxidized due to lower Gibbs free energy [14]. The absence of Ge–O bonding in interfacial oxide for Si0*.*56Ge0*.*44 sample is evidenced by element mapping as shown in the inset of Fig. 7. Further confirmation of the IL thickness is done by TEM analysis as shown in Fig. 8(a). The cross-sectional images reveal an IL of 11 and 6 Å, respectively, for Si and Si0*.*56Ge0*.*44. From the viewpoint of the capacitive voltage divider, given identical HZO thickness, thinner IL leads to smaller stress voltage across it. Typically, the IL is a defect-rich layer, a smaller voltage across it would suppress generation of cycling-induced defects. In addition, thinner IL is less possible to trap charges and thus corresponds to superior reliability. In addition to a smaller voltage drop across IL for Si0*.*56Ge0*.*44, IL with better quality is the other reason for the improved reliability and it is confirmed by the XPS Si 2p spectra of IL for Si and Si0*.*56Ge0*.*44 shown in Fig. 8(b). Compared to Si, SiO*x* component in IL of Si0*.*56Ge0*.*44 is also found but with much weaker intensity and higher oxidation state Si4+, implying higher oxide quality and more stoichiometric bonding with fewer Vo. Furthermore, the interfacial quality was also verified by extracting the interface state density (*D*it*)* from *C*–*V* and *G*–*V* typical MOS (lightly doped) for Si and Si0*.*56Ge0*.*44 (not shown). By adopting a single-frequency Hill–Coleman technique [15], the calculated *D*it values for HZO MFS capacitor with Si and Si0*.*56Ge0*.*44 substrate are 7.53 × 1012and 5.42×1012eV−1cm−2, respec-tively. About 28% decrease of *D*it for Si0*.*56Ge0*.*44 sample can be attributed to the barely Ge–O bonding coexistence in

Reliability of FE-HZO was evaluated on Si and Si0*.*56Ge0*.*44 substrate by MFS structure. For HZO on Si0*.*56Ge0*.*44, enhanced *Pr*, insignificant *Pr* degradation up to 107cycles under fatigue stress, desirable retention at woken-up state, and small imprint effect at 85◦C are obtained, much improved as compared to Si counterpart. The mechanism behind the improved characteristics was investigated by TEM, XPS, and element mapping. It is the thinner IL of (6 Å) with robust quality (fewer Vo) that makes less charge trapping and gener-ation during the test. The results indicate that by introducing Ge atom into Si substrate, reliability issues for HZO on of Si can be circumvented and it becomes very suitable for FeFET for advanced logic and memory applications. Further enhanced performance is expected as the platform migrates to Ge technology.

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