14-3   
 **Low Power 1T DRAM/NVM Versatile Memory Featuring Steep Sub-60-mV/decade**  **Operation, Fast 20-ns Speed, and Robust 85oC-Extrapolated 1016 Endurance**  Yu-Chien Chiu1, Chun-Hu Cheng2,\*, Chun-Yen Chang1,4, Min-Hung Lee3, Hsiao-Hsuan Hsu1,5 and Shiang-Shiou Yen1 1Dept. of Electronics Eng., National Chiao-Tung Univ., 2Dept. of Mechatronic Eng., & 3Inst. of Electro-Optical Science and Tech., National. Taiwan Normal Univ., 4Research Center for Applied Sciences, Academia Sinica, 5TQRPO, TSMC, Taiwan \*Tel: +886-02-77343514, E-mail: chcheng@ntnu.edu.tw

**Abstract**   
 In this work, we report a one-transistor (1T) versatile memory; the memory transistor characteristics achieve sub-60-mV/dec operation and considerably low off-state leakage of 10-15 A/μm at a supply voltage below 0.5V. The versatile memory features DRAM/NVM functions of large Δ*VT*window of 2.8V, fast 20-ns speed, 103s retention at 85oC, and long extrapolated 1016 endurance at 85oC, which show the potential for 3D memory application with severe requirement on both high density and low power consumption.

**Introduction**   
 The next-generation non-volatile memory (NVM) requires low operating voltage and fast speed to save switching power (PS) for high-density memory application. However, further VD and PS reductions in a MOSFET are limited by the fundamental transistor physics of 60 mV/decade subthreshold swing (*SS*). The steep *SS* property not only lowers the PS but also reduces the DC off-state leakage (*Ioff*), as shown in Fig. 1. One proposed solution is to adopt ferroelectric MOSFET with a steep *SS* lower than 60 mV/dec [1]. However, a weak ferroelectric polarization at a scaled thickness is not sufficient to prevent performance degradation on memory window, data retention and high-temperature endurance [2], [3]. In this work, we proposed a 1T versatile memory with combining storage mechanisms of ferroelectricity (FE) and charge trapping (CT) to simultaneously reach sub-60 mV/dec operation and fast write/erase speed for power saving. The memory behaviors improved by excellent subthreshold performance are also investigated.

**Device Fabrication**   
 The *p-*MOSFETs using ferroelectric HfZrO (HZO) and charge-trapped ZrSiO (ZSO) dielectrics were fabricated. A 3.5-nm dry oxide was grown on Si as buffer layer, followed by HZO (22.5nm) and ZSO (7nm) film deposition and 400oC annealing. Subsequently, the 3.5-nm SiO2 was covered as a tunnel oxide. After TaN gate patterning (W/L=100μm/10μm), self-aligned B+ was implanted and activated by 950oC.

**Results and Discussion**   
 Fig. 2 shows the orthorhombic crystallization of nanoscale FE-HZO responsible for ferro-domains switch. In Fig. 3, a *VT* shift (Δ*VT*) of 1.2 V, minimum *SS* (*SSmin*) of 58 mV/dec, and *Ion/Ioff* ratio of 108 are measured in FE-HZO MOSFET with ±6 V bias sweep. To further improve memory performance, we employ a versatile memory integrating a CT node (ZSO) into FE-HZO. As shown in Fig. 4, the extra aligned dipoles formed near ZSO/HZO interface add toward the polarization electric field at the same drive voltage. The well-behaved *ID-VD* and *ID-VG*are shown in Fig. 5 (inset: TEM image of gate stack). Under ±6 V bias sweep, a 3V *ΔVT* window, an ultralow *Ioff* of ~10-15A/μm, and a large *Ion/Ioff* ratio of >109 are achieved. The large Δ*VT* window with various gate bias (Fig. 6) due to strong polarization enhancement facilitates multi-level operation and high-temperature endurance.

In Fig. 7, the extracted *SSmin* of 54 mV/dec is critical for the reduction of standby power. From simulation results (Fig. 8)

fitted to *ID-VG* curve, the surface potential gain (dΨs/dVG) >1 is confirmed. The *m* factor possibly becomes smaller than 1 to reach low *SS* (<60mV/dec) when 1T versatile NVM shows a negative capacitance effect [1] and dΨs/dVG >1. As for low *SS* property (Fig. 9), the <60mV/dec *SS* are measured at a wide *VD* range from 0.1 to 0.5V, and also reveals the decrease of *SS* with downscaling of channel length. Fig. 10 presents max. Δ*VT* of 2.8V under 20 ns pulse and pulse-dependent Δ*VT* at ±4V. The Δ*VT* window triggered by faster 20ns speed (inset) shows very slight degradation in comparison with DC sweep mode, which verifies a reliable switching response between

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ferroelectric | domain | and | charge | trapping. | Although |

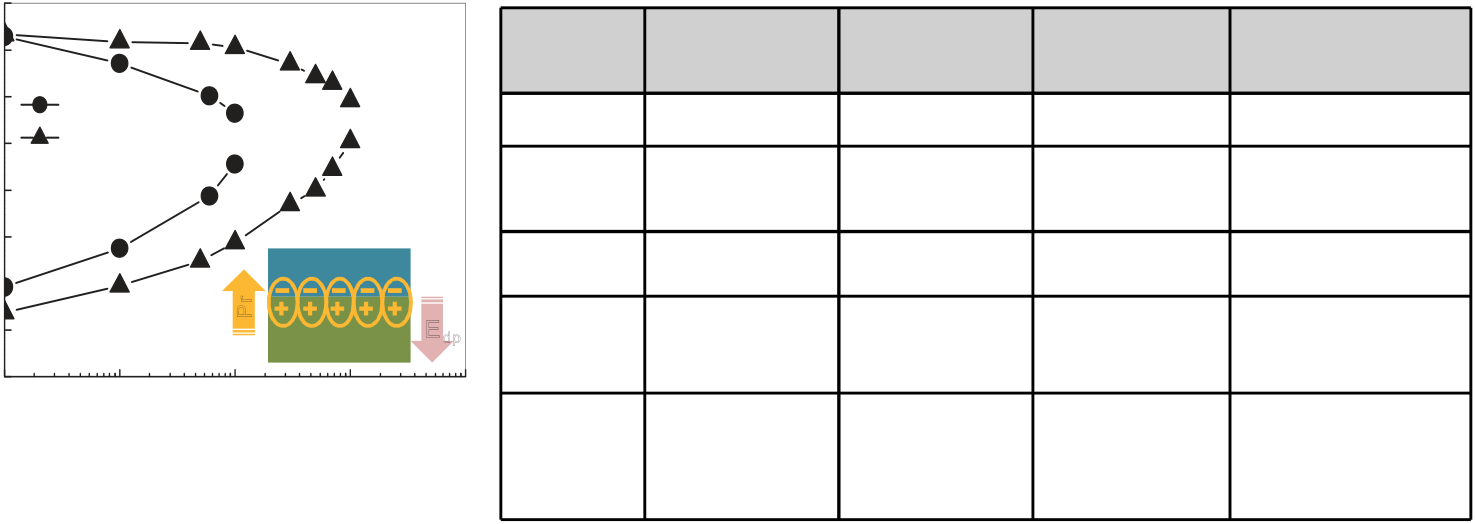
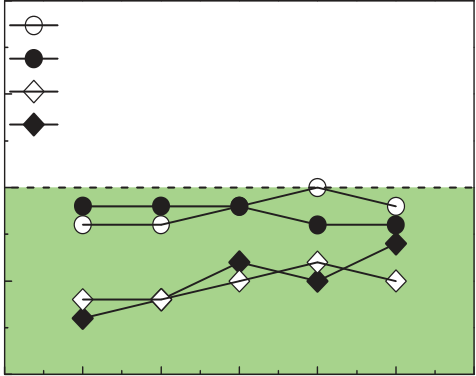
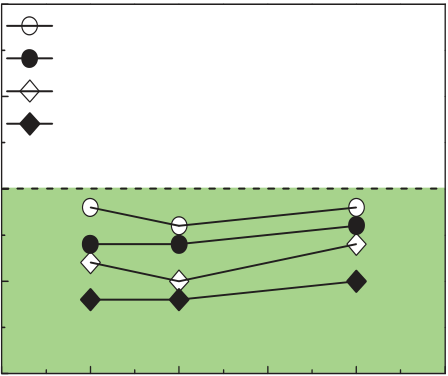
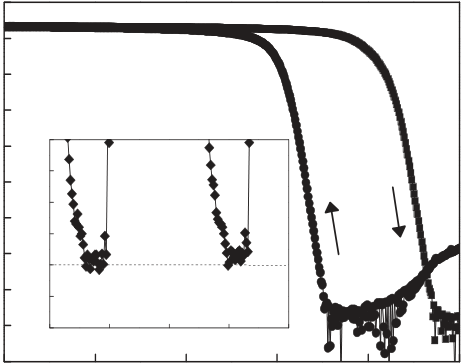
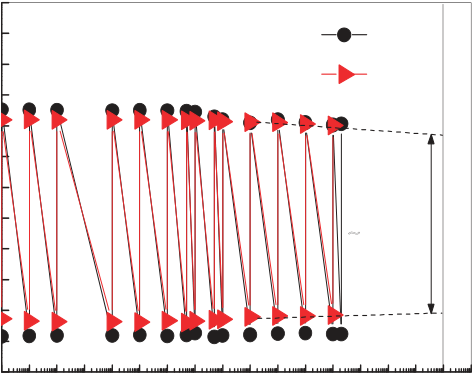
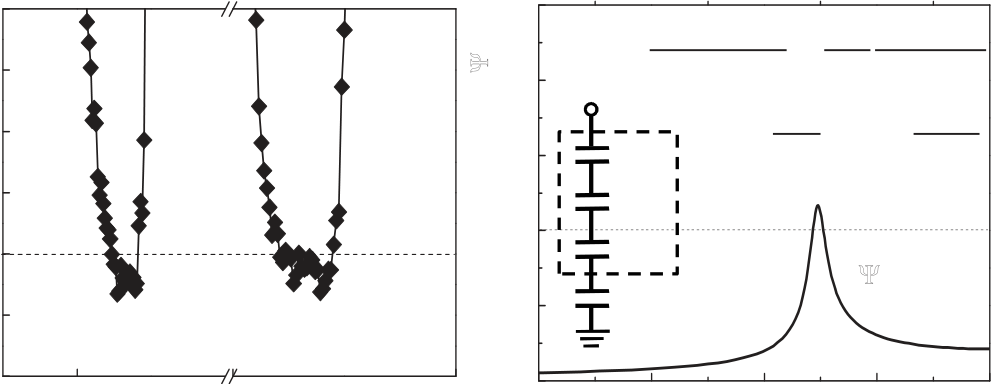
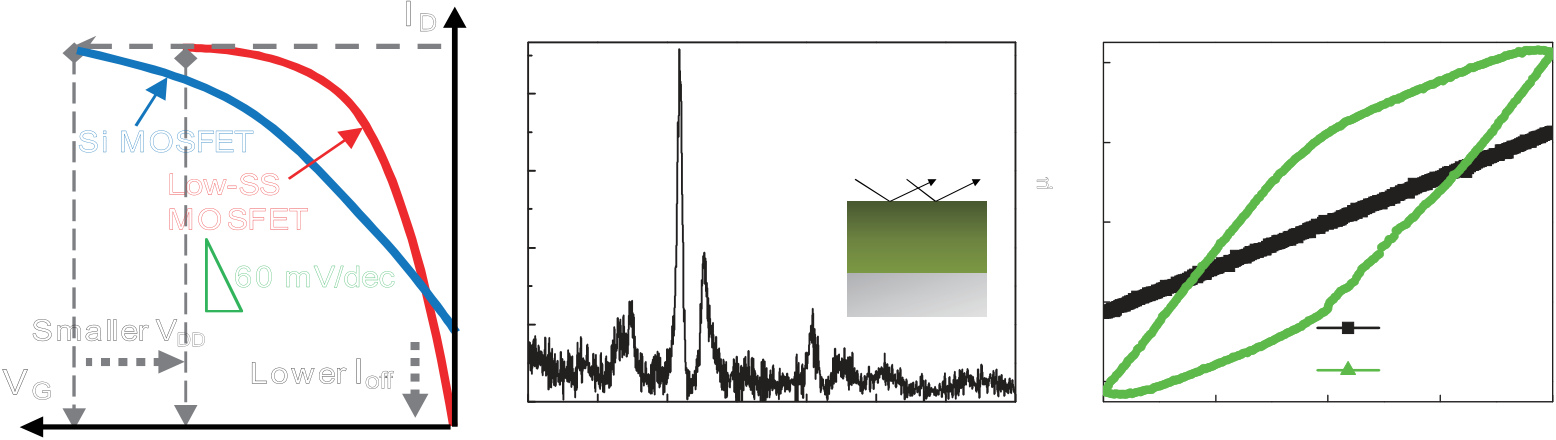
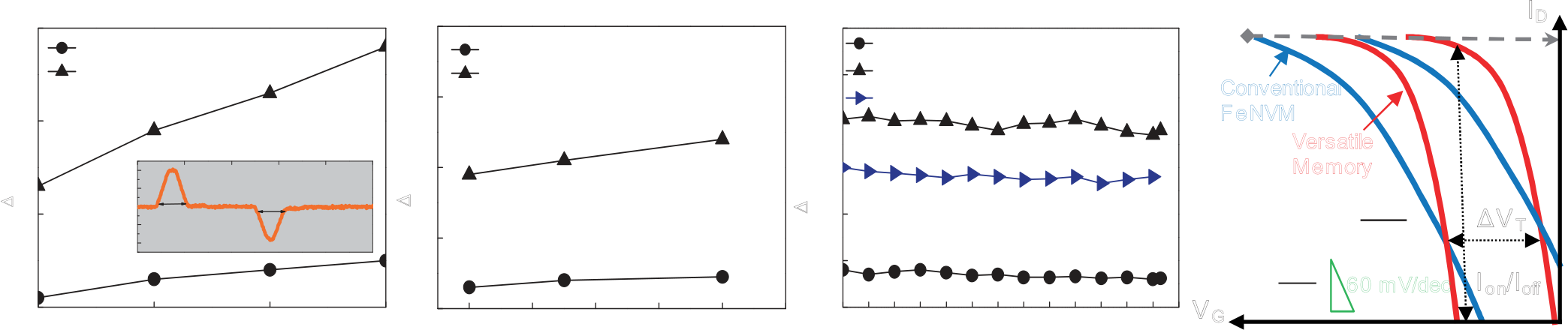
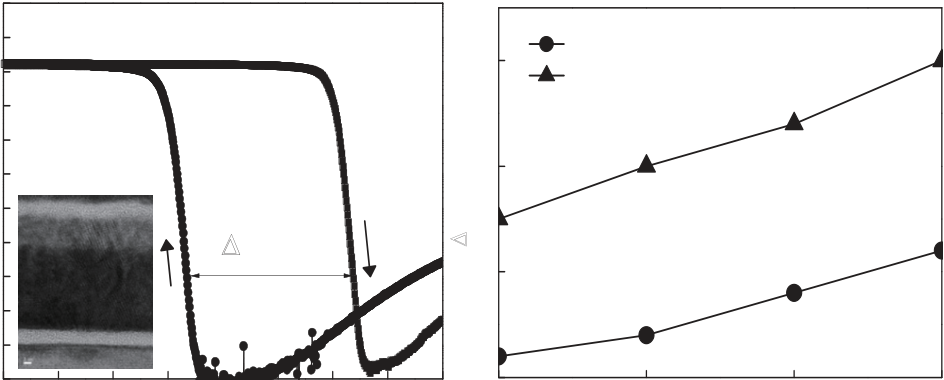
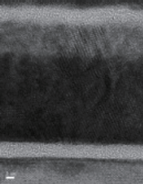
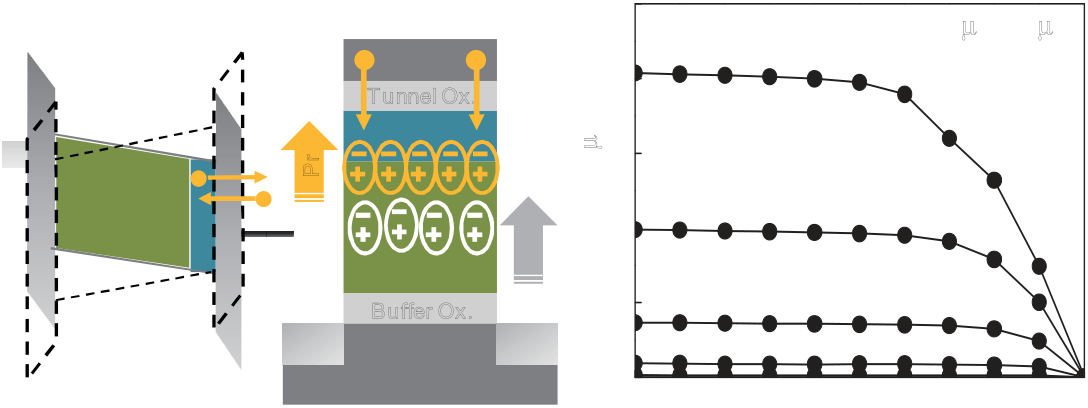
gate-injection charge tunneling may affect P/E speeds, faster pico-sec ferroelectric domain switching raises the speed up to ns level. Regarding sub-50ns P/E speeds, the measured Δ*VT* window of 1.9~2.1V are much larger than the saturated 0.3~0.4V of 1T FeNVM. Notably, a favorably low overdrive voltage (*VG-VT*) of <3V with a steep *SS* still provides a Δ*VT* window of 1.3V that is much better than that (0.9V Δ*VT* at ±4V) of FinFET DRAM with the best *SSmin* of 109 mV/dec [4].

We further evaluate the cycling endurance (Fig. 11). The versatile memory shows no significant degradation in Δ*VT* window with endurance beyond 1012 cycles even at higher 85oC. Since *VT* is sensitive to ferroelectric capacitance effect, a preferred read scheme adopting *Ion/Ioff* ratio to define sense margin is also tested. As shown in Fig. 12, sub-60mV/dec *SS* (*m*<1) can stabilize *Ion/Ioff* ratio (*Ioff* ∝10-VT/*SS*) and Δ*VT* due to low subthreshold leakage (*Isubth* ∝exp(VG/*m*VT)) to reach low drive voltage, uniform switch and long endurance. In Fig. 13, a stable and large *Ion/Ioff* ratio of ~107 is shown to exceed 1012 P/E cycles at 25oC. Furthermore, only slightly degraded *Ion/Ioff* (~106) is retained after extrapolation to 1016 cycles at 85oC. The extremely long endurance and high speed close to DRAM and sub-pJ switching energy like Flash NVM demonstrates the great potential for high-density & energy-efficient memory application. The high-temperature data retention is shown in Fig. 14. The improved retention of 103s at 85oC in versatile memory is superior to FeNVM, which can be ascribed to interface aligned dipoles, resisting depolarization field to delay retention time. Since the retention behavior is dominated by slow charge tunneling in CT layer, a long retention is expected by increasing ZSO thickness to enhance ferroelectric polarization stability. Table I summarizes memory characteristics of advanced 1T DRAM and NVMs. 1T versatile memory offers the competitive performance on low-driving voltage, steep *SS*, large Δ*VT* window at fast ns speed and robust 85oC endurance.

**Conclusions**   
 Steep 54-mV/dec *SS*, large 2.8V Δ*VT*, fast 20-ns speed, and stable endurance>1012 cycling at 85oC are achieved in versatile memory combining with CT and FE mechanisms.

**References**   
[1]A. I. Khan *et al,IEDM Tech. Dig.*, 2011, p. 255. [2]. J. Muller *et al*, *Symp. on VLSI Dig.,* 2012, p. 25. [3] C. H. Cheng *et al*, *IEEE EDL*,vol. 35, p. 138, 2014. [4] D. I. Moon *et al*, *IEEE EDL*,vol. 35, p. 1236, 2014.

T184978-4-86348-501-3 2015 Symposium on VLSI Technology Digest of Technical Papers



I D **-3**

**10**

**(a)**  **O**  **c-HfZrO**  **40**  **(b)**

Si MOSFET   
 **(Orthorhomic)**

GI-XRD   
 **20**   
 **10**  
 **-5**  **+6V/-6V sweep,**

**VD= -0.2 V**  **2) Polarization(**μ**C/cm**   
 **Intensity (a.u.)**   
 **Abs(ID) (A)**   
Low-SS **10** **-7**  **100**

MOSFET **O**  HfZrO **0**

**-9**   
 **90**

**80**

**SS (mV/dec)** 60 mV/dec **O**  **O**  Si Sub. **-20**  **10**  **70**

**60**

Smaller VDD **O**

**O**  **HfO2**  **10**  
 **-11**

**50 58 mV/dec**  **59mV/dec**

VG Lower Ioff

**10**  **20**  **30**

**2 Theta (degree)**   
 **40**  **50**  **60**  **70**  **80**  
 **-40**

**-4** **-2**

**E (MV/cm)**   
 **0**  
  **Ferro-HfZrO**

**2**  **4**  **10**  
 **-13**

**-4**   
 **40-1.0**

**-3**  
**-0.5**

**VG (V)**   
**0.0**

**-2**

**VG (V)**   
**0.5**

**-1**   
**1.0**

**0**  **1**

Fig. 1 Schematic *ID-VG* of Si MOSFET

and low-*SS*  MOSFET. The sub-  
 Fig. 2(a) Orthorhombic phases were measured by GI-XRD in ferro-HfZrO film.

(b) Polarization-electric field (P-E) loop. Such hysteresis loop observed in Fig.

FeNVM under ±6 V sweep. Extracted   
3 *ID-VG* characteristic of HZO

60mV/dec operation can

overdrive (*VG-VT*) andoff-state current.

lower gate HfZrO film can beinterpretedas the existenceof ferroelectric domains.

**150**

**(a)**  **W/L= 100**μ**m /10**μ**m**  **10-3 (b)**  **+6V/-6Vsweep,**   
 *SSmin* is about 58 mV/dec.

**FeNVM**

TaN **120**  **VG=0~ -1V**  **VD= -0.2 V**  **3**  **Versatile Memory**

Tunnel Ox. **-5**

**10**

**Abs. (ID)(**μ**A)**   
 **Abs. (ID) (A)**   
CT-ZSO **90**  **DC sweep**

Si Ferro- **10**

**-7**  **2**

Pr

Δ**VT (V)** HfZrO

TaN

FE-HZO

Buffer Ox.   
 **60**

**30**

**10**   
**10**

**-11**  
**-9**  ZSO (CT)

HZO (FE)   
 Δ**VT~3V**  **1**  Pr **Surface Potential Gain, d**Ψ**s/dVG** Δ**VT (V) Abs. (ID)(A))**   
Buffer Ox. Tunnel Ox. p+ p+

Si **0**

**-2.0** **-1.6** **-1.2**

**VD (V)**  
 **-0.8** **-0.4**  **0.0 10**

**-13**

**-5** **-4** **-3** **-2**

**VG (V)**  
**-1**  **0**  **1**  **2**  **3**   
 **0**

**3**  **4**  **VG (V)**  **5**  **6**

Fig. 4 Schematic device structure of 1T Fig. 5(a) *ID-VD* and (b) *ID-VG* characteristics of versatile memory. The low *Ioff* of Fig. 6 *ΔVT* as a function of DC

versatile memory with enhanced ~10-13A (10-15A/μm), large *Ion/Ioff* ratio of >109, and max. Δ*VT* of 3V can be sweep voltage from ±3V to ±6V.

ferrelectricpolarization byCT node. simutanouslyobtained. The inset shows TEMimage of device structure.

**100**  **2.5**  **70**  **70**

**90**

**80**   
 **6V to -6V**  
 **-6V to 6V**

**2.0**

**1.5**  
 �� =

VG

CCT  
 ∂(log10 ID ) = ∂VG

� = ∂VG∂φS= 1 +  
 ∂ log10 ID  
 ∂φS

Cins,eq   
CS **65**   
 **FeNVM (Forward)**

**FeNVM (Reverse)**

**Versatile Memory (Forward)**

**Versatile Memory (Reverse)**   
 **(a)**

**65**   
 **FeNVM (Forward)**

**FeNVM (Reverse)**

**Versatile Memory (Forward)**

**Versatile Memory (Reverse)**   
 **(b)**

**SSmin (mV/dec)**  **SSmin (mV/dec)** Δ**VT (V)**   
**SS (mV/dec)** Δ**VT (V) Abs. (ID)(A)**   
 **70**

**1.0**  CFE Cins,eq **60**  **60**

**60**  Cox

**d**Ψ**s/dVG > 1**  **55**  **55**

**50**

**54 mV/dec**  **54 mV/dec**  **0.5**  Cs

**40**  **0.0**  **50**  **50**

**-2**

**VG (V)**  **1**  **2** **-4** **-3**

**VG (V)**  
**-2** **-1**  **0**  **0.0** **-0.1** **-0.2**

**VD (V)**  
 **-0.3** **-0.4** **-0.5** **-0.6**  **0**  **5**

**Channel Length (**μ**m)**   
 **10**  **15**  **20**  **25**

Fig. 7 *SS*  characteristics of 1T Fig. 8 Surface potential gain versus gate Fig. 9 *SS* dependence on (a) *VD* and (b) channel length for 1T FeNVM and

versatile memory under ±6 V DC voltage. FE-HZO may result in a sub- versatile memory. The *SS* becomes smaller at lower overdrive votlage and

sweep.

**3**   
 60mV/dec *SS* by negative capacitance effect.

**4**  **3.0**  gate length that have great potential fordevicescalingin 3D memory. ID

**FeNVM**  **(a)**  **FeNVM**  **(b)**  **FeNVM @25 oC**  **P/E: +4V/-4V@20ns**

**Versatile Memory**  **Versatile Memory**  **2.5**  **Versatile Memory @25 oC**

**@20ns pulse**  **3**  **Versatile Memory @85 oC**  Conventional

**2**  **P/E: +4V/-4V**  **2.0**  FeNVM

**Time (ns)**  Versatile

**0**  **50**  **100**  **150**  **200**  **250**

**4**  **2**  **1.5**  Memory

**Voltage (V)**   
 **2**  **20ns**

**1** **-2**

**-4**   
**0**

**20ns**

**20ns Pulse**  **1**  **1.0** �subth ∝ exp( VG�VT) ΔV T

**0.5**

**0**

**3**  **4**  **5**  **6**   
 **0**

**20**  **40**  **60**  **80**  **100**  **120**   
 **0.0**

**10**   
 **0**

**10**   
 **2**

**10**   
 **4**

**10**   
 **6**

**10**   
 **8**

**10**   
 **10**

**10**  **12**  VG  
 � = ∂VG

∂φS 60 mV/dec Ion/Ioff

**P/E Voltage**  **P/E pulse speed(ns)**  **Number of P/E cycles**  Fig. 12 Schematic transfer

Fig. 10 Δ*VT* as the function of (a) P/E voltage and (b) pulse speed. Various P/E Fig. 11 Δ*VT* versus P/E cycles with ±4 characteristics of FeNVM and versatile

voltages (≤ 6V) and speeds (≤100 ns) were tested and verified in 1T FeNVM V P/E voltages at a 20ns speed. No memory. Sub-60mV/dec *SS* (*m*<1) and

and versatile memory devices. The fastest 20ns pulse (inset) was employed in significant degradation is observed up low subthreshold leakage can stabilize

endurancecyclingtest.

**-1** **-4**  to 1012cyclesevenat 85oC. *Ion/Ioff* ratio and Δ*VT* window.

**10**  **10**

**P/E= +4V/-4V @ 20ns**  **25 oC**  **@ 85 oC**  **1T**  **FinFET**  **HfSiO**  **HfZrO**  **Versatile**

**-3**

**10**  **85 oC** **-6**  **Memory**  **DRAM** [4] **FeNVM**[2] **FeNVM**  **Memory**

**10**  
 **-5**   
 **10**

**Versatile Memory**   
**FeNVM**

Speed 50ns 100ns <20ns 20ns

**10**  
 **-7**

**on/off ratio**

**6**   
 **10**  
 **-8**

ΔVT 0.9V@±4 V

@+4V/-6 V   
 0.8V 0.3V@±4 V

0.5V@±6 V   
 1.9V@±4 V

2.8V@±6 V

**-9** ∼**10**

**10**

**10** **-10**  CT-ZSO *SSmin*  109 mV/dec 58 mV/dec 54 mV/dec

**-11**

**10**

Pr

**10**  
 **-13**

**10 0 10 2 10 4 10 6 10 8 10 10 10 12 10 14 10 16**  **10**  
 **-12**

**10**   
 **0**

**10**   
 **1**

**10**   
 **2**   
 FE-HZO

**10**   
 **3**   
 Edp

**10**   
 **4**   
 Retention 104s @125oC

(ΔVT ~ 0.1V) (ΔVT~0.6V)   
 105s @25oC 102s @85oC

(*Ion/Ioff* <10)   
 103s @85oC

(*Ion/Ioff* <10)

Fig. 13 25oC- and 85oC-endurance of 1T

versatile memory. An On/off ratio of ~106is   
**Number of P/E cycles**

Fig. 14 85oC retention of 1T FeNVM

and versatile   
 **Time(sec)**

memory. CT node   
 Endurance

@25, 85oC   
 2×1012@25oC

(ΔVT ~ 0.8V) (ΔVT~0.5V)   
 104@25oC   
 >1012@25oC

(*Ion/Ioff* ~106)

(ΔVT ~0.3V)   
 >1012@25, 85oC

(*Ion/Ioff* ~106-107)

(ΔVT ~1.5-1.8V)

still reached under extrapolated 1016cycles weakens *Edp* in FE-HZO layer and

at 85oC. extendsretentionwindow to 103s. Table I Comparisonof advanced1T FinFET DRAMand1T NVMs.

2015 Symposium on VLSI Technology Digest of Technical Papers T185