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Program/Erase Cycling Degradation Mechanism of HfO2-based FeFET Memory Devices

Binjian Zeng, Min Liao, Jiajia Liao, Wenwu Xiao, Qiangxiang Peng, Shuaizhi Zheng, and Yichun Zhou

***Abstract*—The mechanism of memory window (*MW*) degradation of Hf0.5Zr0.5O2-based ferroelectric field effect transistors (FeFETs) with program/erase (P/E) cycling is investigated. Firstly, P/E cycling properties of the FeFETs are characterized at the different cycling voltages. Then the midgap voltage method is proposed to address the underlying drivers for threshold voltage shift and *MW* degradation by separating the effects of oxide-trapped charges and interface-trapped charges. The mechanism for the different threshold voltage evolutions between programed and erased states during P/E cycling is revealed. Moreover, the amount of *MW* degradation is nearly equal to the difference of midgap voltage shift values between programed and erased states, and the interface trap generation contributes to the midgap voltage shift.**

***Index Terms*—HfO2-based FeFET, endurance degradation, midgap voltage, oxide charge trapping, interface trap generation**

I.INTRODUCTION   
F ERROELECTRIC field effect transistor (FeFET) memory is one of the most promising emerging non-volatile memories, with the sign of non-destructive readout, low power consumption, fast write/read speed and Flash-like structure [1]. Recent demonstrations of aggressively scaled planar FeFET and 3D FeFET with HfO2-based ferroelectric thin film (FE-HfO2) have sparked the implementation for embedded and mass storage applications due to the excellent CMOS compatibility, high scalability, and mature manufacturability [2]-[4].

Nevertheless, one potential issue for HfO2-based FeFET memory is its limited endurance, i.e. the memory window (*MW*) degrading with program/erase (P/E) cycling[5]-[9]. Due to the continuity of electric displacement field, ferroelectric polarization of FE-HfO2 exerts significant electrical field stress on the interface between FE-HfO2 and silicon, which causes severe charge trapping and trap generation [7]. Most works indicated charge trapping is the dominant factor or main driver for the *MW* degradation [5], [7], [10]-[13], where *MW* is the difference of threshold voltage (*VTH*) values between programed

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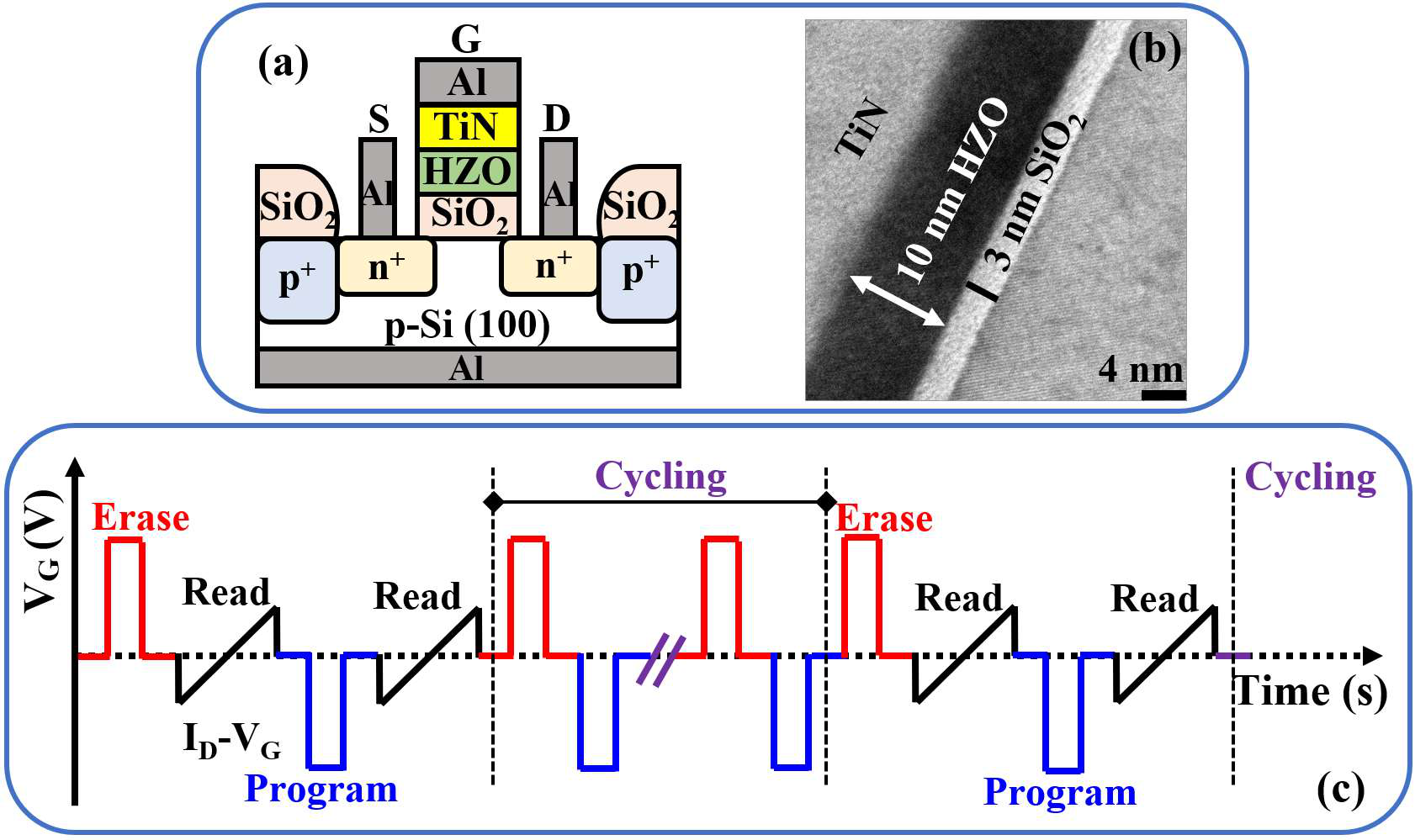


Fig. 1. (a) Schematic of the fabricated FeFETs. (b) Cross-sectional TEM image of the gate structure of the FeFET. (c) Test sequences for endurance measurement.

and erased states. For example, Yurchuk et al. identified that the wear-out of the interface between FE-HfO2 and silicon is responsible for the *MW* degradation, driven by charge trapping upon the bipolar P/E cycling [5]. Lately, from the point view of P/E read current ratio (the other expression for *MW*), Gong et al. found that both charge trapping in the gate stack and generation of interface traps (including border traps) contribute to the endurance failure [6]. But a more comprehensive and clear understanding of the evolution of *MW* closure is required for practical engineering applications, such as the respective effects of charge trapping and interface trap generation, and the different *VTH* evolutions between programed and erased states with P/E cycling [5], [6], [8]-[10].

Inspired by the significant achievements in clarifying the *VTH* shift of MOSFETs and revealing the P/E cycling degradation mechanism of Flash memories for practical engineering applications [14]-[18], the midgap voltage method of separating the oxide-trapped charges and interface-trapped charges is employed to clarify their individual contributions to *VTH* shift and *MW* degradation of Hf0.5Zr0.5O2-based FeFETs in this work.

II.EXPERIMENTS

The n-channel FeFETs with a TiN/Hf0.5Zr0.5O2/SiO2 gate stack were fabricated using a gate last process, schematically shown in Fig. 1(a). Following the formation of source (S)/drain (D), a 3-nm-thick SiO2 insulator layer was grown on chemically cleaned active area by dry oxidation. Afterward, a 10-nm-thick Hf0.5Zr0.5O2 layer was formed by alternately depositing Hf and

|  |  |  |  |  |
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| Zr | precursors through | ALD process. | Annealing | for |

crystallization was performed at 600oC for 30 s in N2 following the formation of TiN gate electrodes. After opening contact holes at S/D region, the contact was formed by Al metal deposition and patterning. Finally, the devices were annealed at 400oC for improving the S/D contacts. The gate length (*L*) and

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width (*W*) of the fabricated devices are 2 μm and 15 μm, respectively. Besides, thicknesses of the thin films integrated into the gate structure were confirmed by transmission electron microscopy (TEM), shown in Fig. 1(b).

The test sequence used for endurance measurement is shown in Fig. 1(c). P/E pulse is first applied to the gate of FeFET, and read operation is performed using *ID-VG* sweep (*VD* =0.1 V) to sense *VTH*. In this work, *VTH*is extracted by the current-to-square-root-of-the-transconductance ratio (CsrTR) method [19], and *MW* is defined as the difference of *VTH* values between programed and erased states in this work. Then, *MW* is tested again after a certain number of alternative P/E pulses.

III.RESULTS AND DISCUSSION

P/E cycling characteristics of the fabricated FeFETs at different cycling voltages are investigated. The *ID–VG* evolutions with +/-4.2 V/100 ns, +/-4.85 V/100 ns and +/-5.5 V/100 ns cycling are shown in Figs. 2(a), (b) and (c), respectively. Clearly, the *MW* decreases with P/E cycling, and the amounts of *ID–VG*curvesshifts in erased states are different from those in programed states, leading to an asymmetry closure of *MW,* which are summarized as the variation of *VTH* values (*VTH*) in Fig. 2(d). Meanwhile, the slopes of all *ID-VG* curves degrade with P/E cycling. The slopes degradations are indicated by the variation of subthreshold swing (*SS*) values, as shown in Fig. 2(e). It is found that the *SS* values in programed states are nearly same to those in erased states, suggesting the nearly same amounts of generated interface traps (*Nit*) in the both states according to Eq. (1), [16], [20]

∆𝑆𝑆 = ∆����� �� �� (1) ���∅�  
where *k* is the Boltzmann constant, *T* is the absolute temperature, *CFI* is the total capacitance of gate stack, and *F*is the fermi potential. The larger*SS* values under higher P/E cycling voltage would be the result of more interface traps generated.

Based on the device physics of FeFETs [21]-[22], the change of *VTH* compared to initial state (i.e. *VTH*) can be expressed as

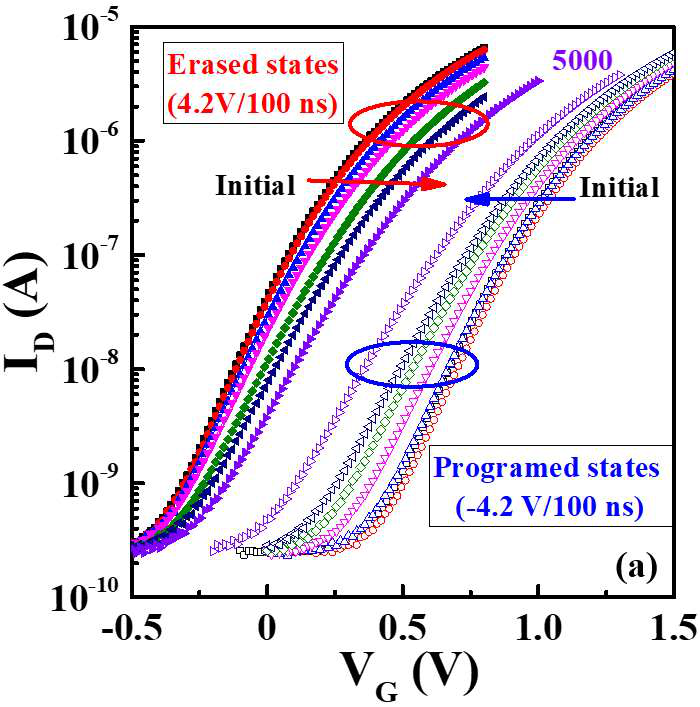
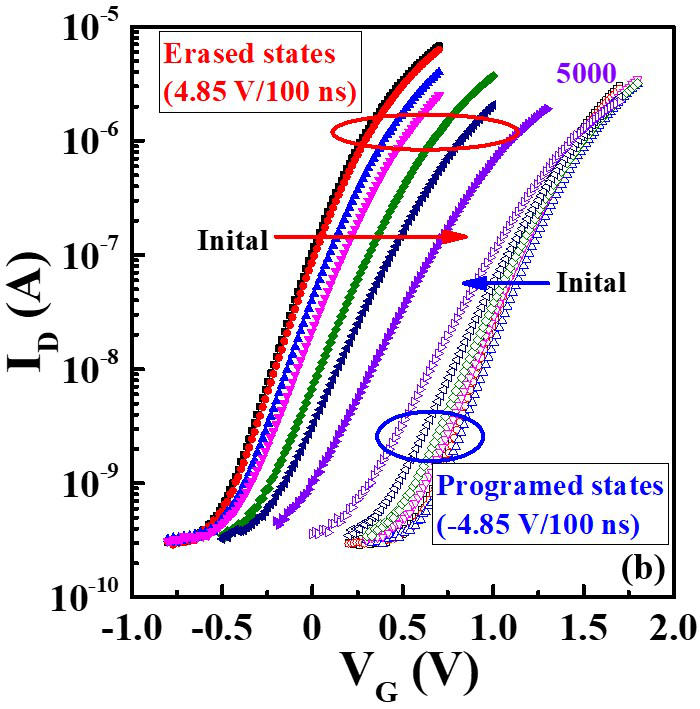
∆𝑉𝑇𝐻 = (   
 𝑃1(𝐸𝐹1)

𝐶𝐹  
 −  
 𝑃0(𝐸𝐹0)

𝐶𝐹 ) − ∆𝑄𝑜𝑡 𝐶𝐹𝐼−  
 ∆𝑄𝑖𝑡(∅𝑆=2∅𝐹)

𝐶𝐹𝐼   
 (2)

where *P0(EF0)* and *P1(EF1)* are the initial and actual polarization of ferroelectric thin film, respectively, *CF* is the capacitance of ferroelectric thin film, *Qot* is the change of oxide-trapped charges (*Qot*), and *Qit* is the change of interface-trapped charges (*Qit*) at *S* (surface potential)=*2**F*. Since *Qit* strongly depends on *S* while the *P1(EF1)* and *Qot*are negligibly influenced by it, *VTH* can be summarized as   
 ∆𝑉�� = ∆𝑉�� + ∆𝑉�� (3) where *Vmg* is the voltage shift at midgap condition (*S*=*F*) with uncharged interface traps, consisting of the former two parts in right branch of Eq. (2) (i.e. including the effects of charge trapping in the gate stack and polarization switching of ferroelectric thin film), and *Vit* is the voltage shift caused by interface trap generation, corresponding to the last part in right branch of Eq. (2). Note that *Vmg* is obtained by   
 ∆𝑉�� = (𝑉��)� − (𝑉��)� (4)

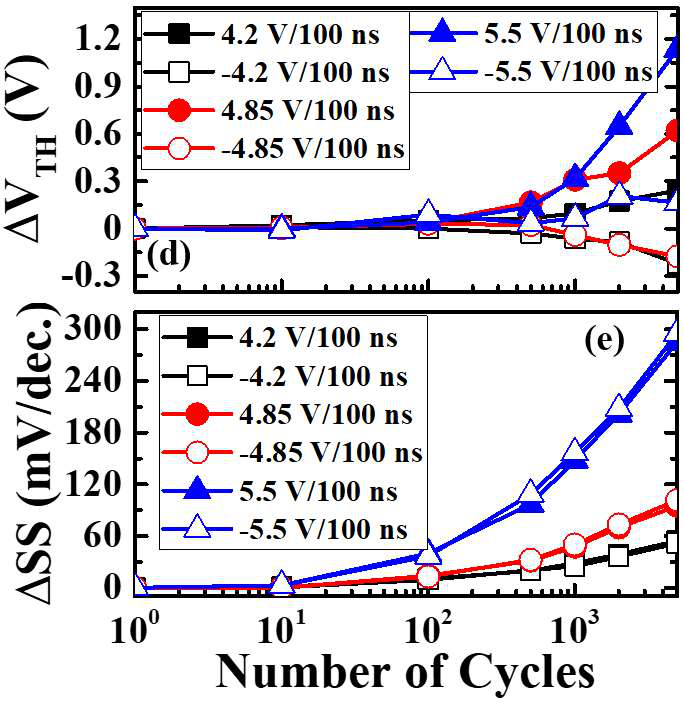
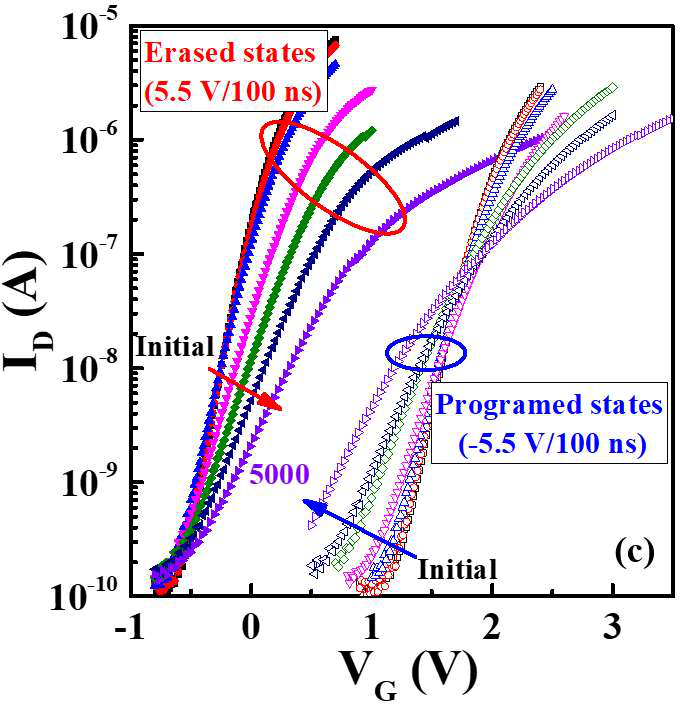
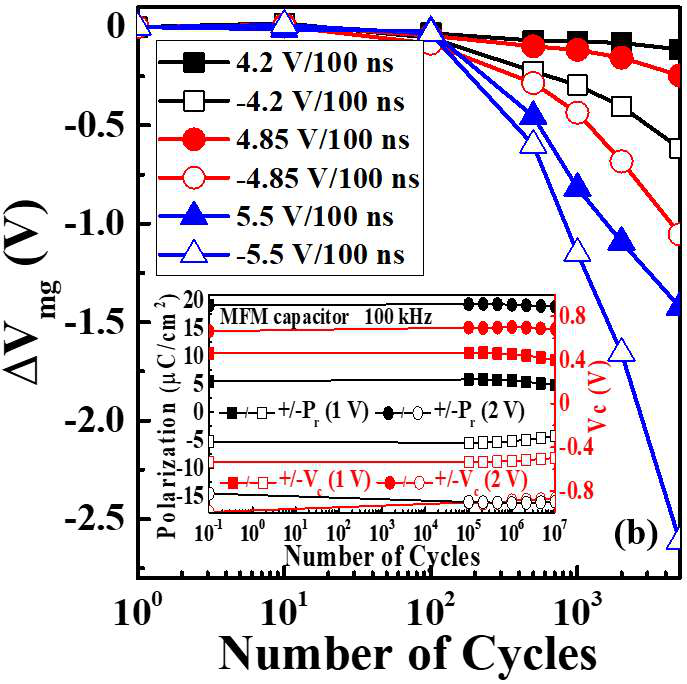
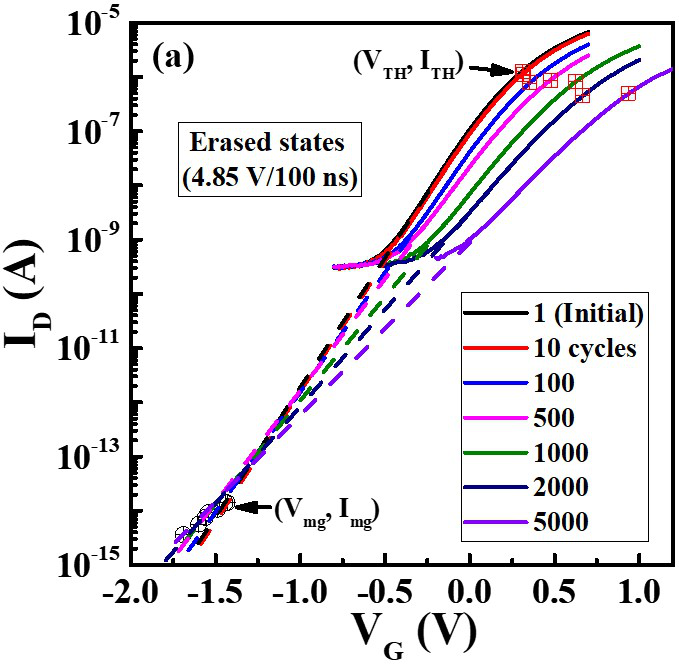


Fig. 2. (a), (b) and (c) are *ID-VG*characteristics with +/-4.2 V/100 ns, +/-4.85 V/100 ns and +/-5.5 V/100 ns cycling, respectively. (d) and (e) are the corresponding *VTH* and *SS* values with P/E cycling, respectively.



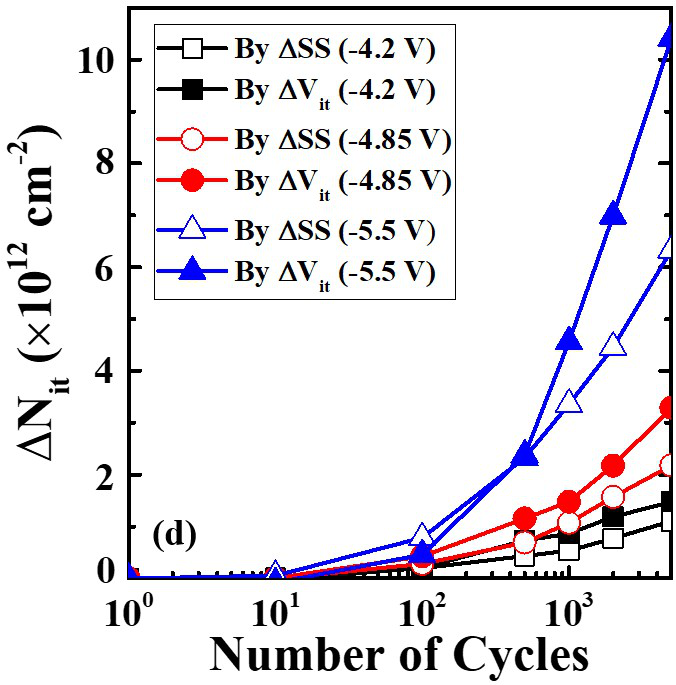
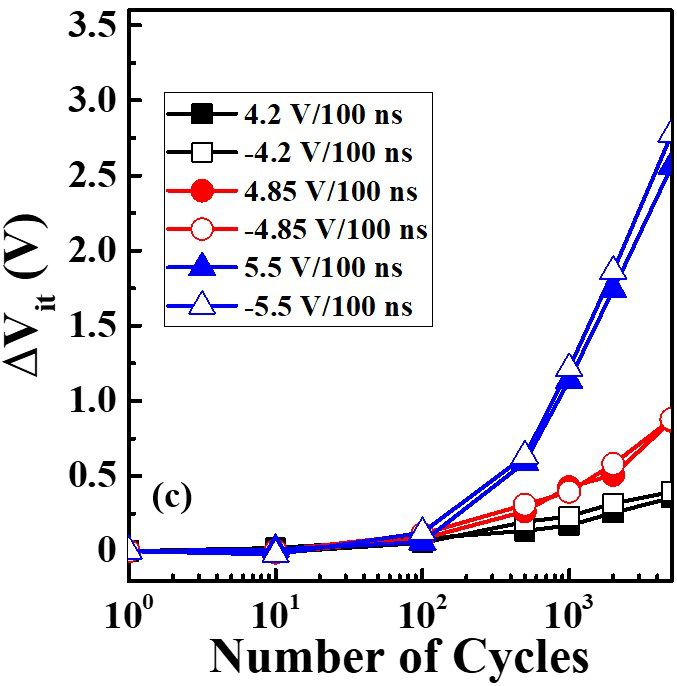


Fig. 3. (a) Subthreshold-current curves for the erased states (-4.85 V/100 ns), (b), (c) and (d) are*Vmg*,*Vit*, and*Nit* evolutions with P/E cycling, respectively.

where (*Vmg*)0 and (*Vmg*)1 are the initial and actual midgap voltage, respectively, which is the voltage corresponding to midgap current (*Img*). While *Img* is normally obtained from the subthreshold current equation (Eq. (5)) at *S*=*F* [23],

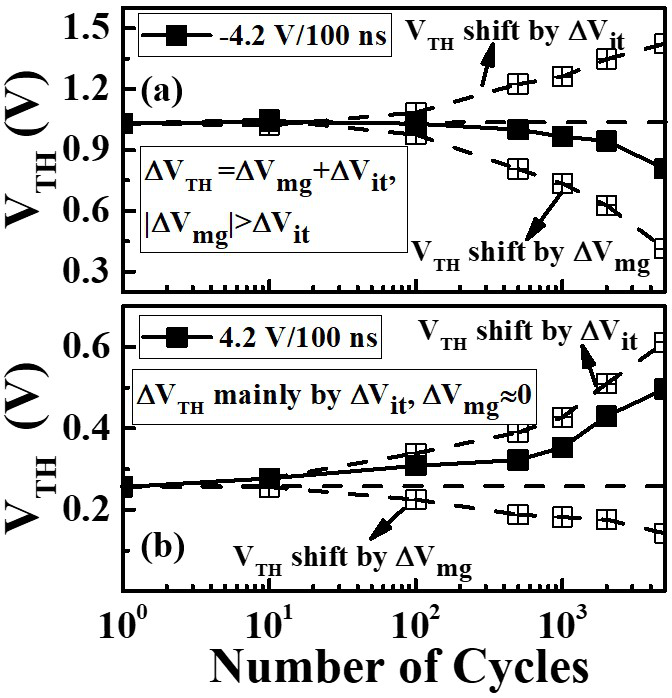
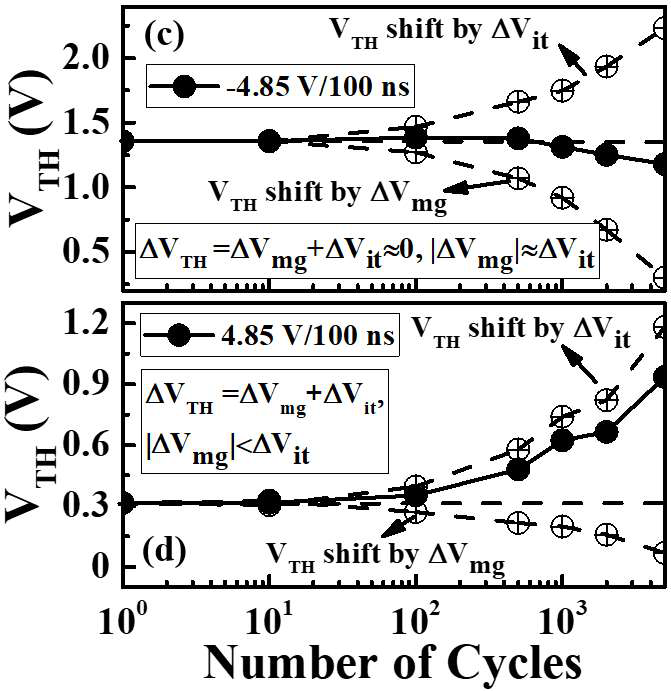
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| --- | --- | --- | --- |
| 𝐼� = | ��� ���� | ������ �� �∅����� | (1 − 𝑒����)𝑒�∅� (5) |

here,=*q/kT* (*q* is the absolute value of unit electronic charge), *n* is the electron mobility, *S* is the dielectric constant of silicon, *NA* and *ni* are the channel doping and intrinsic carrier

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P/E cycling. In the three cycling cases, *Vmg* values are negative, and the absolute values of *Vmg* (|*Vmg*|) increase with increasing cycling number and voltage.Meanwhile, the |*Vmg*| values in erased states are smaller than those in programed states. Besides, as shown in the inset of Fig. 3(b), the remanent  

concentration, respectively. Since *Img* is very small (calculated   
as 0.001-0.02 pA in the studied devices), the midgap voltage   
*Vmg* can be obtained by linearly extrapolating the subthreshold   
curve to the value of *Img* [14]-[15], [24], as shown in Fig. 3(a).

Fig. 3(b) shows the evolution of extracted *Vmg* values with

polarization (+/-*Pr*) and coercive voltage (+/-*Vc*) values of the HZO film almost do not change up to 1106 cycles at different cycling voltages (1 V and 2 V/100 kHz), which indicates that the *Vmg* is not caused by the HZO film itself [5]. Moreover, the variations of +/-*Pr* or +/-*Vc* in HZO film induced by the *VTH* shift also make a little contribution to *Vmg*. For program operations (starting from erased states), the positive *VTH* shift in erased states would decrease the applied voltage on the HZO film and thus decrease the |*-Pr*| or +*Vc* value, leading to the negative shift of *Vmg*. However, the amount of this negative shift might be much smaller than the observed |*Vmg*| value, which can be addressed based on the voltage division rule between HZO film (r 30) and SiO2 layer (r 3.9). For erase operations (starting from programed states), the +*Pr* or -*Vc* value of HZO film would not be influenced, due to the nearly constant *VTH* values in programed states. Thus, the negative *Vmg* values in both programed and erased states are mainly caused by the trapped holes in the gate stack. Compared to the |*Vmg*| values in the programed states, the smaller |*Vmg*| values in erased states might result from holes de-trapping or compensating of electrons trapping under erase pulse. The larger |*Vmg*| values at larger cycling number and voltage might be due to the more deteriorated insulating properties of SiO2 layer, which will facilitate the hole injection/trapping.

Fig. 3(c) shows the evolution of *Vit* values with P/E cycling, which are calculated by Eq. (3), from the results of Fig. 2(d) and Fig. 3(b). The *Vit* values are positive, consistent with that interface traps in the upper half of the band gap are acceptors and those in the lower half of the band gap are donors [25]. Besides, *Vit* values in the programed states are nearly same to those in the erased states, and both of them increase with increasing P/E cycling number and voltage, which agree with

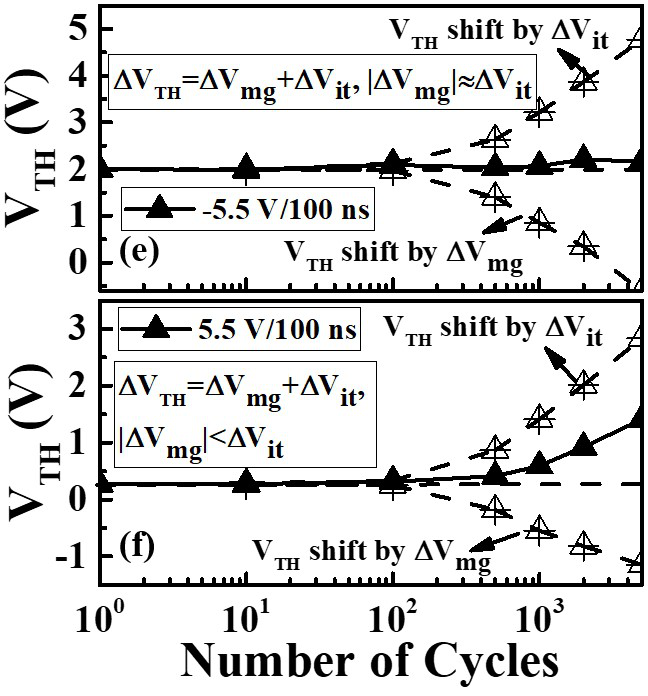
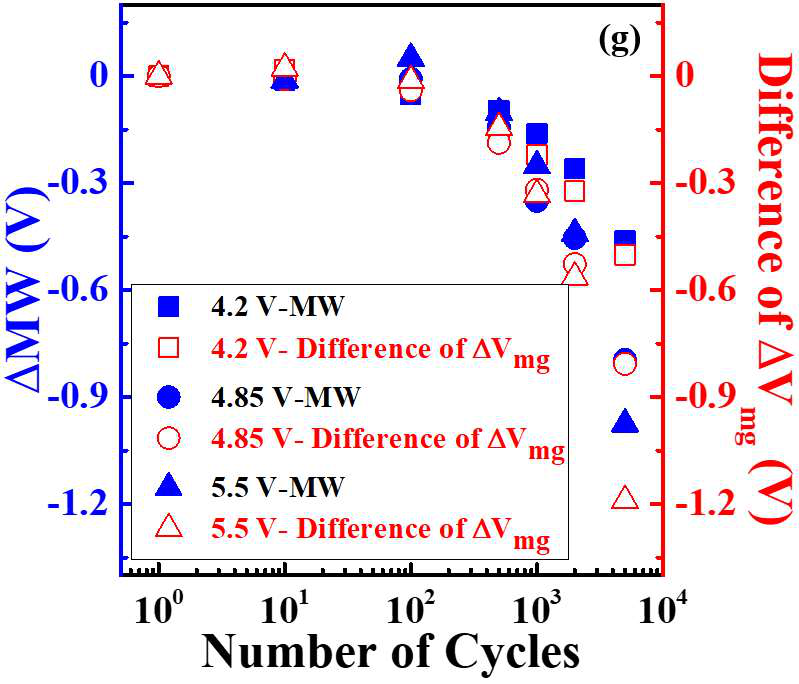
 

Fig. 4. (a) to (f) are *VTH* evolution with +/-4.2 V/100 ns, +/-4.85 V/100 ns and +/-5.5 V/100 ns cycling, respectively. (g) is the summary of *MW* degradation with P/E cycling.

in erased states, and they are nearly equal to *Vit* values in programed states. Therefore, the *VTH* is almost constant in the programed states, but it shifts to positive direction in the erased states, leading to the asymmetry *MW* closure. Similarly, the different *VTH* evolutions between programed and erased states for the +/-4.2 V/100 ns (Figs. 4(a), (b)) and +/-5.5 V/100 ns (Figs. 4(e), (f)) cycling cases can be addressed. On the basis of above discussion, the quantitative illustration of threshold voltage shift with P/E cycling can also be applied to explain the similar observations of *MW* degradations in elsewhere [5], [6], [8]-[10]. Moreover, as shown in Fig. 4(g), the amounts of *MW* degradation (*MW*) are nearly equal to the differences of *Vmg* values between programed and erased states. The larger differences of the *Vmg* values at higher P/E cycling voltages are responsible for their more severe *MW* degradations. It seems that the interface trap generation does not contribute to the *MW* degradation, but it would lead to the *VTH* shift, thereby having an effect on oxide charge trapping and midgap voltage shift.

the observations of *SS* values in Fig. 2(e). The generated IV.CONCLUSION

interface traps compared to the initial state (i.e. *Nit*) with P/E cycling are obtained according to Eqs. (2) and (3), shown in the solid symbols in Fig. 3(d). For validation of the proposed method, the *Nit* values calculated according to Eq. (1) using the obtained *SS* values are shown in Fig. 3(d), which are in good agreement with those calculated by *Vit* values.

Therefore, it is deduced that the unequal *Vmg* values lead to different amounts of *VTH* between programed and erased states. For the +/-4.85 V/100 ns cycling case shown in Figs. 4(c) and (d), the interface trap generation contributes to the nearly same shifts of *VTH*in programed and erased states to positive direction. On the other hand, the |*Vmg*| values are smaller than *Vit* values

The mechanism of P/E cycling degradation of Hf0.5Zr0.5O2-based FeFETs at different P/E cycling voltages has been investigated with the midgap voltage method. It was found that the midgap voltage shift is mainly contributed by charge trapping in the gate stack. The different threshold voltage evolutions with P/E cycling between programed and erased states are due to their unequal amounts of midgap voltage shift. Moreover, the amount of memory window degradation is nearly equal to the difference of midgap voltage shift values between programed and erased states. And the interface trap generation will affect the midgap voltage shift.

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> REPLACE THIS LINE WITH YOUR PAPER IDENTIFICATION NUMBER (DOUBLE-CLICK HERE TO EDIT) < 4

REFERENCES

[1]International Roadmap for Devices and Systems (IRDS) 2017 Edition: https://irds.ieee.org/.

[2]S. Dünkel, M. Trentzsch, R. Richter, P. Moll, C. Fuchs, O. Gehring, M.

Majer, S. Wittek, B. Müller, T. Melde, H. Mulaosmanovic, S. Slesazeck, S. Müller, J. Ocker, M. Noack, D.-A. Löhr, P. Polakowski, J. Müller, T.

Mikolajick, J. Höntschel, B. Rice, J. Pellerin, and S. Beyer, “A FeFET based super-low-power ultra-fast embedded NVM technology for 22nm FDSOI and beyond,” in IEDM Tech. Dig., Dec. 2017, pp. 19.7.2–19.7.4, doi: 10.1109/IEDM.2017.8268425.

[3]J. Van Houdt, “3D memories and ferroelectrics,” in IEEE International Memory Workshop, May. 2017, doi: 10.1109/IMW.2017.7939066.

[4]K. Florent, S. Lavizzari, L. Di Piazza, M. Popovici, E. Vecchio, G.

Potoms, G. Groeseneken, and J. Van Houdt, “First demonstration of vertically stacked ferroelectric Al doped HfO2 devices for NAND applications,” in Proc. Symp. VLSI Technol., Jun. 2017, pp. T158–T159, doi: 10.23919/VLSIT.2017.7998162.

[5]E. Yurchuk, S. Müller, D. Martin, S. Slesazeck, U. Schroeder, T.

Mikolajick, J. Müller, J. Paul, R. Hoffmann, J. Sundqvist, T. Schlösser, R.

Boschke, R. Bentum, and M. Trentzsch, “Origin of the endurance degradation in the novel HfO2-based 1T ferroelectric non-volatile memories,” in Proc. IEEE IRPS, Jun. 2014, pp. 2E.5.1–2E.5.5, doi: 10.1109/IRPS.2014.6860603.

[6]N. Gong and T.-P. Ma, “A study of endurance issues in HfO2-based ferroelectric field effect transistors: Charge trapping and trap generation,” IEEE Electron Device Lett., vol. 39, no. 1, pp. 15–18, Jan. 2018, doi: 10.1109/LED.2017.2776263.

[7]J. Muller, P. Polakowski, S. Muller, H. Mulaosmanovic, J. Ocker, T.

Mikolajick, S. Slesazeck, S. Muller, J. Ocker, T. Mikolajick, S.

Flachowsky, and M. Trentzsch “High endurance strategies for hafnium oxide based ferroelectric field effect transistor,” in 16th Non-Volatile Memory Technology Symposium (NVMTS), Oct. 2016, doi: 10.1109/NVMTS.2016.7781517.

[8]J. Müller, T. S. Böscke, S. Müller, E. Yurchuk, P. Polakowski, J. Paul, D.

Martin, T. Schenk, K. Khullar, A. Kersch, W. Weinreich, S. Riedel, K.

Seidel, A. Kumar, T.M. Arruda, S.V. Kalinin, T. Schlösser, R. Boschke, R. van Bentum, U. Schröder, and T. Mikolajick, “Ferroelectric hafnium oxide: a CMOS-compatible and highly scalable approach to future ferroelectric memories,” in IEDM Tech. Dig., Dec. 2013, pp. 10.8.1–10.8.4, doi: 10.1109/IEDM.2013.6724605.

[9]B. J. Zeng, W. W. Xiao, J. J. Liao, H. Liu, M. Liu, Q. X. Peng, S. Z. Zheng, and Y. C. Zhou, “Compatibility of HfN metal gate electrodes with Hf0.5Zr0.5O2 ferroelectric thin films for ferroelectric field-effect transistors,” IEEE Electron Device Lett., vol. 39, no. 10, pp. 1508–1511, Sept. 2018, doi: 10.1109/LED.2018.2868275.

[10]T. Ali, P. Polakowski, S. Riedel, T. Büttner, T. Kämpfe, M. Rudolph, B.

Pätzold, K. Seidel, D. Löhr, R. Hoffmann, M. Czernohorsky, K. Kühnel, P. Steinke, J. Calvo, K. Zimmermann, and J. Müller, “High endurance ferroelectric hafnium oxide-based FeFET memory without retention penalty,” IEEE Trans. Electron Devices, vol. 65, no. 9, pp. 3769–3774, Sept. 2018, doi: 10.1109/TED.2018.2856818.

[11]K. Ni, P. Sharma, J. Zhang, M. Jerry, J. A. Smith, K. Tapily, R. Clark, S.

Mahapatra, and S. Datta, “Critical role of interlayer in Hf0.5Zr0.5O2 ferroelectric FET nonvolatile memory performance,” IEEE Trans.

Electron Devices, vol. 65, no. 6, pp. 2461–2469, Jun. 2018, doi: 10.1109/TED.2018.2829122.

[12]M. Pešiü, V. Di Lecce, D. Pramanik, and L. Larcher, “Multiscale modeling of ferroelectric memories: insights into performances and

[16]E. W. Enlow, R. L. Pease, and D. R. Alexander, “Subthreshold technique for fixed and interface trapped charge separation in irradiated MOSFETs,” Mission Research Corp., Univ. Volkswagen Mazda, Albuquerque, NM, USA, Tech. Rep. 28, Feb. 1987.

[17]J. D. Lee, J. H. Choi, D. G. Park, and K. Kim, “Effects of interface trap generation and annihilation on the data retention characteristics of Flash memory cells,” IEEE Trans. Electron Devices, vol. 4, no. 1, pp. 110–117, Mar. 2004, doi: 10.1109/TDMR.2004.824360.

[18]A. Fayrushin, K. S. Seol, J. H. Na, S. H. Hur, J. D. Choi, and K. Kim, “The new program/erase cycling degradation mechanism of NAND Flash memory devices,” in IEDM Tech. Dig., Dec. 2009, pp. 34.2.1–34.2.4, doi: 10.1109/IEDM.2009.5424213.

[19]A. Ortiz-Conde, F. J. Garcıa-Sánchez, J. Muci,A. T. Barrios J. J. Liou, and C. S. Ho, “Revisiting MOSFET threshold voltage extraction methods,” Microelectron. Reliab., vol. 53, no. 1, pp. 90–104, Jan. 2013, doi: 10.1016/j.microrel.2012.09.015.

[20]W. J. Zhu, "Hafnium oxide and hafnium aluminum oxide for CMOS application", Ph.D. dissertation (Chapter 2), Dept. Elect. Eng., Yale Univ., New Haven, CT, 2003.

[21]S. L. Miller and P. J. McWhorter, “Physics of the ferroelectric nonvolatile memory field-effect transistor,” J. Appl. Phys., vol. 72, no. 12, pp. 5999–6010, Sep. 1992, doi: 10.1063/1.351910.

[22]H. T. Lue, C. J. Wu, and T. Y. Tseng, “Device modeling of ferroelectric memory field-effect transistor (FeMFET),” IEEE Trans. Electron Devices,

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| vol. | 49, | no. | 10, | pp. | 1790–1798, | Oct. | 2002, | doi: |

10.1109/TED.2002.803626.

[23]S. M. Sze and Kwok K. Ng, Physics of Semiconductor Devices. New York: Wiley, 2006, pp. 314.

[24]Y.-B. Park and D. K. Schroder, “Degradation of thin tunnel gate oxide under constant fowler-nordheim current stress for a flash EEPROM,” IEEE Trans. Electron Devices, vol. 45, pp. 1361–1368, Jun. 1998, doi: 10.1109/16.678579.

[25]S. M. Sze and Kwok K. Ng, Physics of Semiconductor Devices. New York: Wiley, 2006, pp. 214.

reliability,” in Int. Conf. Simul. Semicond. Processes Devices, Setp. 2018,   
pp. 111–114, doi: 10.1109/SISPAD.2018.8551722.

[13]D. Martin, E. Yurchuk, S. Müller, J. Müller, J. Paul, J. Sundquist, S.

Slesazeck, T. Schlösser, R. V. Bentum, M. Trentzsch, U. Schröder, and T.

Mikolajick, “Downscaling ferroelectric field effect transistors by using   
ferroelectric Si-doped HfO2,”Solid-State Electron., vol. 88, pp. 65–68,   
doi:10.1109/ULIS.2012.6193391.

[14]P. S. Winokur, J. R. Schwank, P. J. McWhorter, P. V. Dressendorfer, and   
D. C. Turpin, “Correlating the radiation response of MOS capacitors and   
transistors,” IEEE Trans. Nucl. Sci., vol. 31, no. 6, pp. 1453–1460, Dec.   
1984, doi: 10.1109/TNS.1984.4333529.

[15]P. J. McWhorter, and P. S. Winokur, “Simple technique for separating the   
effects of interface traps and trapped-oxide charge in metal-oxide-  
semiconductor transistors,” Appl. Phys. Lett., vol. 48, no. 2, pp.133–135,   
Feb. 1986, doi: 10.1063/1.96974.

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