**Dependence of Reliability of Ferroelectric HfZrOx on Epitaxial SiGe Film with Various Ge Content**

Kuen-Yi Chen, Yen-Hua Huang, Ruei-Wen Kao, Yan-Xiao Lin, and Yung-Hsien Wu\*

Department of Engineering and System Science, National Tsing Hua University, 300, Hsinchu, Taiwan \*E-mail: yunhwu@mx.nthu.edu.tw

**Abstract**   
 TiN/ferroelectric-HfZrOx (HZO)/epi-SiGe (MFS) structure was employed as the platform to investigate the dependence of Ge content on reliability performance and the mechanism behind it. As compared to Si counterpart, HZO on Si0.56Ge0.44 exhibits not only enhanced remnant polarization (Pr) by 58 % but much improved reliability in terms of negligible Pr degradation up to 109 cycles under ±4 V/100k Hz bipolar AC stress, desirable retention at pristine and cycled state up to 104 sec, and smaller imprint effect against time at 85 oC. The Ge content-dependent reliability performance is mainly due to the thinner sub-oxide interfacial layer (IL) with better quality since it is too thin to trap charges while less vulnerable to defect generation due to stronger bonding (fewer Vo). IL with higher κ value is also helpful to suppress E-field across it, beneficial to enhance reliability. The results suggest that as the technology advances into SiGe platform, it is more viable for MFS-based memory as the reliability issues for Si will be greatly mitigated.

**Introduction**   
 The development of HfO2-based ferroelectric (FE) has ushered in a new era for green memory and logic devices which encompass two basic structures, metal-ferroelectric-metal (MFM) typically for memory applications such as FeRAM [1] or ferroelectric tunneling junction (FTJ) [2] and metal-ferroelectric-semiconductor (MFS) mainly for steep-slope negative capacitance logic devices [3] and memory-based FeFETs [4]. Besides performance, it is imperative to study the reliability performance before devices can be practically used. The reliability issues have been well explored and possible solutions were proposed for MFM structures [5]. For MFS structures, although the semiconductor material has been evolved from Si to Ge substrate [6], similar studies on Ge are in the very early stage [7, 8] and the impact of introducing Ge into Si substrate on reliability characteristics has never been reported. In this work, by using epitaxial SiGe on Si substrate with various Ge content as the platform, with MFS structure, the dependence of reliability characteristics of ferroelectric HZO on Ge content ranging from 16 % to 44 % was investigated. The importance of this work lies in two aspects. (a) Bridging the understanding gap between FE-HZO on Si and Ge substrate and (b) Pioneering the in-depth FE-HZO investigation on epitaxial SiGe film, which is the most promising successor to Si for sub-7 nm VLSI technology before Ge process matures. The results indicate that as compared to Si counterpart, FE-HZO on Si0.56Ge0.44 corresponds to enhanced Pr and improved reliability in terms of more robust endurance up to 109 cycles, better retention, and less imprint effect at 85 oC. The Ge content-dependent reliability implies that the reliability issues of MFS devices on Si are alleviated as it migrates to SiGe platform.

**Device Fabrication**   
 15-nm epitaxial SiGe film with Ge content of 16 % and 44 % grown on Si substrate was adopted as the platform. After doping the SiGe by P (21019 cm-3), HZO dielectric of 10 nm was formed followed by 30-nm TiN electrode deposition, both by ALD, to form the MFS structure. Then 30-sec RTA at 500 oC was used to crystallize HZO for inducing ferroelectricity. The same substrate doping and MFS structure was also prepared on Si substrate as reference. Besides electrical measurement to confirm the ferroelectricity, extensive reliability characteristics including endurance, retention and imprint effects were studied for different samples. Physical analyses were also carried out to investigate the mechanism of different behaviors.

**Results and Discussion**   
*(A). Conformation of ferroelectricity of HZO on epitaxial SiGe*  XRD patterns (**Fig. 1**) reveal the HZO crystallinity for different substrates. Although HZO on all kinds of samples exhibit orthorhombic phase (o-phase), HZO on substrate with higher Ge content shows better crystallinity due to smaller FWHM of the o-phase diffraction peak. All samples were found to have ferroelectricity by measuring polarization (P) and capacitance (C) vs. voltage (V) and doing piezo-response force microscopy (PFM) analysis. **Fig. 2** shows the results for HZO on Si0.56Ge0.44 after wake-up. Asymmetriccoercive voltage (VC)

is due to different top/bottom electrode. **Fig. 3** displays the enhanced Pr by 58 % for Si0.56Ge0.44 as compared to Si.

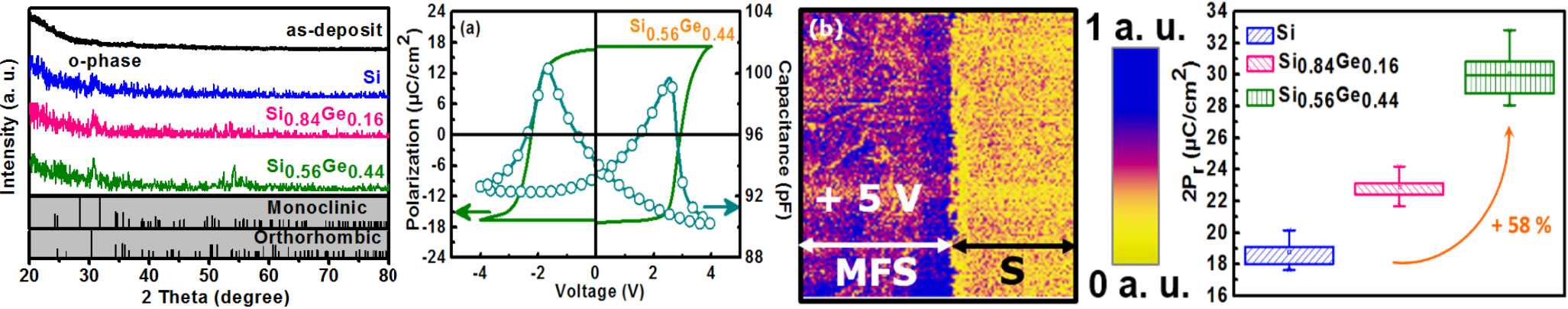
*(B). Ge content-dependent reliability performance*   
 **Fig. 4** shows the dependence of cycling on P-V curves for

devices on Si0.56Ge0.44 by ±4 V/100k Hz bipolar stress. **Fig. 5** displays the endurance performance under the same stress but with different frequencies for all kinds of samples. Abrupt leakage increase indicates generation of a large amount of defects that completely pin domain walls. For Si, although reliability improves as stress frequency increases from 1k to 100k Hz, significant wake-up and fatigue effects are still observed. However, devices on Si0.56Ge0.44 are almost free from the issues up to 109 cycles (100k Hz)**.Fig. 6** shows the Arrhenius plot of wake-up for activation energy (Ea) extraction [9]. Ea for Si is 0.58 eV, which is close to the oxygen vacancy (Vo) migration energy near Si/HfO2 interfaces [10]. Si0.56Ge0.44 with higher Ea of 1.17 eV implies fewer Vo at interface. **Fig. 7** shows the retention of PSW, OS (Switched Polarization, Opposite State) for all samples under pristine state at 25/85 oC. Severer retention degradation is found at 85 oC for Si due to imprint effect, which is inferred by the significant OS read current peak shift (**inset**). The degradation is greatly mitigated for Si0.56Ge0.44 with stable PSW, OS up to 104 sec at 25 oC. However, PSW, SS (Same State) is independent of substrate/temperature (**Fig. 8**). Retention for cycled devices are shown in **Fig. 9** and Si0.56Ge0.44 still shows stable PSW, OS against time even with 106 cycles. Imprint effect is characterized by VC shift at 25/85 oC vs. retention time and the results for all kinds of samples are shown in **Fig. 10**. Vc shift with retention time is observed for Si and worse degradation is found at 85 oC, consistent with PSW, OS. The imprint effect is alleviated by using Si0.56Ge0.44. As the Ge content in the substrate increases, HZO reliability improves accordingly. It indicates that HZO/substrate interface plays the essential role.

*(C). Origin of superior reliability for higher Ge content*   
 The fatigue effect during cycling is due to newly generated defects and injected charges that pin the domain walls. Retention loss is resulted from leakage followed by charge trapping while imprint effect is caused by internal E-field due to trapped charge. The reliability improvement by increasing Ge content can be explained by the thinner sub-oxide interfacial layer (IL) with better quality between HZO/substrate that helps suppress trapping/generation of charges. The inference is evidenced by the XPS Ge 2p and Si 2p spectra (**Fig. 11**). For Ge 2p spectra, the peak at 1220.5 eV corresponds to Ge-O bond in the form of GeOx (x=1.5~2). However, the GeOx:Ge peak intensity ratio is rather weak and independent of Ge content, indicating less GeOx. It is caused by interdiffusion between ZrO2 in HZO and GeOx, consistent with the result that ZrO2/Ge tends to form nearly zero GeOx IL after 500 oC annealing [11]. Interdiffusion means Ge incorporation into HZO which is helpful to form o-phase [11] as seen in XRD and explains a larger Pr due to Zr-Ge bond at interface [6]. For Si 2p spectra, compared to Si, SiOx component on Si0.56Ge0.44 is also found but with much weaker intensity and stronger oxide quality (BE closer to higher oxidation state Si4+ implies more stoichiometric bonding with fewer Vo, consistent with the larger Ea of Si0.56Ge0.44). EDS line scan also proves Zr-Ge bond for Si0.56Ge0.44 due to incorporation of Ge at HZO/IL interface (**Fig. 12**). The thinner IL is confirmed by the inset TEM. IL in MFS is critical for reliability [12]. Better reliability for Si0.56Ge0.44 is due to its IL that is too thin to trap charges and of stronger bonding to suppress defects generation. Smaller E-field across the IL (higher κ with GeOx) also explains the better reliability.

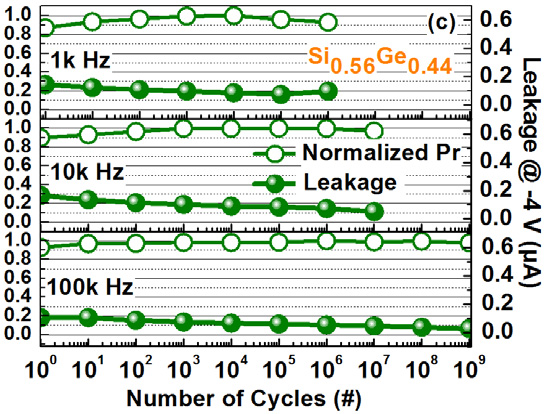
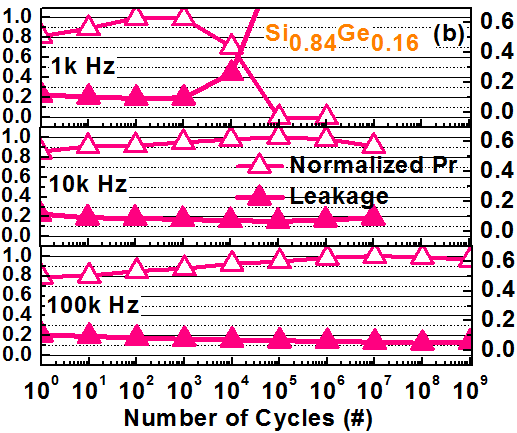
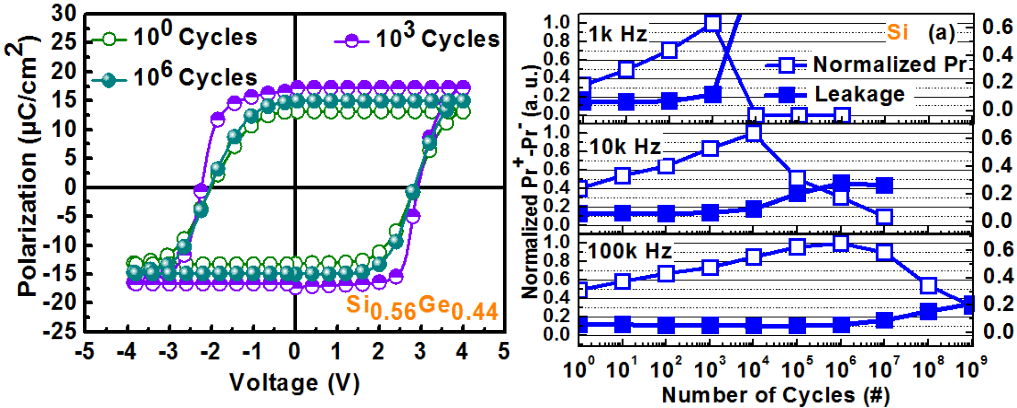
**Conclusion**   
 Reliability of FE-HZO was evaluated in MFS structure on epitaxial SiGe film with various Ge content. For devices on Si0.56Ge0.44, negligible Pr degradation up to 109 cycles under bipolar AC stress, desirable retention at pristine and cycled state, and small imprint effect at 85 oC are obtained, much improved as compared to Si counterpart due to IL with thinner thickness, robust quality (fewer Vo) and higher dielectric constant, making less charge trapping and generation during test. The Ge content-dependent reliability suggests that the reliability issues will be alleviated as VLSI technology enters new era of SiGe platform.

|  |  |  |
| --- | --- | --- |
| 978-1-5386-4218-4/18/$31.00 ©2018 IEEE | 2018 Symposium on VLSI Technology Digest of Technical Papers | 119 |



(b)

|  |  |  |
| --- | --- | --- |
| **Fig. 1** XRD patterns for HZO on Si and epi-SiGe with various Ge content. O-phase is found for all samples. | **Fig. 2** Confirmation of ferroelectricity of HZO on epi-Si0.56Ge0.44 by | **Fig. 3** Dependence of 2Pr (woken-up state) on samples with various Ge content. |
| (a) woken-up hysteresis P-V and butterfly-like C-V by ±4 V/1k Hz cycling and (b) PFM amplitude poled with +5 V over 5 μm. |



**Fig. 4** P-V hysteresis for epi- **Fig. 5** Dependence of Pr+-Pr- and leakage current on cycling for (a) Si, (b) Si0.84Ge0.16 and (c) Si0.56Ge0.44

Si0.56Ge0.44 with ±4 V/1k Hz cycling. with ±4 V cycling. Impact of cycling frequency on reliability is also investigated.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | | | | | 120 |
| **Fig. 6** Arrhenius plot of wake-up for (a) Si and (b) Si0.56Ge0.44 for activation energy (Ea) extraction. The wake-up threshold is defined as the cycling number at which Pr reaches the maximum Pr at 25 oC. | | | **Fig. 7** Impact of temperature on retention of PSW, OS for (a) Si and (b) Si0.56Ge0.44. Inset shows the read current vs. hold time and reduced current/shifted peak for Si implies worse imprint effect. | |
|  | |  | | |
| **Fig. 8** Retention of PSW, SS for Si and Si0.56Ge0.44. Both are stable at 85 oC. | **Fig. 9** Retention of PSW, OS for (a) Si and (b) Si0.56Ge0.44 pre-cycled by different cycling numbers (±4 V/1k Hz cycling) at 25 oC. | | | **Fig. 10** Imprint performance for Si and Si0.56Ge0.44 at 25 oC and 85 oC. |
|  |  | **Fig. 11** XPS (a) Ge 2p and (b) Si 2p spectra for different substrates. For Ge 2p, the rather weak peak implies that nearly no GeOx component is formed on SiGe. For Si 2p, SiOx formed on Si0.56Ge0.44 shows weaker intensity (thinner IL) but more stoichiometric bonding (stronger oxide quality with fewer Vo) as compared to Si counterpart. | | **Acknowledgement**  The authors would like to thank the supports by TSMC and the Ministry of Science and Technology of Taiwan. |
| **References:**  **[1]** J. Muller et al., APL, 99, 112901, 2011. **[2]** S. Fujii et al., Symp. VLSI Tech. (2016), 148. **[3]** M. H. Lee et al., IEDM (2015), 616. **[4]** T. S. Bösckea et al., IEDM (2011), 547. **[5]** K. Y. Chen et al., Symp. VLSI Tech. (2017), 84. **[6]** C. J. Su et al., Symp. VLSI Tech. (2017), 152. **[7]** C. J. Su et al., IEDM (2017), 369. **[8]** X. Tian et al., IEDM (2017), 816. **[9]** Franz P. G.  ESSDERC, Fengler et al.,  (2016), 369. **[10]** C. Tang et al., Phys. Rev. B, 76, 073306, 2007. **[11]** Y. Kamata, Mater. Today, 11, 30, 2008. **[12]** E. Yurchuk et al., IRPS (2014), 2E.5.1. |
|  |  | **Fig. 12** EDS line scan for HZO on (a) Si and (b) Si0.56Ge0.44. Ge incorporation at HZO/IL which forms Ge-Zr bond is observed for Si0.56Ge0.44 and responsible for the higher Pr. The TEM image shown in the inset confirms the thinner IL for Si0.56Ge0.44, consistent with the results from XPS analysis. | |
| 2018 Symposium on VLSI Technology Digest of Technical Papers | | | | |