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Device Modeling of Ferroelectric Memory

Field-Effect Transistor (FeMFET)

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***Abstract—*A numerical analysis of the electrical characteristics for the ferroelectric memory field-effect transistors (FeMFETs) is presented. Two important structures such as the metal–ferroelec-tric–insulator–semiconductor field–effect transistor (MFISFET) and metal–ferroelectric–metal–insulator–semiconductor field–ef-fect transistor (MFMISFET) are considered. A new analytic expression for the relation of polarization versus electric field (P–E) is proposed to describe the nonsaturated hysteresis loop of the ferroelectric material. In order to provide a more accurate simulation, we incorporate the combined effects of the nonsat-urated polarization of ferroelectric layers and the nonuniform distributions of electric field and charge along the channel. We also discuss the possible nonideal effects due to the fixed charges, charge injection, and short channel. The present theoretical work provides some new design rules for improving the performance of FeMFETs.**

***Index Terms—*Ferroelectric memory field-effect transistors (FeMFET), ferroelectric, ferroelectric random access memory (FeRAM), memory, metal–ferroelectric–insulator–semiconductor (MFIS),**  **metal–ferroelectric–metal–insulator–semiconductor (MFMIS), modeling, one transistor (1T), transistor.**

I. INTRODUCTION   
**T** they can provide nonvolatile memory operation with fast has acquired much attention in recent years because HE ferroelectric random access memory (FeRAM) [1]

writing time. Among several possible device structures, the

ferroelectric memory field-effect transistor (FeMFET) [2]–[7]

having a nondestructive readout operation and high density

is of vital interest. The FeMFET includes the MFISFET

[2]–[5] and MFMISFET [6], [7]. In these device structures, the

ferroelectric material is placed on the gate of the transistor. The

stored dipole moments in the ferroelectric material can adjust

the threshold voltages of an FeMFET and thus the drain current

of each switching state can be discriminated and identified as a

logic state in a memory.

There have been many reports on the fabrications of MFIS-

and/or MFMIS-based FETs and capacitors thus far. The system-

atic theoretical methods [2], [3] for the characterization and pre-

diction of the experimental results however remain rarely seen.

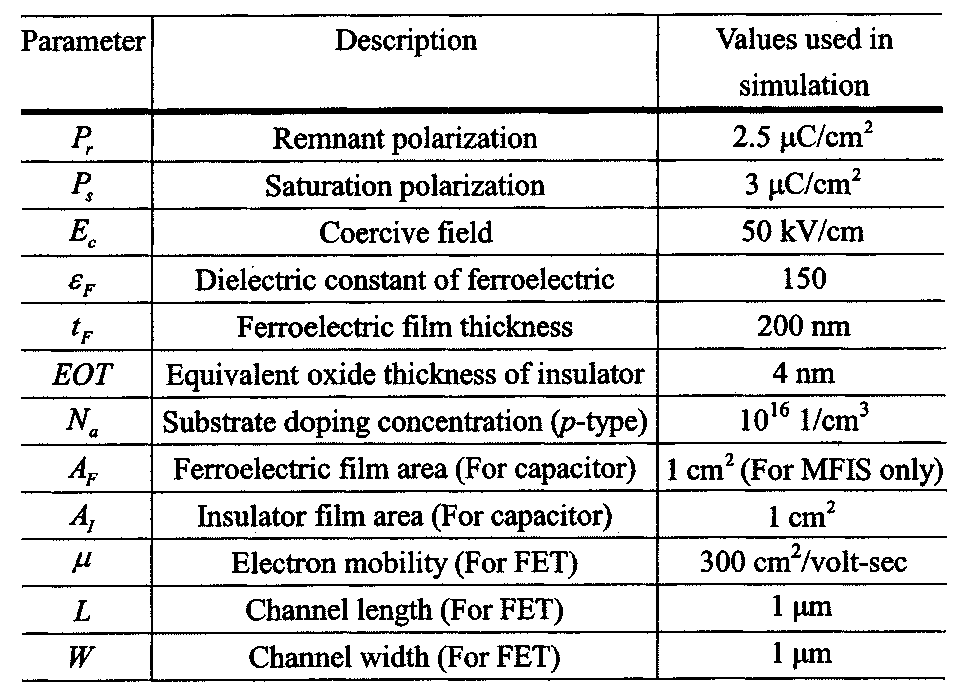
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TABLE I   
DEVICE PARAMETERS FOR THE SIMULATION OF FeMFET IN THE TEXT



In order to theoretically investigate the electrical characteristics of an FeMFET, Miller *et al.* have first proposed a mathematical model [2]. In their model, the drain current calculated by using Brews charge sheet model [10] is not suitable for an FET oper-ated in the saturation (after pinchoff) and subthreshold regions. The model simply assumes the electric field in the ferroelectric film to be constant, independent of the channel position [2], [3]. This assumption is only valid for the case of low drain voltage. In this paper, we shall remove these limitations and propose a more relevant model to include not only the nonsaturated po-larizations of the ferroelectric layer but the nonuniform distri-bution of the field and charge along the channel position. Sys-tematic analyses on the electrical characteristics for MFISFET and MFMISFET in addition to the associated capacitors will be made. The material and geometric parameters of these devices used are in a wide range in order to gain some physical insight about the operation of FeMFETs. The calculation algorithm will also be described in detail so that one can easily follow. We have used 12 parameters to describe the transistor (as listed in Table I), which are the required minimum physical parameters and no other phenomenological ones are needed. The results of the electrical properties of the FeMFETs will be shown to be independent of the value of equivalent oxide thickness (EOT) of the insulator. In addition, the insulator may be fabricated in a stacked structure rather than a single layer, for the purpose of better crystallization in some experiments. With these reasons and for a more general simulation purpose, the parameter of the insulator is indicated by a single EOT instead of the dielectric constant and thickness ( ).

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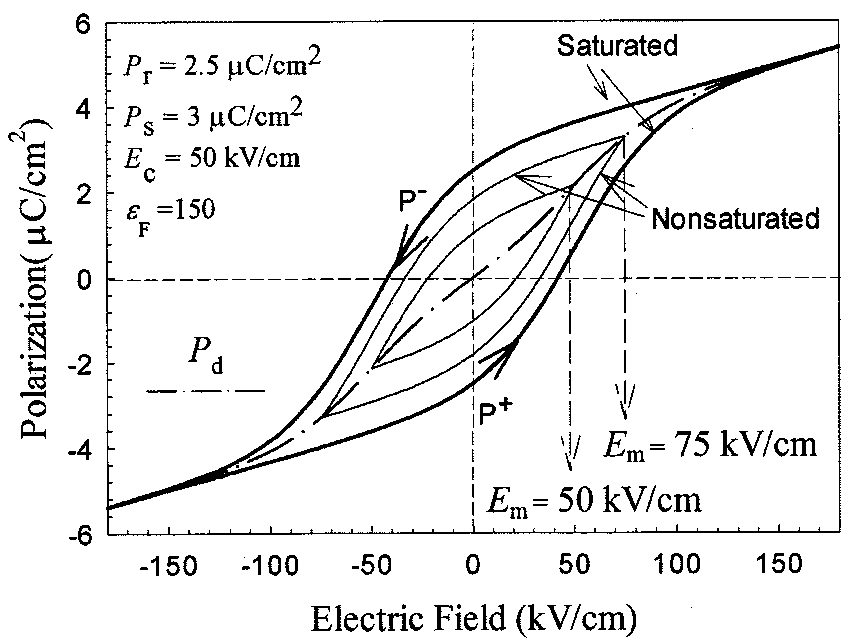


Fig. 1. P–E for the ferroelectric materials under various maximum electric fields in (1)–(6).

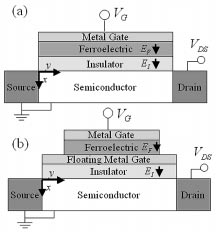


Fig. 2. Device structures and the associated sign conventions for the (a) MFISFET and (b) MFMISFET.

II. PHENOMENOLOGICAL MODEL OF POLARIZATION ELECTRIC FIELD (P–E) OF THE FERROELECTRIC CAPACITORS

Miller *et al.* [8] have proposed a simple model to fit the exper-imental polarization–electric field (P–E) relationship in a ferro-electric capacitor, namely

(1)

where

(2)

(3)

Here, indicates the lower (positive-going) branch of the P–E relation, while is the upper (negative-going) branch. The last term in the right hand side of (1) denotes the linear contribution of the dipole moment. Equations (1)–(3) fit well into the P–E relation of the saturated hysteresis

|  |
| --- |
| loop. They cannot, however, describe the nonsaturated (minor) situation. We now construct a new expression for the minor hysteresis loop within the framework of the previous model. The minor hysteresis loop is supposed to be determined by a parameter, , the maximum electric field that the ferroelec-tric layer may undergo. The minor hysteresis loop consists of two branches,   and . Since is the maximum electric field, it is expected that  and must intersect there. Together with the fact stated in [8], “existing data indicate that the derivative of the polarization with respect to the electric field, evaluated at a constant field, is independent of the amplitude of the applied signal, at least to first order,” the minor loops can be derived and given by |

(4)

(5)

The polarization as a function of the maximum electric field is defined by

(6)

Two calculated minor loops of P–E are depicted in Fig. 1. The unpolarized ferroelectric material is first at the origin ( ). Once the applied field is increased, the dipole moment will follow the curve of until the maximum electric field is reached. Then the polarization will follow and along the direction indicated in Fig. 1.

Equations (4)–(6) are simple and analytic and they can be used to simulate the characteristics for a ferroelectric-based de-vice. Although they are not suitable for the case of the applied voltage being arbitrarily asymmetrical as stated in the [9], yet they are time-saving in the computer calculation.

III. – SIMULATION OF THE CAPACITORS

The structures of MFISFET and MFMISFET together with the sign conventions are depicted in Fig. 2. For the capacitance–voltage ( – ) simulation of MFIS capacitor, the continuous boundary condition for the normal electric displacement is

(7)

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where , , and are the electric fields in the ferroelectric

layer, insulator, and semiconductor (Si), respectively. We can ig-

nore in (7) because it is much smaller than the dipole mo-

ment . Gauss’s law gives , where

is the space charge (per unit area) in the semiconductor

and is the surface band bending potential. Equation (7) can

then be rewritten as

(8)

(9)

The corresponding voltage drops in the ferroelectric layer and

insulator are and , respectively. The space charge density

is given in [10].

The total gate voltage is given by

(10)

Assuming the unpolarized ferroelectric film is first at the origin

( ), then the dipole moment will follow .

Given the maximum writing gate voltage, or and

solving, with the help of Newton’s method, (8)–(10), one can

find the corresponding surface band bending potential as

well as the maximum electric field in the ferroelectric

layer. Once is determined, two branches

and in (4) and (5) are explicitly determined.

Repeatedly solving (8)–(10) by sweeping gate voltage from

to and using , then , and as

a function of gate voltage can be obtained. Similarly, one can

find , and by sweeping from to together

with . The reason for the direction will be further

discussed in Section V.

The capacitance, obtained from the series combination of the

multilayered capacitors, is expressed as

IV. SIMULATION OF DRAIN CURRENT OF FEMFETS

The drain current is calculated by using Pao and Sah’s double integral [11], namely

(15)

where , is the intrinsic carrier con-centration, and is described in Table I. Here, is the electric field at the insulator/semiconductor interface given in [11]. The double integral over the band bending potential and the channel potential includes the integration over the width of depletion region and the channel length. The channel potential is the relative change of the electron quasi-Fermi po-tential along the channel position with respect to the source. In (15), both drift and diffusion currents have been considered and consequently can be used to investigate the drain current for an FeMFET operating in all possible regions such as sub-threshold, triode and saturation. In addition, the electric field and surface band bending potential are assumed not to be constant along the channel, which appears to be more relevant than the previous models [2], [3]. For an MFISFET, the gate voltage is given by

(16)

where

(17)

where

(11)   
where   
 (12)

|  |  |
| --- | --- |
| (13) | (18) |

|  |
| --- |
| and is the capacitance of semiconductor given in [10].  As for MFMIS capacitor in Fig. 2(b), the area of ferroelectric  is different from that of the insulator. Then (8) should be modi-  fied as |

(14)

Equations (11)–(13) describe the capacitance of semicon-ductor at low frequency. However, the capacitance at high frequency does not satisfy this relation at strong inversion. At high frequency, the generation rate of the charge carriers from the depletion region can not follow the rapid change of the applied signal and consequently the capacitance remains at the minimum value. Since the ordinary –  
 is measured at high frequency, we constrain the capacitance to the minimum value at the strong-inversion condition.

and or for

or , respectively. Here

is the same as that in Section II for the capacitors. Equations

(16) and (17) can be used to solve for and by Newton’s

method. The gate voltage and drain voltage can be

varied arbitrarily to obtain the desired current-voltage ( – )

relationship. Note that the value of must be sufficiently

large to ensure . In the case such that the

condition of no inversion is produced in the semiconductor

surface, FeMFET then will be operated in the cutoff region,

which is of no interest to us here.

The electric field, surface band bending and channel poten-

tials as a function of the channel position can be calculated based

on the original derivation of (15) [11]. With the fact that the

drain current is unchanged at every channel position, , we can

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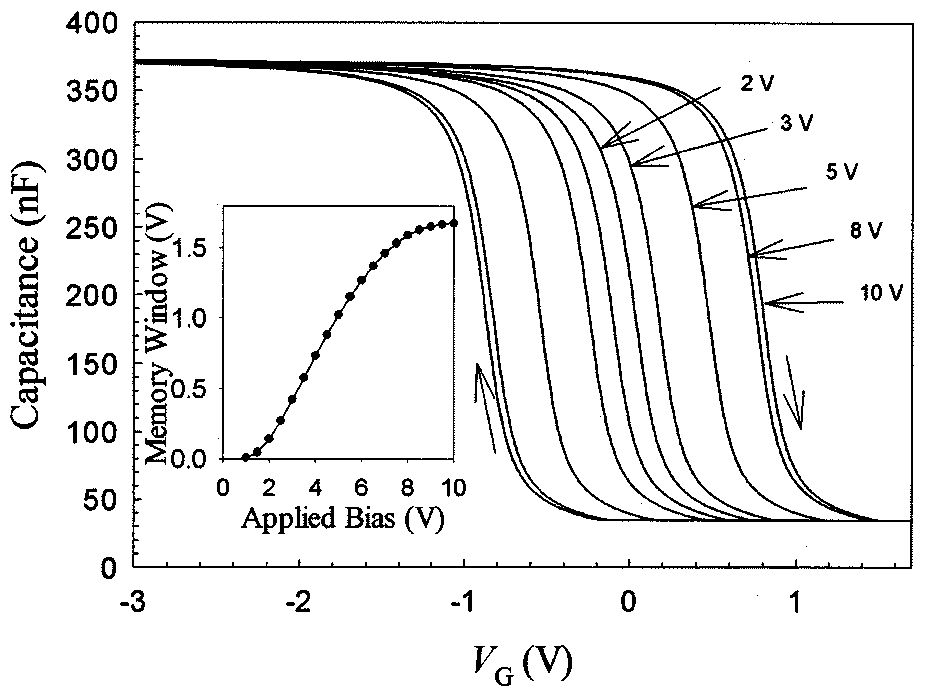


Fig. 3. C–V simulations of MFIS capacitor at various applied biases. The device parameters are defined in Table I. The inset shows the corresponding memory window as a function of applied bias.

integrate the drain current over the channel position. With the aid of the change of variable we then have

(19)

where the drain voltage is integrated to instead of . It seems to be a tedious task to solve (19) because it is an inte-gral equation. In fact, without any additional numerical calcu-lation there is a simple way of directly converting the - plot. Note that the channel position in (19) plot to the is more easily solved for a given channel potential because the right-hand side of (19) is simply the drain current if the drain voltage is . Therefore, if the - plot is first calcu- from 0 to   
 , then lated by changing the drain voltage can be simply converted to whereas just corresponds to the channel potential at this bias con- , and dition. Upon getting the , the corresponding are readily determined according to (16)–(18).

As for the MFMISFET, some different calculation procedures must be done because the floating metal gate will make the voltage across the ferroelectric uniform in the longitudinal direction. As shown in Fig. 2(b), an MFMISFET can, in effect, be treated as a series of an MOSFET and an MFM capacitor. Thus by separately investigating the behaviors for these two devices enable us to analyze the characteristics of an MFM-ISFET. At a low drain voltage, the stored charges in MOSFET are closely equal to those in MOS capacitor. In this case, (9) and (14) can be employed to determine the gate voltage of MOSFET and the drain current may be found from (15).

V. NUMERICAL RESULTS AND DISCUSSION

The simulations to be done are for both the capacitor and tran-sistor. The device and material parameters used in the present study are listed in Table I. The EOT of the insulator is set to be 4 nm and the ferroelectric is chosen to have a moderate polar-ization in order to obtain a suitable memory window at the low operation voltages.

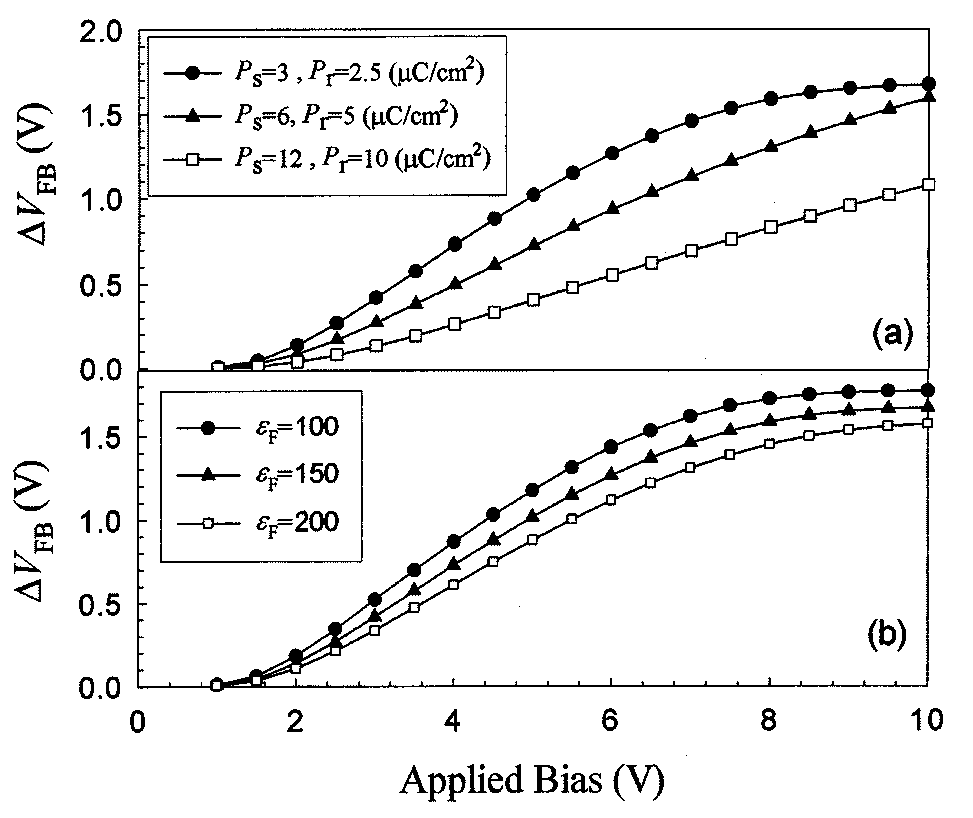


Fig. 4. Memory window as a function of applied bias of MFIS capacitor for (a) various P with a constant ratio of P =P = 5=6 and (b) various " . The other parameters are the same as Table I.

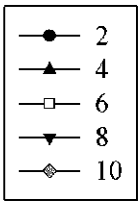
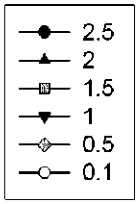
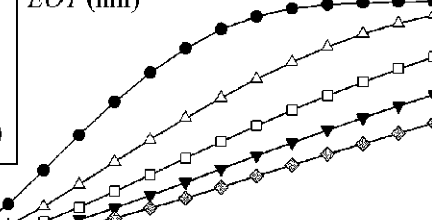
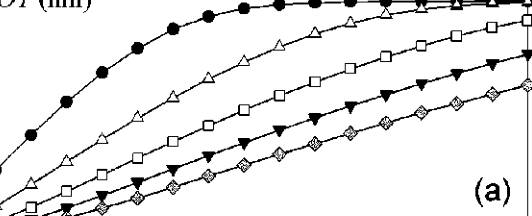
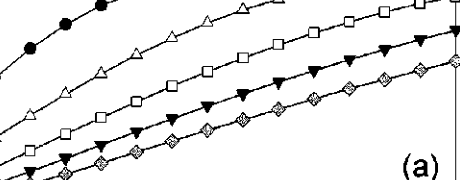
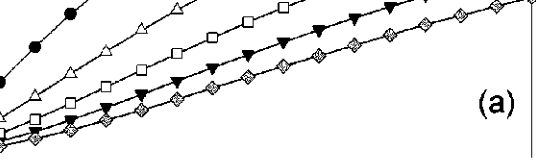
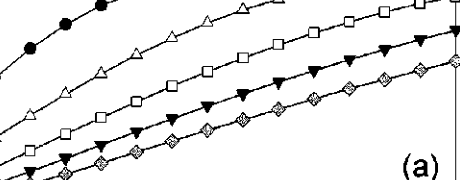
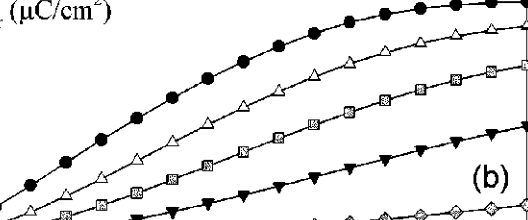
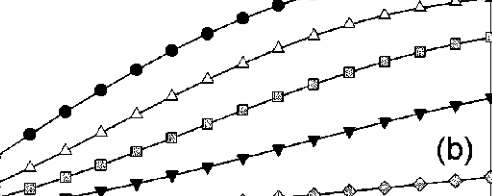
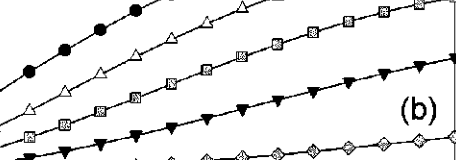
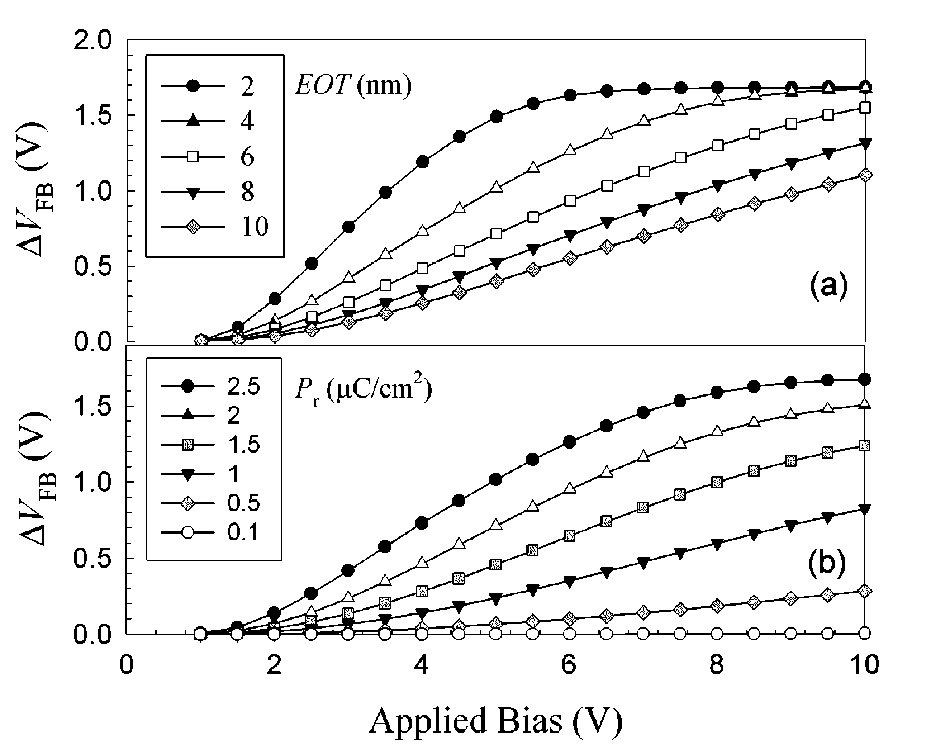
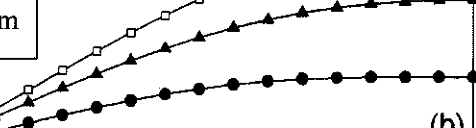
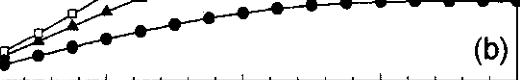
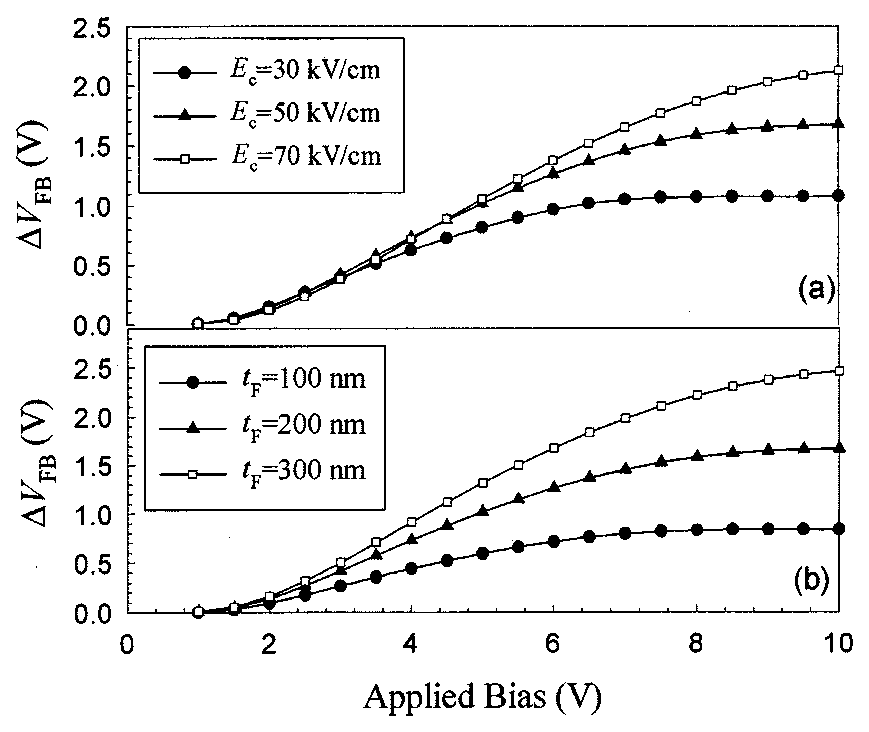
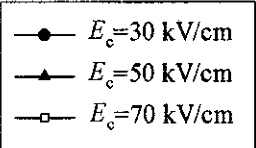
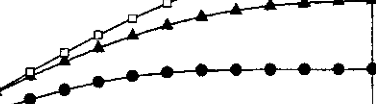
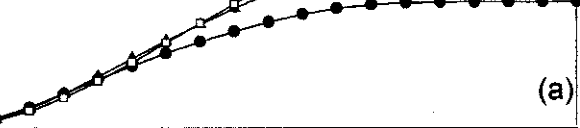
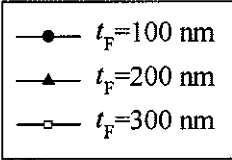
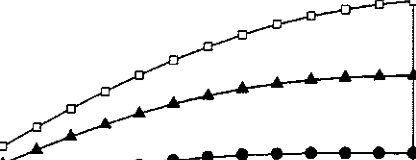
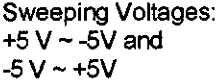
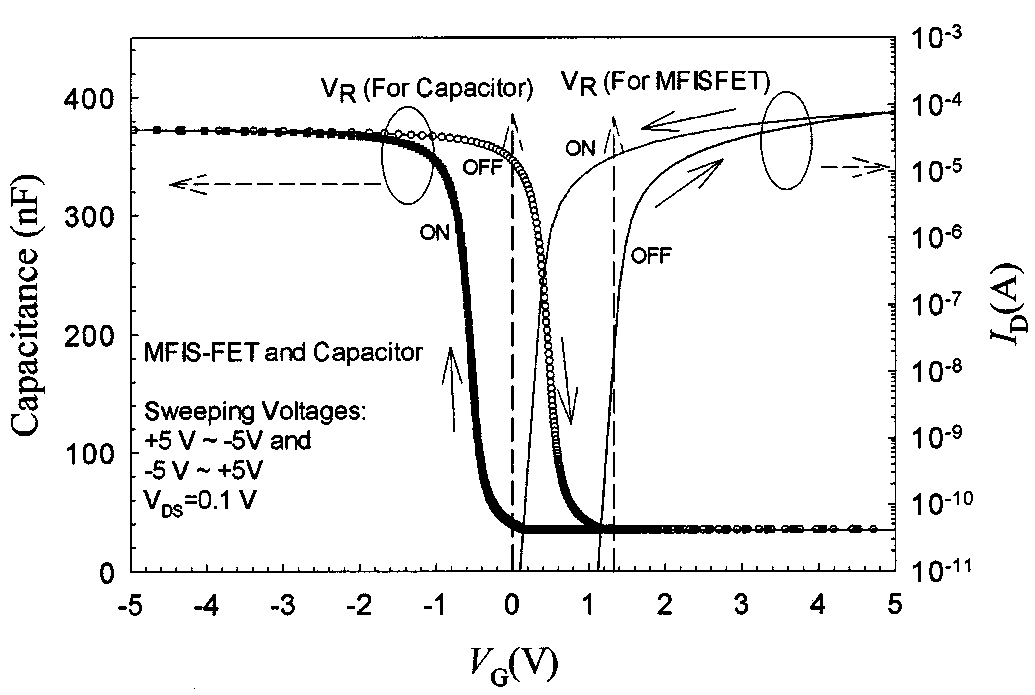
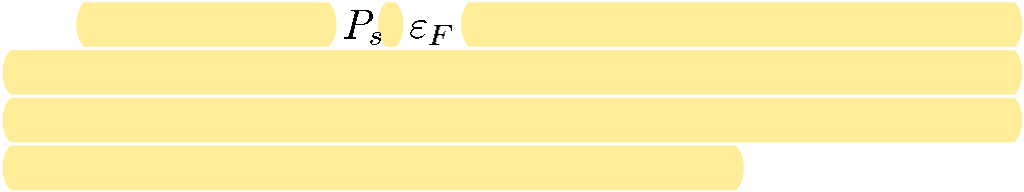
In Fig. 3, we plot the – memory window for an MFIS capacitor. The window is opened wider as the bias voltage is increased, reaching a saturated value for a larger applied bias as displayed in the inset of Fig. 3. The memory window width is defined as the flat-band voltage shift of the two aligned di-rections of the polarizations. At flat-band condition,   
and then both and the polarization of ferroelectric film are equal to zero according to (11) and(12). Thus the flat-band gate voltage is simply the voltage in ferroelectric, . The max-imum memory window at large bias can be calculated by , where   
 is the electric field with zero polarization. Accord-ingly, the maximum memory window under large applied bias can then be derived as

(20)

Equation (20) agrees with the maximum value obtained in the inset of Fig. 3.

Although it is common to recognize that the hysteresis di-rection for – curve should follow the direction in Fig. 3, its physical reason however is rarely given thus far. We now give ), an explanation on it. If one applies a writing voltage (   
then the electric field generated in the ferroelectric and the in-sulator should be negative-valued according to the sign conven-tion in Fig. 2. The polarization will then follow the lower branch based on the description in Section II. At the flat-band con-dition, the polarization is zero and the corresponding electric field is positive-valued. Hence the flat-band gate voltage is pos-itive. Similarly, the flat-band gate voltage is negative for a pos-itive writing voltage ( ). Consequently, the hysteresis loop will trace the clockwise direction as demonstrated in Fig. 3. Likewise, the hysteresis loop will trace counterclockwise direc-tion for an -type substrate.

Shown in Figs. 4–6 are the memory windows as a function of bias voltage at various material parameters for an MFIS ca-pacitor. Figs. 4(a), (b) and 5(a) show the effect of , and EOT on the memory window, respectively. The results imply



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Fig. 5. Memory window as a function of applied bias of MFIS capacitor at different values of (a) EOT of insulator and (b) P at the condition of a constant value of P . The other parameters are the same as Table I.

Fig. 6. Memory window as a function of applied bias of MFIS capacitor for various values of (a) E and (b) t . The other parameters are the same as Table I.

that the decrease in , and EOT is necessary for capaci-tance matching of the ferroelectric and insulator layers so that the voltage drop in the ferroelectric layer can be increased to drive the ferroelectric into larger minor loop. Fig. 5(b) shows the memory window versus bias voltage at various values of . The memory window is enhanced with increasing for a fixed . Several literatures [5] have stated that a small polarization ( C cm ) is sufficient to obtain the memory window. We think that this assumption is incorrect because a small value of would result in the linear-like P–E curve, leading the ferro-electric to behave closely to the paraelectric phase. The memory window for C cm is very small, as indicated in Fig. 5(b). Therefore, increasing the ratio , or equivalently obtaining a square-like hysteresis loop, is essential for obtaining a large memory window.

Fig. 6 illustrates the effects of coercive field and thickness of ferroelectric layer on the memory window. Larger values in and generally increase the memory windows at the same writing voltage but the writing voltage should be increased to obtain the saturated memory window. Although increasing

Fig. 7. C–V and I –V simulations of MFIS capacitor and MFISFET. The device parameters are given in Table I. The direction of memory window is also shown here.

and enhance the memory window, the devices are operated in a smaller minor hysteresis loop at low operation voltages. We believe the ferroelectric thin film in the saturated polarization is more stable (such as retention characteristics) than that in a minor loop. Therefore, certain trade-off should be made to op-timize the material parameters.

Both – relationship of MFIS capacitor and – curve of MFISFET are shown in Fig. 7 for the purpose of comparison. The drain current shows a similar memory window to the –curve. The results shown here indicate that the threshold volt-ages of these two states are effectively separated by the two di-rections of polarization in the ferroelectric and then can be iden-tified as two states: “ON “ and “OFF”. In order to have a better sense margin, a suitable choice of for an FeMFET is shown in Fig. 7 in which the drain current ratio ON   
 OFF is larger than 10 , suitable for memory operation.

Reported studies in the literatures mostly focused only on MFIS capacitors because they are easy to fabricate and useful for material characterization. For MFIS capacitor, a suitable reading voltage must be selected so that the difference in capacitance is large, as seen in Fig. 7. However, for MFIS capacitor is different from that for FeMFET. Therefore, it is worthy of mentioning that if measurements such as retention and fatigue issues are carried out with a defined , one then should note that the measured results for both MFIS capacitor and FeMFET may be different because of their distinct values in .

Fig. 8 demonstrates the drain current as a function of the drain voltage for both ON- and OFF-state. We can see that the drain current of OFF-state is less than that of ON-state at the same bias condition. A simple insight can be gained from this figure. The threshold voltage of ON-state is smaller than that of OFF-state by about 1 V, namely the drain current of ON-state at V V. Likewise, the drain is close to that of OFF state with current at V (ON) is close to that at V (OFF). Fig. 9 shows the drain current versus gate voltage at various writing voltages of 3 V 10 V. The memory window of the drain current increases with increasing writing voltage, which is similar to – curves indicated in Fig. 3. The inset is the corresponding P–E curve of the ferroelectric layer for each state.

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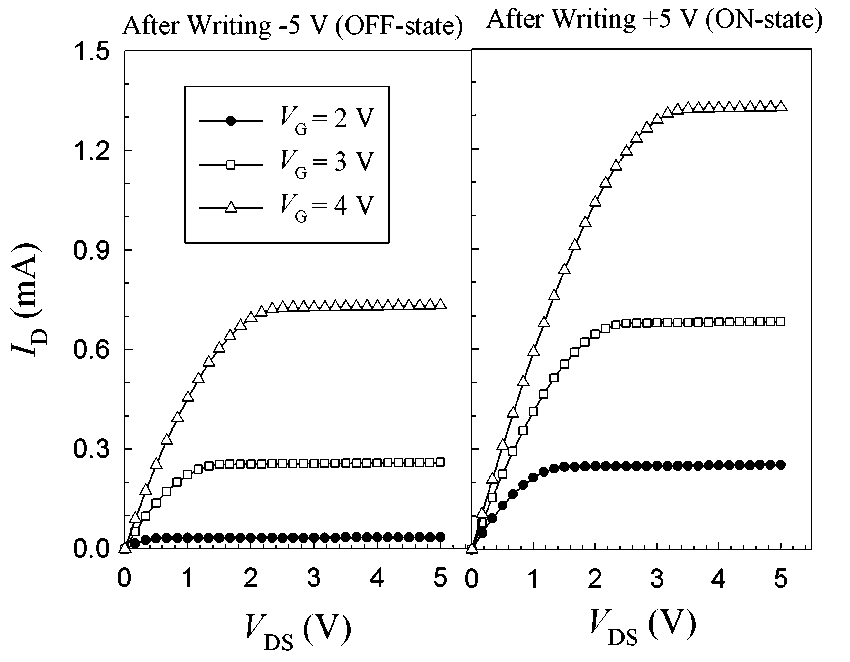


Fig. 8. I -V simulations of MFISFET for the ON and OFF states with various V . The device parameters are given in Table I.

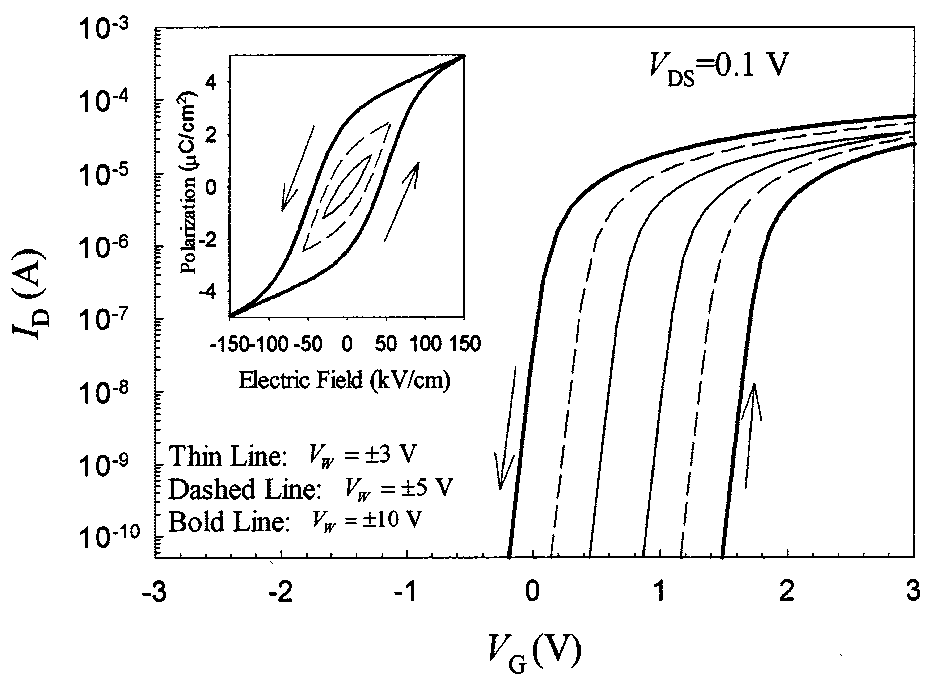


Fig. 9. I -V simulations of MFISFET for various writing voltages, V . The device parameters are given in Table I. The inset shows the corresponding P–E relations of the ferroelectric material.

The results indicate that a larger writing voltage would enhance the polarization to a larger minor hysteresis loop.

The channel potential (or electron quasi-Fermi potential), sur-face band bending, space charge density, and are shown in Figs. 10–12. Fig. 10 shows the results of channel potential, in which we employ the plot of drain current versus drain bias in the inset. The maximum drain voltage is taken to be high (15 V) to clearly illustrate the after pinchoff (or saturation re-gion) behavior. The band bending and channel potential gener-ally increase from the source to drain. When the drain voltage is larger than about - (where is the threshold voltage), the channel becomes “pinchoff” and the band bending is con-stant, as shown in Fig. 11. The space charge density near the drain attains a very small value and the depletion region mainly contributes to the remnant space charges. As seen in Fig. 10, the electron quasi-Fermi potential ( ) drops pronouncedly from the drain to the pinchoff point. This causes a large gradient in the quasi-Fermi potential and it will compensate the small space charge density and keep the drain current constant. In Fig. 12, it is indicated that both   
 and decrease from the source to the drain. The will decrease to a very small value after pin-choff while there is still a remanent value of . In the calcu-

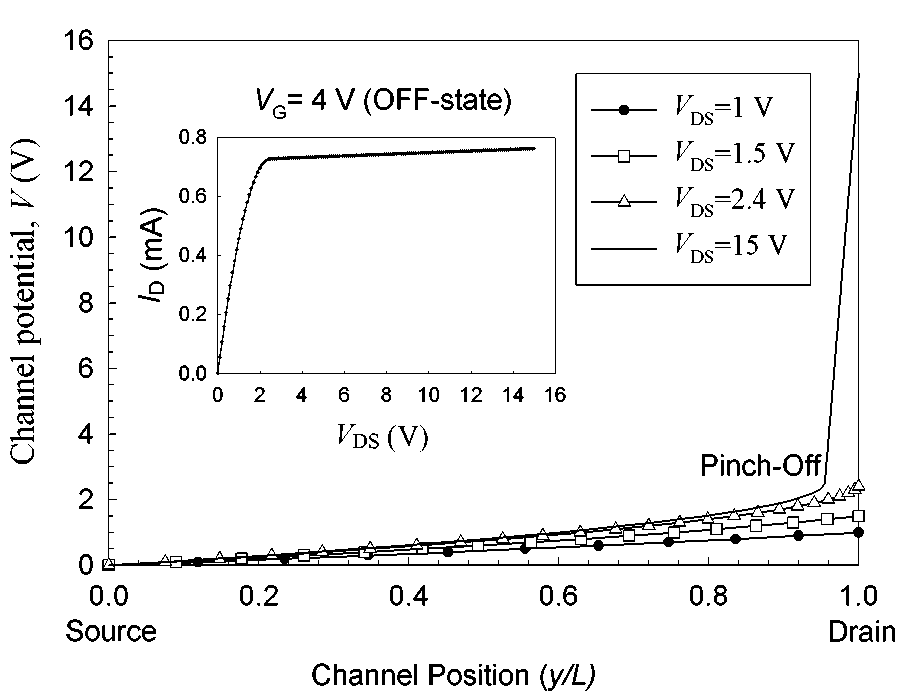


Fig. 10. Channel potential V as a function of the channel position for various drain voltages of MFISFET. The inset shows the plot of I -V at V = 4 V for the OFF state in Fig. 8.

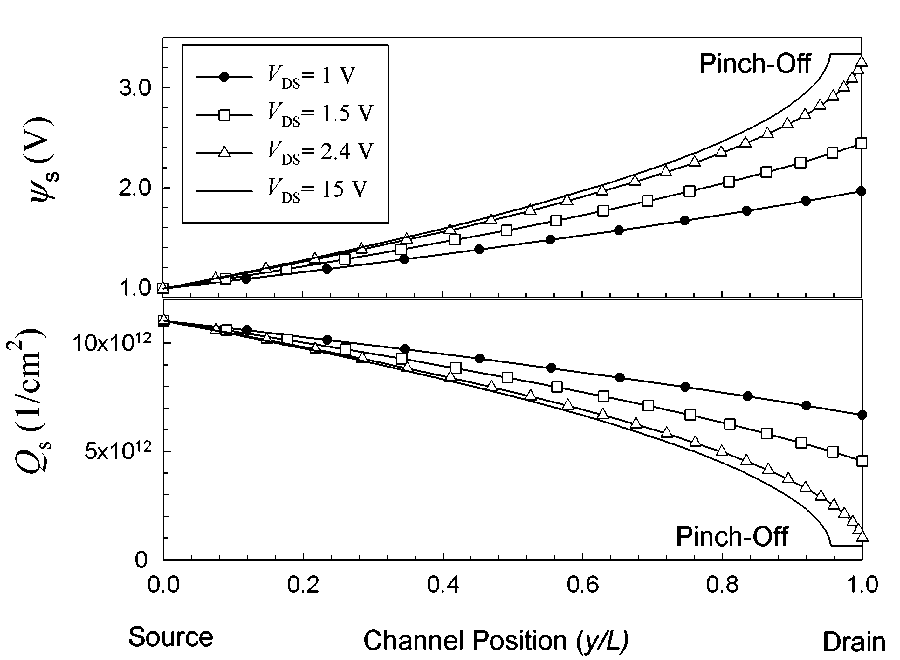


Fig. 11. Surface band bendingand Surface charge density Q as a function of the channel position for various drain voltages of MFISFET.

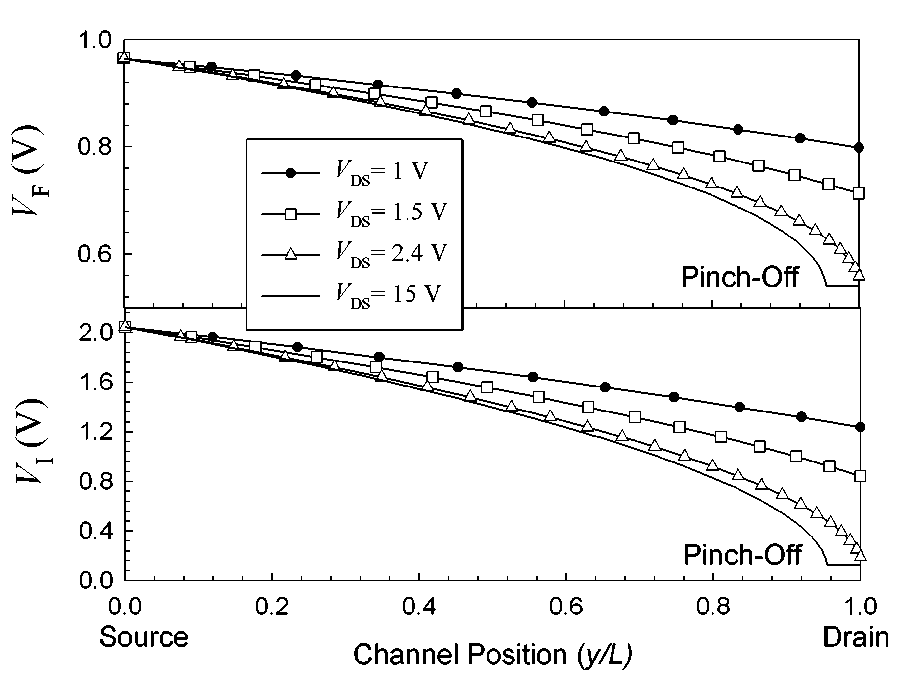


Fig. 12. Voltage drop across the ferroelectric layer V and insulator layer V as a function of the channel position for various drain voltages of MFISFET.

lation of Miller *et al.* [2], the voltages in the insulator and the ferroelectric have been assumed to be constant for convenience. This assumption would lead to a large deviation at a large drain voltage. However, in our model here, we remove this limitation and the distributions of voltages are calculated as well.

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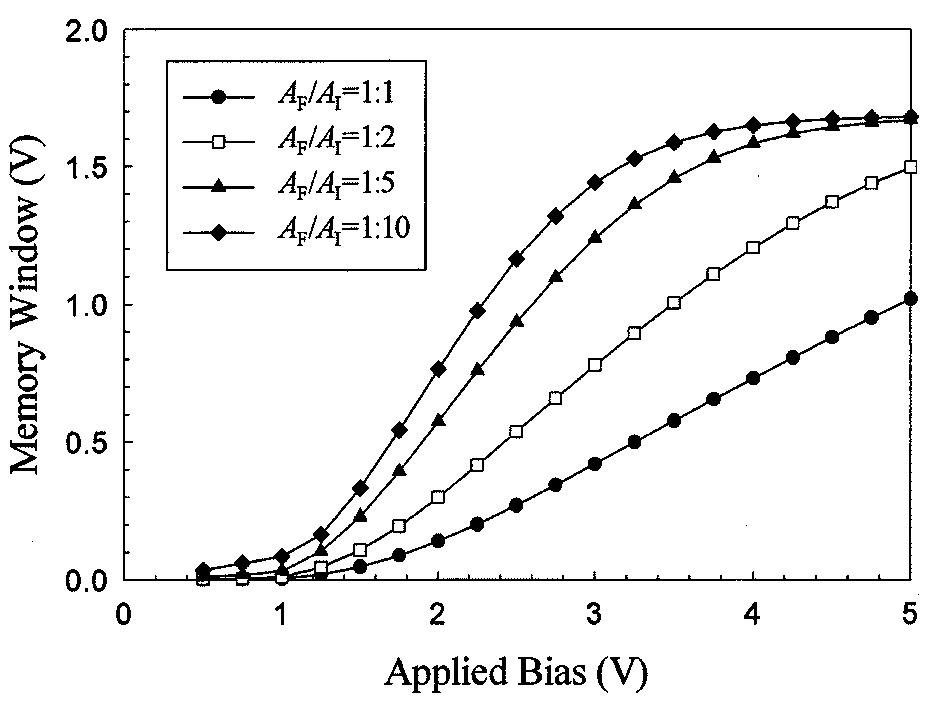
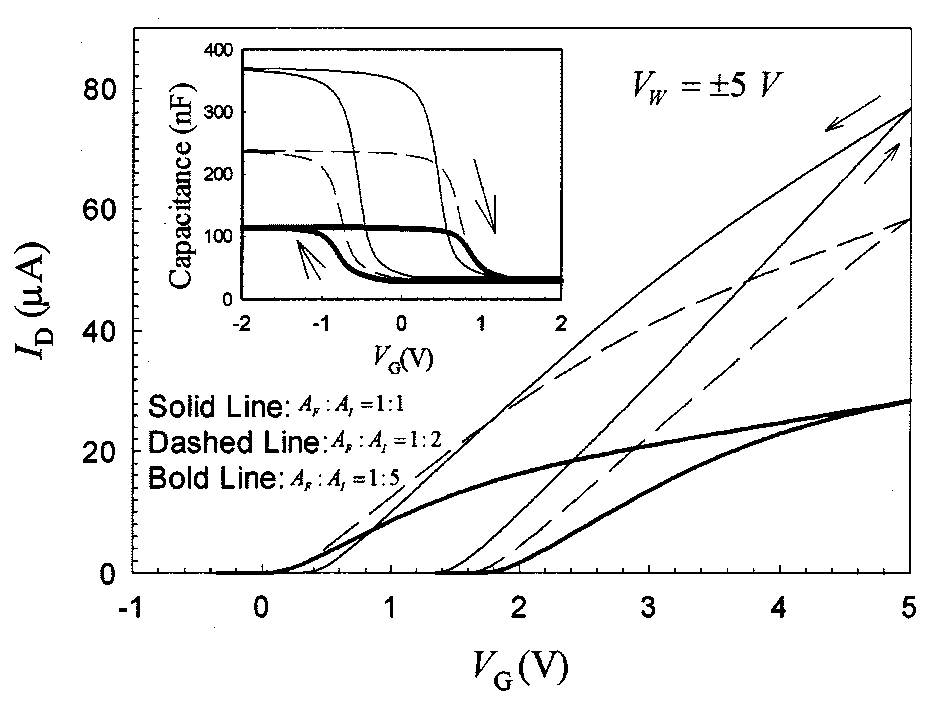


Fig. 13. Memory windows as a function of applied bias of MFMIS capacitor with various area ratios A =A . The other parameters are the same as Table I.



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| Fig. 14. I –V simulations for MFMISFETs with various area ratios  A =A . The other device parameters are given in Table I. The inset is the  corresponding C–V relation of MFMIS capacitors with the same A =A as  in MFMISFETs.  For MFMIS capacitor, the memory windows increase with  decreasing area ratio, , as shown in Fig. 13. For a small  value in area ratio, the memory window increases with applied  bias and attains the maximum memory window rapidly. Fig. 14 | | | | |
| displays the | – | of MFMISFET and | – | of MFMIS capac- |
| itor for various area ratios at the writing voltages of 5 V. The  memory window increases from 1 V to 1.7 V as the area ratio  decreases from 1 to 0.2. The MFMIS structures with small area  ratio can easily drive the ferroelectric layer to saturated polar- | | | | |
| ization, which is more stable than a minor loop and is expected to have a longer retention time [6], [7] and better repeatability of threshold voltage during switching. However, the accumulation capacitance and the drain current decrease when the area ratio is decreased. This phenomenon is due to the decrease in total gate capacitance of the MFMIS structure that arises from the de-crease of area of MFM, as shown in the inset of Fig. 14. The de-creasing drain current effectively reduces the current ON/OFF ratio in spite of the increasing memory window, which is a draw-back of the device performance. The device designers, therefore, should make certain tradeoffs between the memory window and the drain current when the area ratio decreases. | | | | |

VI. OTHER POSSIBLE EFFECTS

*A. Fixed Charges*

For an MFIS structure, the fixed charges may reside at the interface of ferroelectric/insulator or of insulator/semicon-ductor. Denoting respectively the fixed charges as and , Gauss’s law then gives

(21)

and

(22)

|  |
| --- |
| With the existences of and , the voltages across the  insulator and ferroelectric should change to and , respec-  tively. Although (22) cannot be solved in an analytical form, we  can expand the solution in the first —order term and the total  shift in the gate voltage due to the fixed charge is then given by |

(23)

*B. Charge Injection*

In recent developments of MFIS structures there are many high dielectric constant materials for the insulators. However, with their small bandgaps and polycrystalline structures, they often have large leakage currents and low breakdown voltages. If the device parameter is not carefully designed, the applied voltage mostly lies in the insulator rather than in the ferroelec-tric film, causing a large leakage current or even breakdown. In addition, the interdiffusion problems often generate a large den-sity of trap states, in which the charges may be stored. These ef-fects cause charge injection, which is similar to the operation of flash memory. For example, if a large and negative gate voltage is applied to MFIS capacitor, a positive will be generated due to the leakage currents in the insulator, leading to a nega-tive shift (23) in flat-band voltage. Similarly, a large and positive gate voltage will induce a negative   
 , producing a positive shift in flat-band voltage. Note also that this charge injection can cause a hysteresis loop but with a reverse direction in the ferroelectric memory hysteresis loop. Accordingly, the charge injection will reduce the ferroelectric memory window or even results in the wrong hysteresis direction.

*C. Short-Channel Effect*

In Section IV, the current-voltage relationship is calculated from Pao and Sah’s double integral. This formula is derived on the basis of the gradual channel approximation, in which the transverse electric field is much greater than the longitu-dinal one. However, for a short channel device, the influence of source/drain region on the channel and the effect of velocity saturation become important. The overall short channel effects will eventually reduce the drain current that is less than the value estimated in Section IV and increase the subthreshold slope. However, we believe the threshold voltage change between the two polarization states are still close to the estimated using our

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method, at least in the first order. There also exist many compli-cated effects. For example, the thickness of ferroelectric film in-corporated in FeMFET is often several thousands of angstroms, which is comparable to the channel length if submicron tran-sistor is fabricated. Therefore, the fringing electric fields exist outside the gate area and this effect in turn reduces the gate con-trol capabilities of the transistors. This similar effect has been proposed by Chen *et al.* [12] for the transistors made of high-gate dielectrics.

VII. CONCLUSION

In summary, some detailed numerical analyses of MFISFET, MFMISFET, and the associated capacitors have been made for the various material and device parameters. We have presented a new simple and analytical P–E relation for the ferroelectric material, including the nonsaturated polarization. Based on this analytical formula along with Pao and Sah’s double integral for the drain current, the electrical characteristics of the above de-vices can be investigated. First, we have successfully simulated the – memory windows at various applied biases. A simple and clear explanation on the direction of the memory window is also given. Second, the nonuniform distributions of the field and charge along the channel position of the FeMFETs have been taken into account from Pao and Sah’s double integral. The drain current of the FeMFETs operated in all possible regions except the cut-off region can be calculated by this way. Third, other possible effects such as fixed charge, charge injection and the short channel effect are also addressed in the present study. For the MFIS and MFMIS structures, we have found some useful design rules for improving the device performance: De-creasing and , increasing   
 ratio and reducing EOT of the insulators and of the MFMIS structures are the important factors to obtain a saturated memory window at a low operation voltage. Increasing and may also result in a larger memory window, while the voltage required to drive the ferroelectric into saturated polarization is higher. In addition to the memory window, other issues should also be considered. For example, decreasing and , reducing of the MFMIS structures and increasing will reduce the drain current and then the current ON/OFF ratio is decreased. Care must be taken to avoid possible breakdown or charge injection of the insulator due to the small thicknesses and high voltage drops across them. Besides, it is suggested to operate the FeMFETs in saturated po-larizations for better retention characteristics. Therefore to op-timize the device performances, certain tradeoff between these parameters should be made. If some clear device specifications are given, the present simulation method can provide the opti-mization of the device parameters.

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