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Low Voltage Operation of Nonvolatile Metal-Ferroelectric-Metal-Insulator-Semiconductor

(MFMIS)-Field-Effect-Transistors (FETs) Using Pt/SrBi2Ta2O9/Pt/SrTa2O6/SiON/Si Structures

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**Low Voltage Operation of Nonvolatile**   
**Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS)-Field-Effect-Transistors (FETs) Using Pt/SrBi2Ta2O9/Pt/SrTa2O6/SiON/Si Structures**   
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We report p-channel metal-ferroelectric-metal-insulator-semiconductor (MFMIS)-field-effect-transistors (FETs) which can op-erate at a voltage as low as 3.5 V using Pt/SrBi2Ta2O9/Pt/SrTa2O6/SiON/Si structures. It is shown that the use of the saturated *P*–*E* hysteresis loop is effective to improve the data retention time. To utilize the saturated *P*–*E* loop, MFMIS-FETs with a large *S*M*/S*F ratio are fabricated. We demonstrate the nonvolatile memory function of the p-channel MFMIS-FETs with a mem-ory window of 1.5 V, operating at ±3*.*5 V. It was also found that the fabricated MFMIS-FETs have fairly good data retention characteristics.

KEYWORDS: ferroelectric memory, ferroelectric-gate transistor, MFMIS-FET, SrBi2Ta2O9, SrTa2O6

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| **1.** | **Introduction** | | | |
| Recently, ferroelectric-gate field-effect-transistors  (FETs)1–4)have attracted much attention for nonvolatile | | | | |
| memory applications. | | | Using | ferroelectric-gate FETs, |
| one-transistor-cell type nonvolatile ferroelectric ran-  dom access memory (FeRAM) can be obtained and the  ferroelectric-gate FETs obey the scaling rule for high-density | | | | |
| implementation. | | Furthermore, in such “transistor-type” | | |
| FeRAMs, the stored data can be read out nondestructively. In addition, we have proposed the use of ferroelectric-gate FETs in neural network systems as analog memories to store synaptic weights.5)We have also fabricated a neuron chip with a Pt/SrBi2Ta2O9/Si ferroelectric-gate FET and a pulse oscillation circuit, and demonstrated an “adaptive-learning”function.6)   To fabricate ferroelectric-gate FETs, ferroelectric materials have to be deposited on silicon substrates. Such a device is called a metal-ferroelectric-semiconductor (MFS) FET, How-ever, preparation of the ferroelectric/Si structure with good interface properties is extremely difficult. When ferroelectric SrBi2Ta2O9 (SBT) is directly grown on Si by the sol-gel tech-nique, a relatively thick (7–9 nm) transition layer, which is probably an SiO2 layer with poor electrical properties, can be unintentionally formed.7)Hence, it is a common technique to insert an insulating buffer layer between the ferroelectric ma-terial and Si to improve the interface properties. Such a struc-ture is called a metal-ferroelectric-insulator-semiconductor | | | | |
| (MFIS) structure. | | Another structure for ferroelectric gate | | |
| FETs is a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure, where a metal is additionally inserted be-tween the ferroelectric and insulating layers. The MFMIS structure has a merit that the area of an MFM ferroelectric capacitor (*S*F) and that of an MIS diode (*S*M) can be inde-pendently designed. It is important to note that the polariza-tions of well known ferroelectric films such as Pb(Zr, Ti)O3 (PZT) and SBT are much larger than the charge required for the control of the channel conductivity of FETs. By reducing the ferroelectric MFM capacitor size, *S*F, we can equivalently reduce the polarization of the ferroelectric film so that the po- | | | | |

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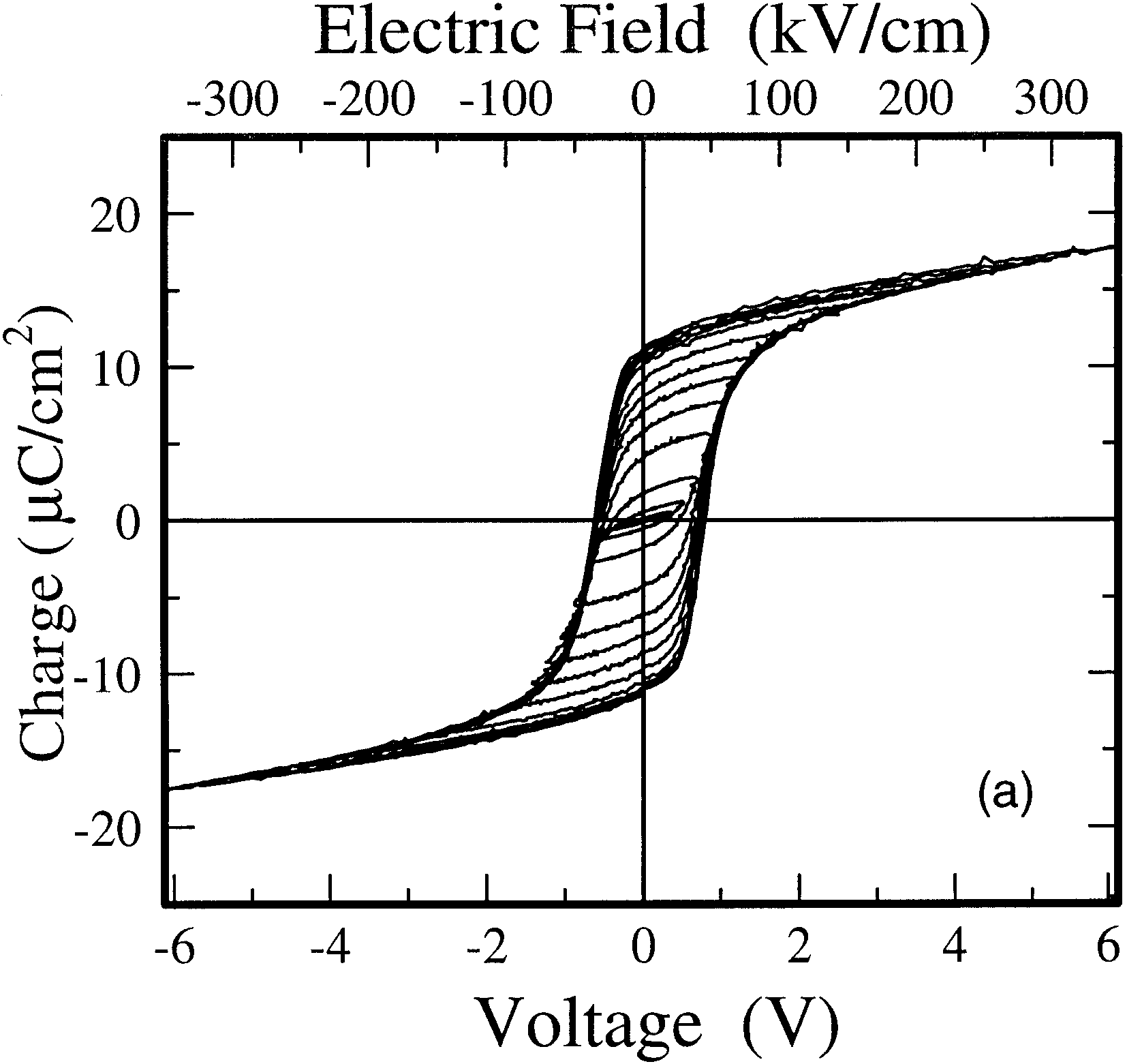
larization can match the induced charge of the MIS capacitor. So far, the MFIS and MFMIS structures have been com-monly used to fabricate ferroelectric-gate transistors.8–13) However, short data retention time and relatively high opera-tion voltage are major problems for ferroelectric-gate FETs fabricated so far. Furthermore, the design strategy to im-prove these drawbacks has not been established yet. In this paper, we show which device parameters are effective for low voltage operation and long data retention time. In particu-lar, we discuss how the electrical properties of MFMIS-FETs are affected by the thickness of the ferroelectric layer and the area ratio of Pt/SBT/Pt MFM capacitors to Pt/SiON/Si MISFETs. We demonstrate nonvolatile memory operation of Pt/SBT/Pt/SrTa2O6(STA)/SiON/Si MFMIS-FETs operat-ing at less than ±3*.*5 V which have fairly good data retention characteristics.

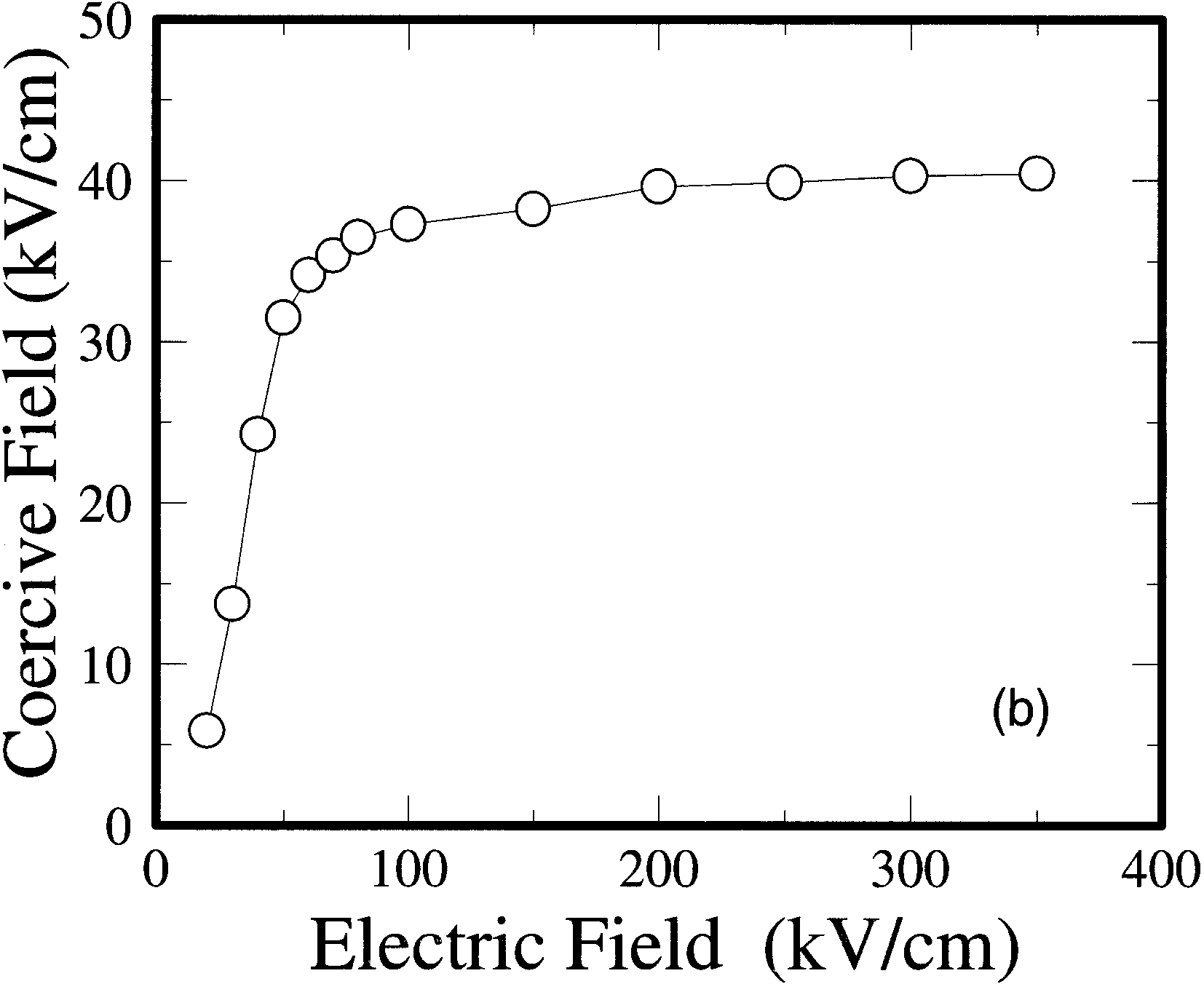
**2.**  **Retention Characteristics of MFM-MIS Structure**  **Diodes**

To clarify the basic behavior of the data degradation during the retention time, we first studied the data retention charac-teristics of MFM-MIS structure diodes. The Pt/SBT/Pt MFM capacitors and Al/STA/SiON/Si MIS diodes were separately fabricated and connected on a probe station. Before the mea-surements of the data retention characteristics, we confirmed ferroelectric properties of the SBT films used in this study. To obtain a long data retention time, it is important to use a ferroelectric film which has a *P*–*E* hysteresis loop with a large *P*r*/P*s ratio. In this work, we used a newly developed annealing method, face-to-face annealing technique, to fabri-cated ferroelectric SBT films by the sol-gel technique.14)SBT film was spin coated and dried at 160◦C in air, and then crys-tallized at 750◦C for 30 min in O2 ambient in the face-to-face configuration. The face-to-face annealing prevents the Bi re-evaporation from the SBT film during the crystallization pro-cess, which enhances the crystallization of SBT. We repeated the above process several times. The thickness of the SBT film was 175–250 nm. After Pt top electrodes were vacuum evaporated, the samples were annealed again at 750◦C for 30 min in O2 ambient. Figure 1(a) shows *P*–*E* characteristics

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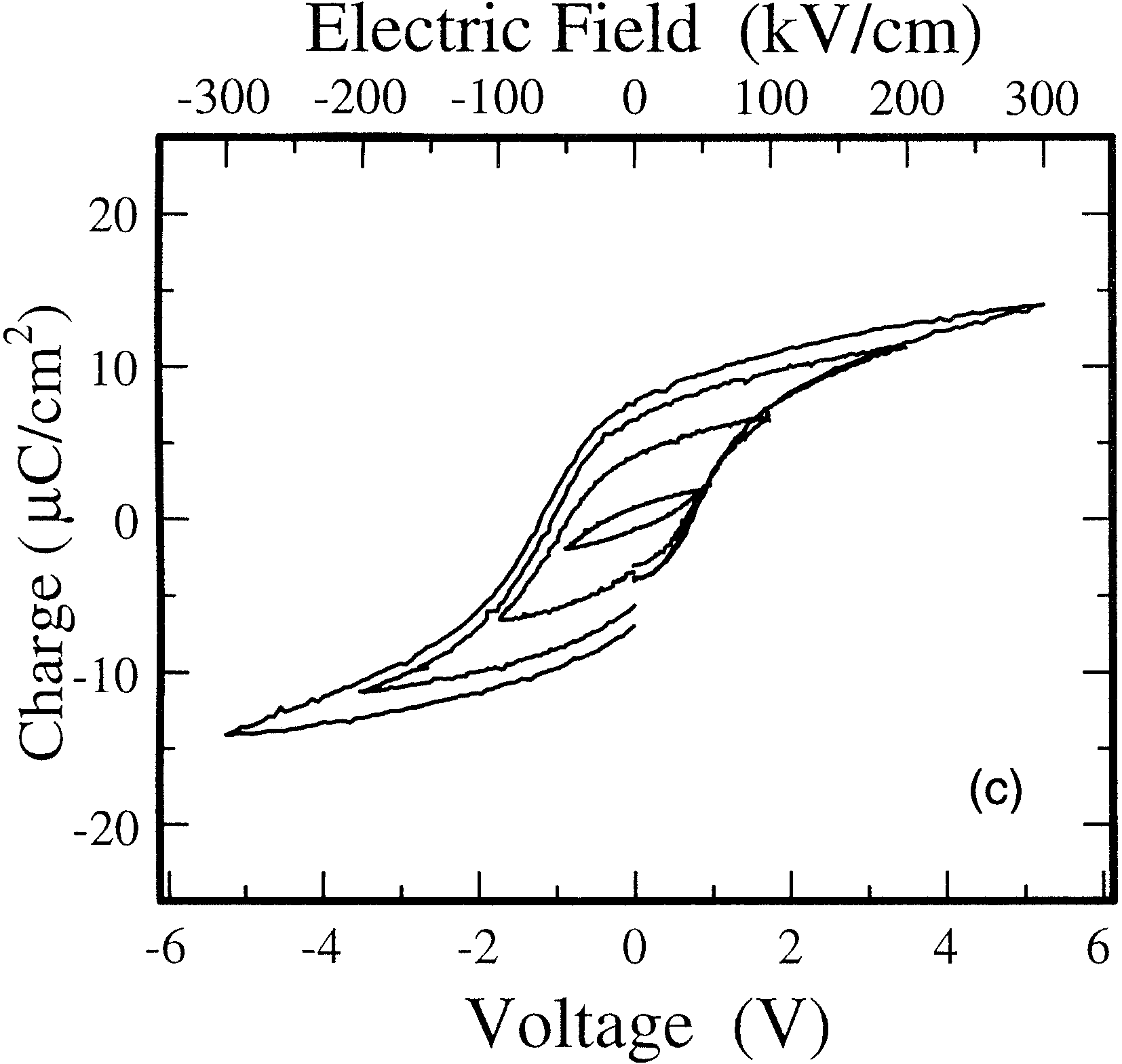


Fig. 1. (a) Typical *P*–*E* characteristics of 175 nm SBT film fabricated by the face-to-face annealing technique, (b) coercive field, *E*C, as a function of the applied electric filed, and (c) *P*–*E* characteristics of the SBT film when the face-to-face configuration is not used.

with various applied voltages of a Pt/SBT (175 nm)/Pt capaci-tor fabricated by the face-to-face annealing technique. Rema-nent polarization 2*P*r and coercive filed 2*E*C are 22 *µ*C/cm2 and 81 kV/cm, respectively, which are comparable to the best values reported in the literature. As shown in Fig. 1(a), the squareness of the *P*–*E* hysteresis loop is excellent. The leak-age current of the SBT film prepared by this technique is less than 10−7A/cm2. Figure 1(b) shows coercive field, *E*C, which

is an important parameter to estimate the memory window, as a function of the applied electric filed. The coercive field rapidly increases with the applied electric field and becomes almost constant when the applied electric field is larger than 70 kV/cm, which demonstrates the good saturation behav-ior of the coercive field in the SBT films used in this work. On the other hand, Fig. 1(c) shows *P*–*E* characteristics of a Pt/SBT/Pt capacitor fabricated with similar annealing con-ditions except that the face-to-face annealing technique was not employed. The electrical properties, such as *P*r and the squareness of the loop, are inferior to those of the sample fab-ricated by the face-to-face annealing.

In the MFIS and MFMIS structures, the ferroelectric and normal capacitors are connected in series. SiO2 is often used as an insulating buffer layer, because of the excellent inter-face properties of SiO2/Si. However, the SiO2 must be very thin, because widely studied ferroelectric materials such as PZT and SBT have very high dielectric constants. Further-more, reduction of the SiO2 thickness is practically limited because of the enhanced leakage current due to direct tunnel-ing. Consequently, the operation voltage for ferroelectric-gate FETs tends to be high in order to apply large enough volt-age for polarization reversal of the ferroelectric film. To pre-vent this, a high-dielectric-constant material should be used as the “I” layer. Furthermore, because of the insulating buffer layer, an electric field, so called “depolarization field”, is gen-erated in the ferroelectric layer when the gate is maintained at 0 V during the data retention, which is the main reason why the ferroelectric-gate FETs have poor data retention charac-teristics. It is important to use a large-capacitance “I” layer in the MFMIS structures to reduce the depolarization field, hence to obtain a long data retention time. In this work we use SrTa2O6(STA)/SiON stacked structure as the “I” layer. A relative dielectric constant of STA is as high as 110 and SiON is used to prevent undesirable oxidation of the Si wafer during the STA growth. We fabricated Al/STA/SiON/Si MIS structures as follows; first nitridation of the Si wafers was per-formed at 1050◦C for 5 s in NH3 ambient to form SiON layer. Then, 20–30 nm-thick STA films were formed by the sol-gel technique. STA films were spin-coated, dried at 160◦C in air and pre-annealed at 400◦C for 30 min in O2. The crystalliza-tion of STA was carried out at 900◦C for 3 min. The SiO2 equivalent thickness of the STA/SiON layer used in this work was 4–5 nm. The leakage current density of STA/SiON layer was as low as 1 × 10−8A/cm2.15) We now examine the electrical properties of MFM-MIS structures. The thickness of the SBT film used for the mea-surements is 250 nm. The area ratio of the MIS diode (*S*M) to the MFM capacitor (*S*F), *S*M*/S*F, used in the measurements is 4. Figure 2 shows capacitance–voltage (*C*–*V*) characteris-tics of the MFM-MIS structures. The solid line shows exper-imentally observed capacitance, while the open circles indi-cate the capacitances estimated from the separately measured charge-voltage (*Q*–*V* ) and *C*–*V* characteristics of MFM and MIS diodes. A counter-clockwise hysteresis loop as indicated by arrows in the figure is obtained, which is due to the ferro-electric properties of the SBT film connected to the MIS gate. The memory window is about 2.0 V. It is found that the ex-perimental values agree well with the calculated values. By comparing the calculated values with the measured value, we can estimate the electric field applied to the SBT layer. When

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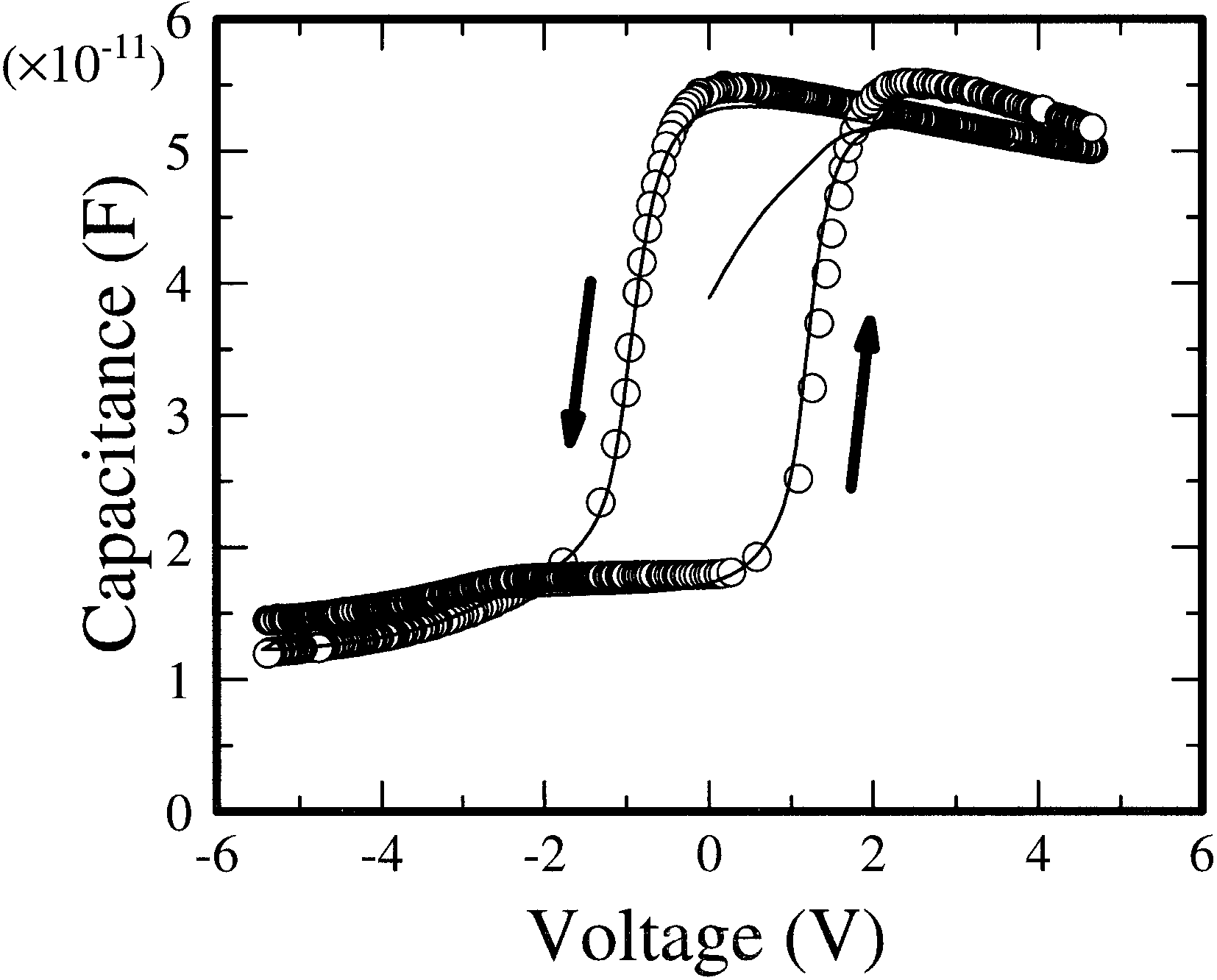
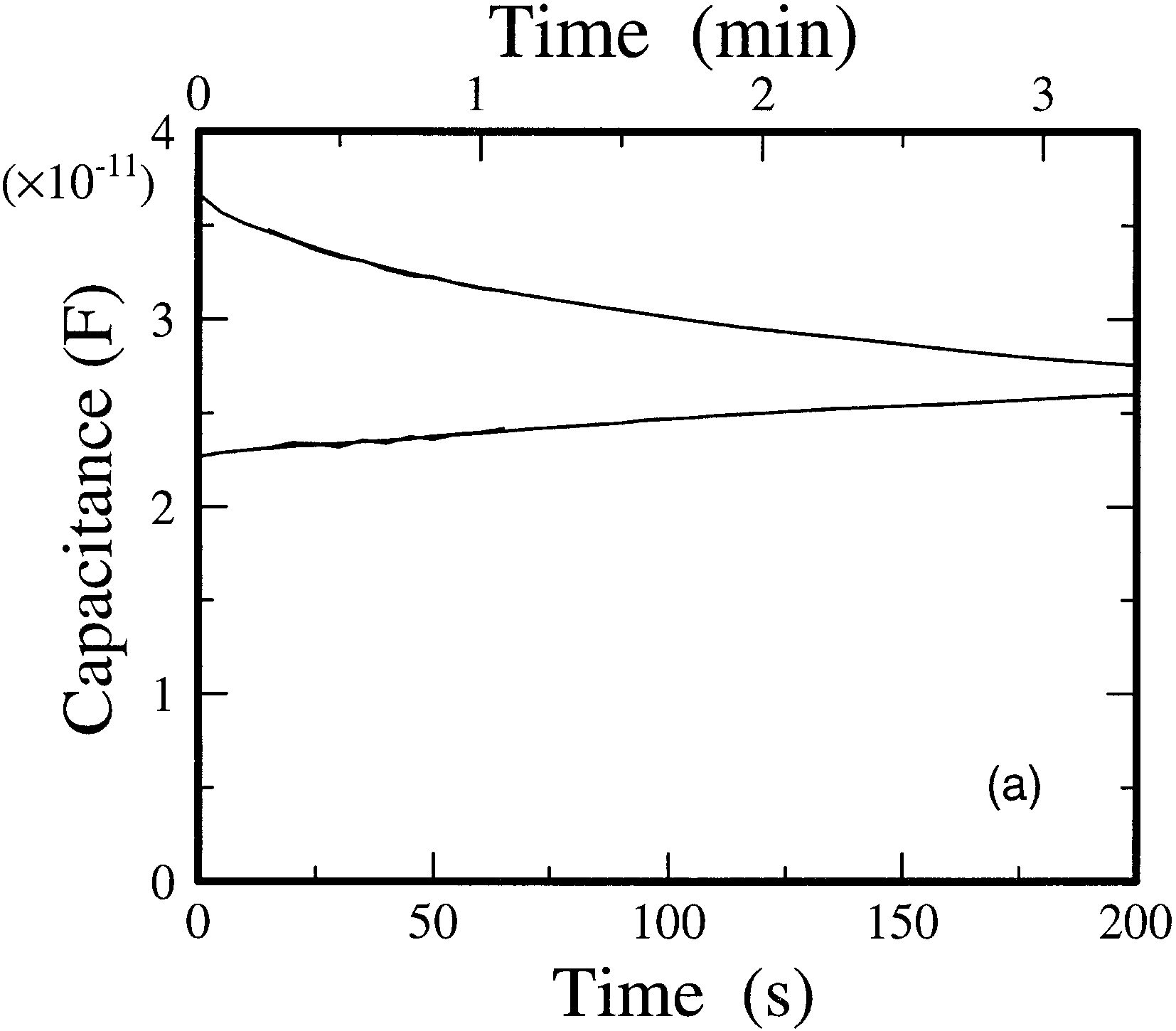


Fig. 2. *C*–*V*  characteristics of the MFM-MIS structures, where the Pt/SBT/Pt MFM capacitors and Al/STA/SiON/Si MIS diodes were sep- arately fabricated. The solid line shows experimentally observed capac- itance, while the open circles indicate the capacitances estimated from the separately measured *Q*–*V* and *C*–*V* characteristics of MFM and MIS diodes.



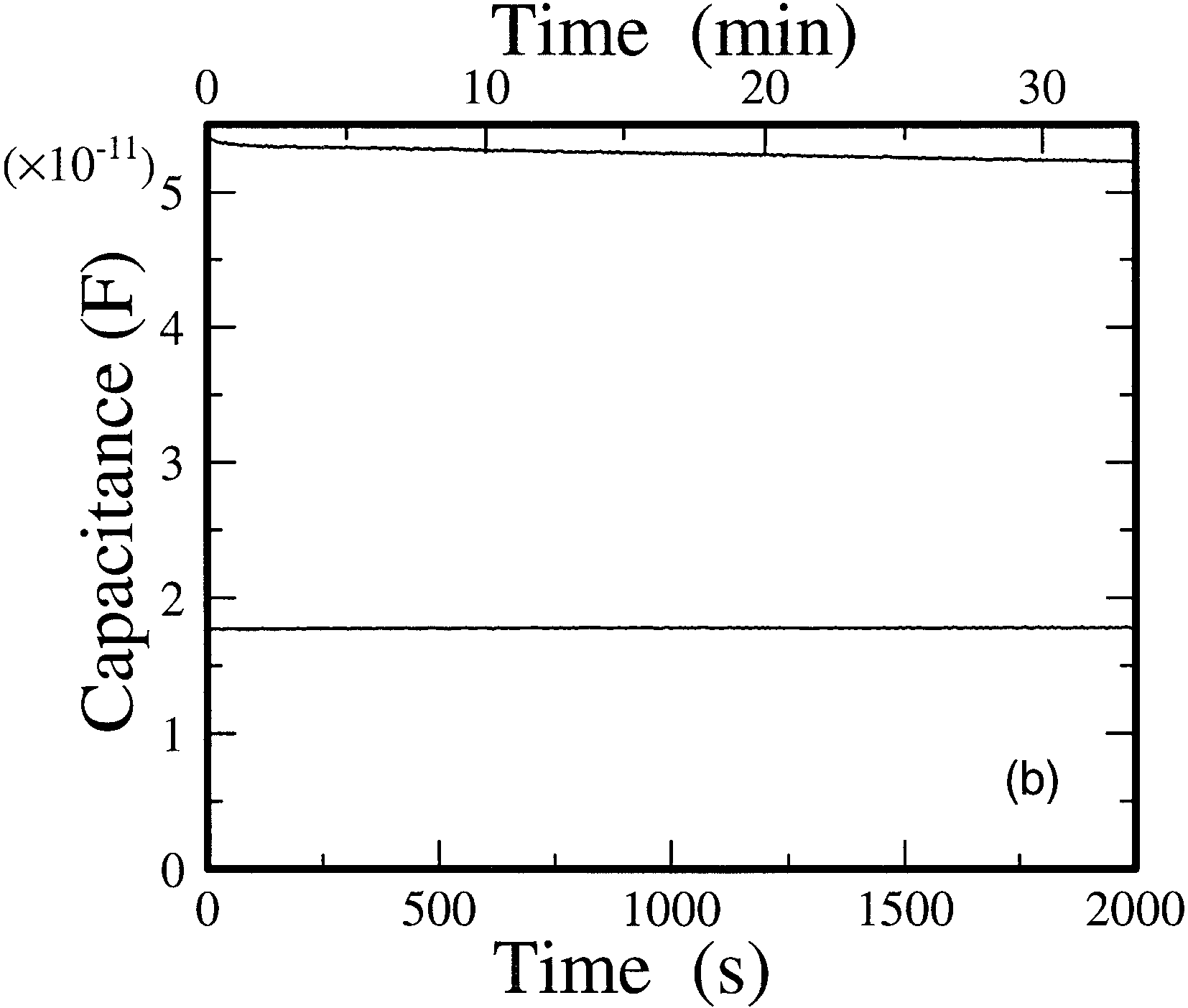


Fig. 3. Accumulation and inversion capacitances as a function of the data retention time for the MFM-MIS structure when (a) small and (b) large voltages are applied for programming.

the total voltage applied to the MFM-MIS structure is swept from +4*.*7 to −5*.*4 V, the estimated electric field applied to the SBT film is approximately 150 kV/cm. Hence, from the *P*–*E* hysteresis shown in Fig. 1(a), an almost saturated hys-teresis loop is used in the measured MFM-MIS structures.

Using this MFM-MIS structure, we measured the data retention characteristics with different programming volt-ages. Figure 3 shows the accumulation and inversion ca-pacitances as a function of the data retention time for the same MFM-MIS structure when small (50 kV/cm) and large (200 kV/cm) voltages are applied for programming. The de-polarization fields during the data retention are estimated to be 20 kV/cm and 25 kV/cm in Figs. 3(a) and 3(b), respec-tively. It is found that when the programming voltage is small, the capacitance change decreases rapidly with time and be-comes almost zero after 200 s. On the other hand, the data retention characteristics can be significantly improved by us-ing a large programming voltage even though the depolariza-tion fields during the data retention are about the same for both cases. This result suggests that saturated *P*–*E* hystere-sis is much more stable than a minor *P*–*E* loop when the ferroelectric capacitor is reversely biased (i.e., under depolar-ization field). Hence, it is important to use a saturated *P*–*E* hysteresis loop of the ferroelectric layer to obtain a long data retention time.

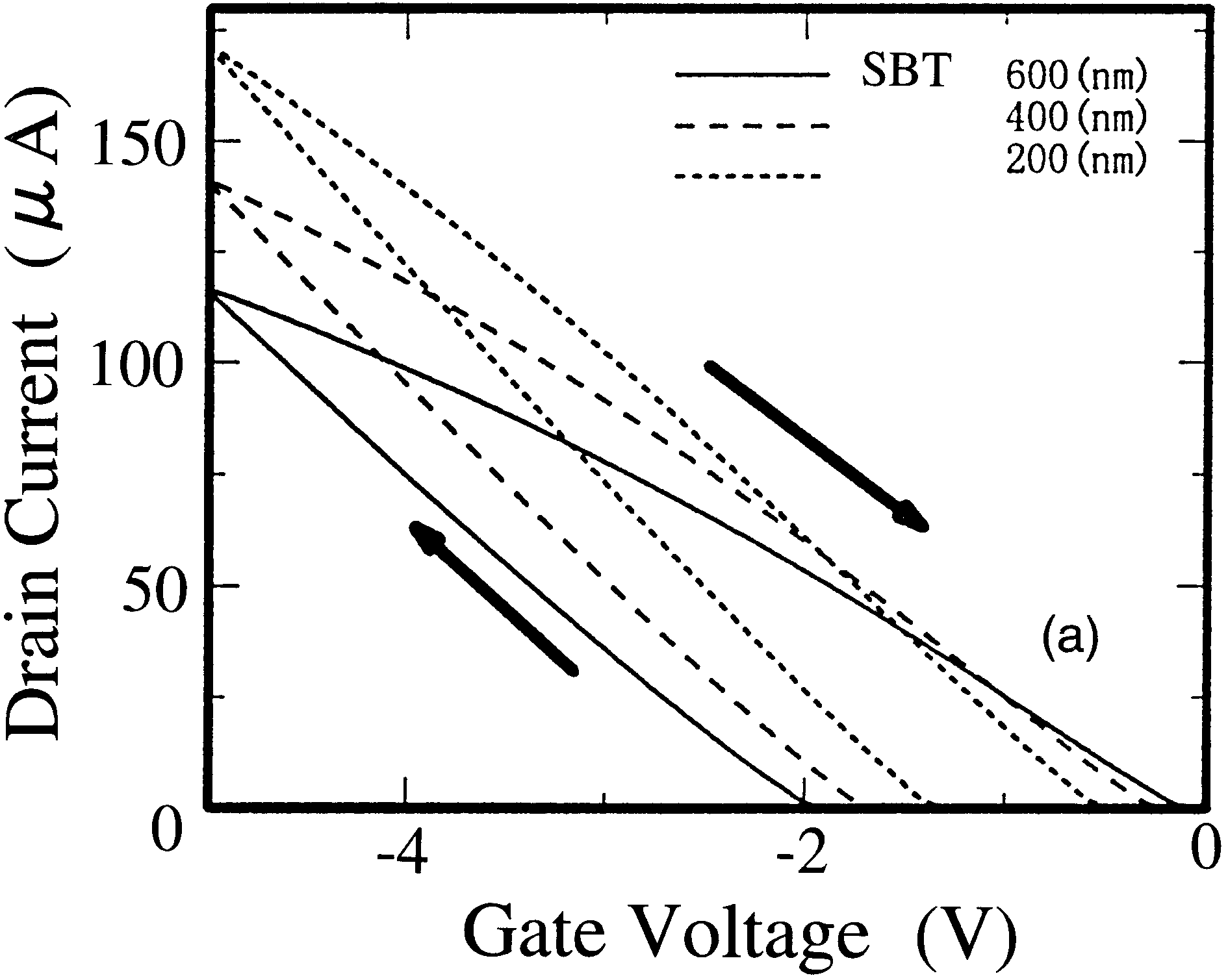
**3.**  **Simulation and Design of Ferroelectric-Gate FETs**

To design the MFMIS-FETs, the operation voltage and memory windows should be determined. From our previous work, it is reported that a subthreshold swing of the Pt/SBT/Pt/STA/SiON MFMIS-FETs is about Hence, to obtain the drain current 200–250 mV/decade.

on-off ratio larger than 5 orders of magnitude, the memory window of the MFMIS-FET should be larger than 1.25 V. In this section, we assume the MFMIS structures to obtain a memory window of more than 1.5 V with an operation volt-age of less than 5 V. We numerically simulated the transistor characteristics of MFIS and MFMIS-FETs using ferroelec-tric SBT films by Miller’s model.16)In the simulations, spon-taneous polarization *P*S, remanent polarization *P*r, coercive field *E*C, and relative dielectric constant *ε*r of the SBT films are assumed to be 13 *µ*C/cm2, 11.5 *µ*C/cm2, 40 kV/cm, and 200, respectively. These are typical values of the SBT films fabricated by the “face-to-face” annealing technique. The SiO2 equivalent thickness of STA/SiON “I” layer is assumed to be 4.5 nm.

We first calculated the drain current-gate voltage (*I*D–*V*G) characteristics of the MFIS structures with various SBT thick-nesses as shown in Fig. 4(a), assuming the operation voltage of 5 V. The SBT thickness is varied from 200 to 600 nm. Since the memory window is given by 2*V*C, to obtain a mem-ory window of more than 1.5 V, the SBT film must be thicker than 187.5 nm, if the coercive field *E*C of the SBT film is as-sumed to be 40 kV/cm. It is found that the memory window is as small as 0.75 V when the SBT thickness is 200 nm, whereas a large memory window can be obtained if we use a thick SBT film. However, in the MFIS structures, the used *P*–*E* hysteresis loop is one of the minor loops as shown in Fig. 4(b). Figure 4(b) shows the *P*–*E* hysteresis loops used in the MFIS structures with the SBT thicknesses of 200, 400, and 600 nm when ±5 V is applied. For the MFIS structure with a SBT film thickness of 200 nm, the electric field applied to the SBT film is only 35 kV/cm when 5 V is applied to the MFIS structure, which is smaller than the coercive field of the sat-urated *P*–*E* loop. When the SBT film thickness is increased

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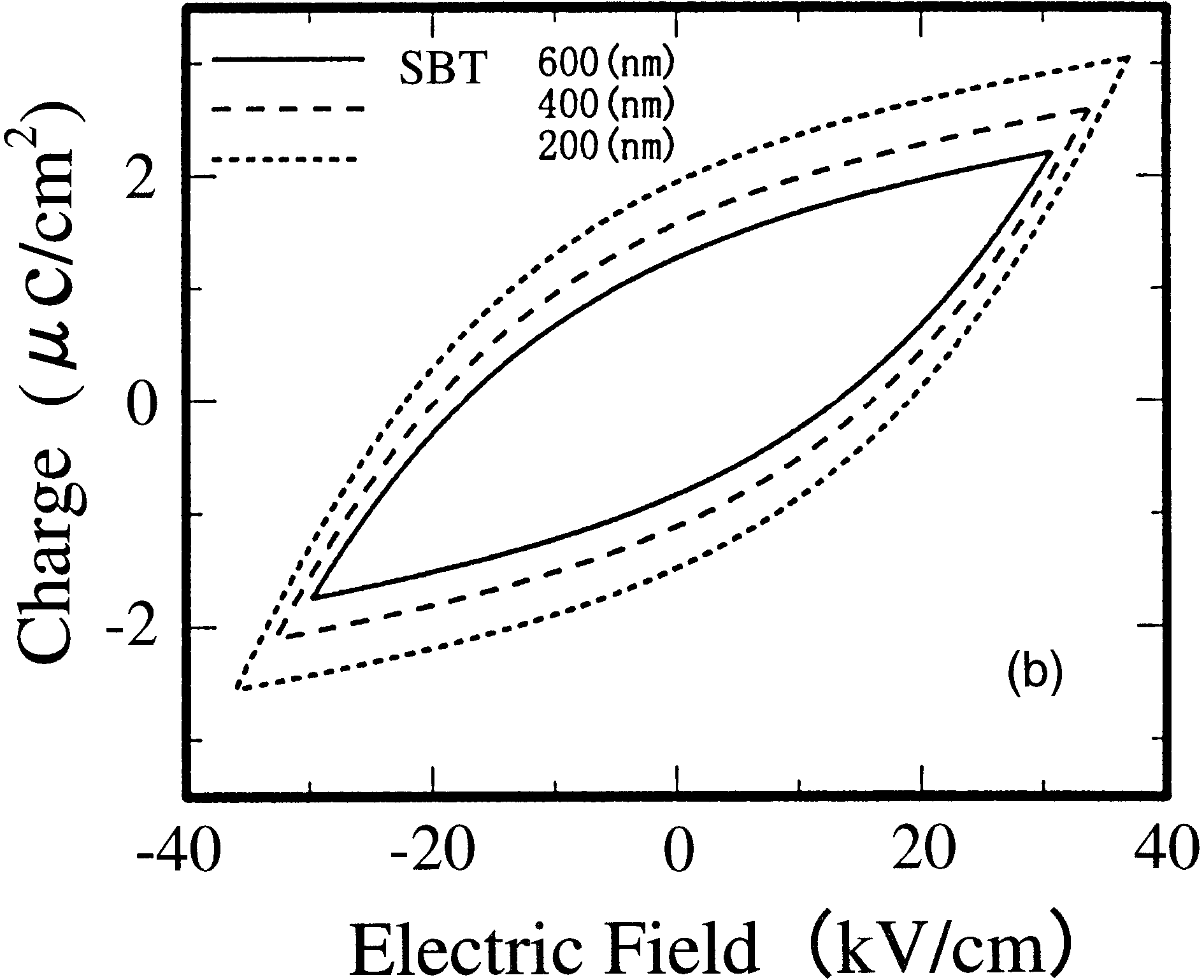
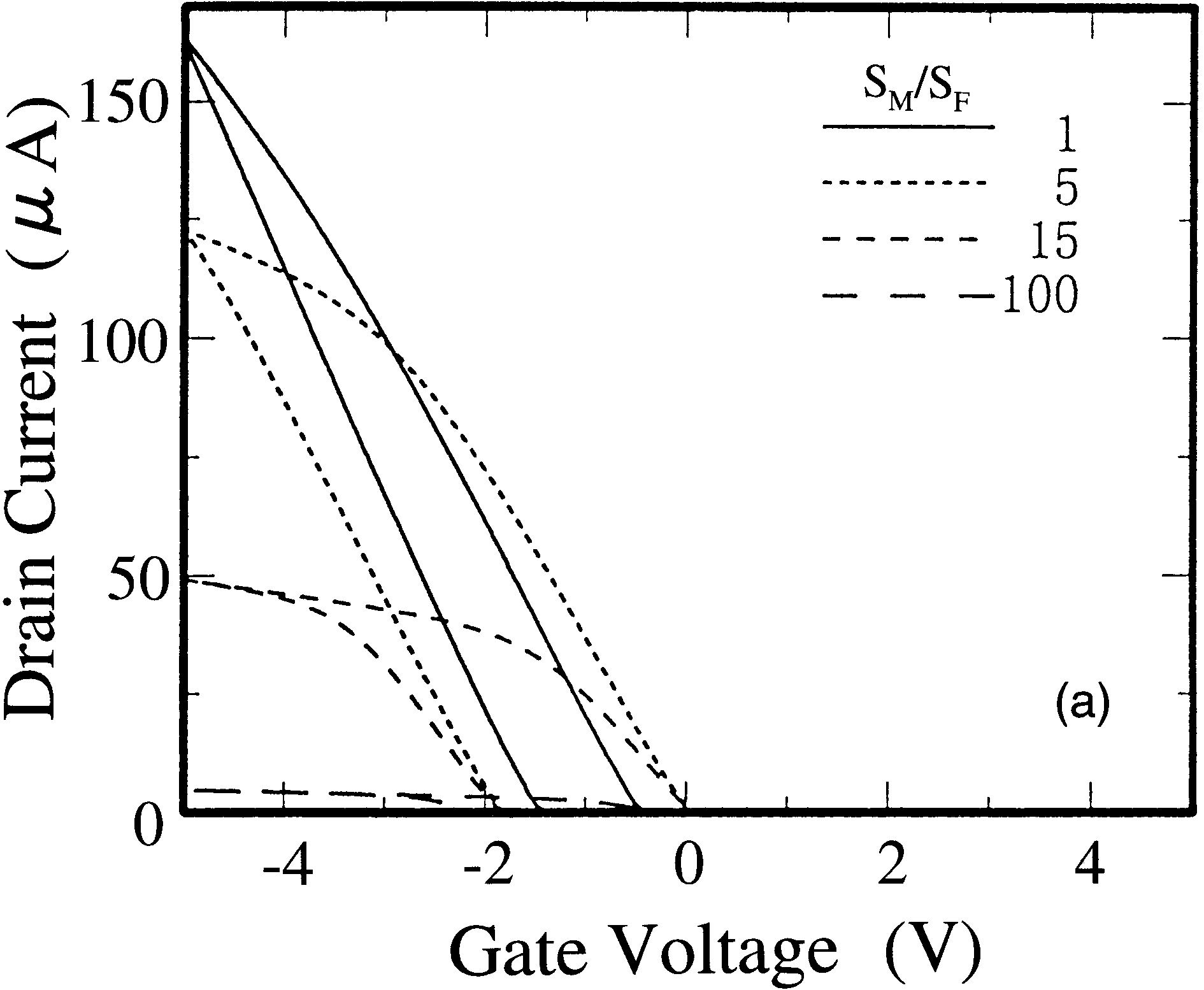


Fig. 4. Calculated (a) *I*D–*V*G characteristics of the MFIS structures with various SBT thicknesses and (b) *P*–*E* hysteresis loops used in the MFIS structures when ±5 V is applied.

to 600 nm, the applied electric filed becomes even smaller, al-though the large memory window can be obtained because of the thick SBT film. This is undesirable for improving the data retention characteristics as shown in the previous section. The reason why only minor loops can be used in the MFIS struc-ture is that the remanent polarization of the SBT film is much larger than the charge required to control the channel conduc-tivity as we pointed out previously.15)The maximum induced charge per unit area by SiO2 is 3.5 *µ*C/cm2, if we assume that the maximum electric field (breakdown field) is 10 MV/cm and the charge which corresponds to the 1 × 1012cm−2elec-trons is 0.16 *µ*C/cm2. On the other hand, the remanent po-larization of SBT films is as large as 10 *µ*C/cm2. Hence, if we select the MFIS structures with SBT films, we cannot use the saturated *P*–*E* hysteresis loop but we can use only a small part of the polarization of the SBT film. This may degrade the data retention characteristics as we experimentally showed in the previous section.

To overcome this difficulty, MFMIS structures should be selected if the SBT film is used. In the MFMIS structure, the area of an MFM ferroelectric capacitor (*S*F) can be de-signed smaller than that of an MIS diode (*S*M). Hence, we can equivalently reduce the polarization of the ferroelectric film. Figures 5(a) and 5(b) show the simulated *I*D–*V*G charac-



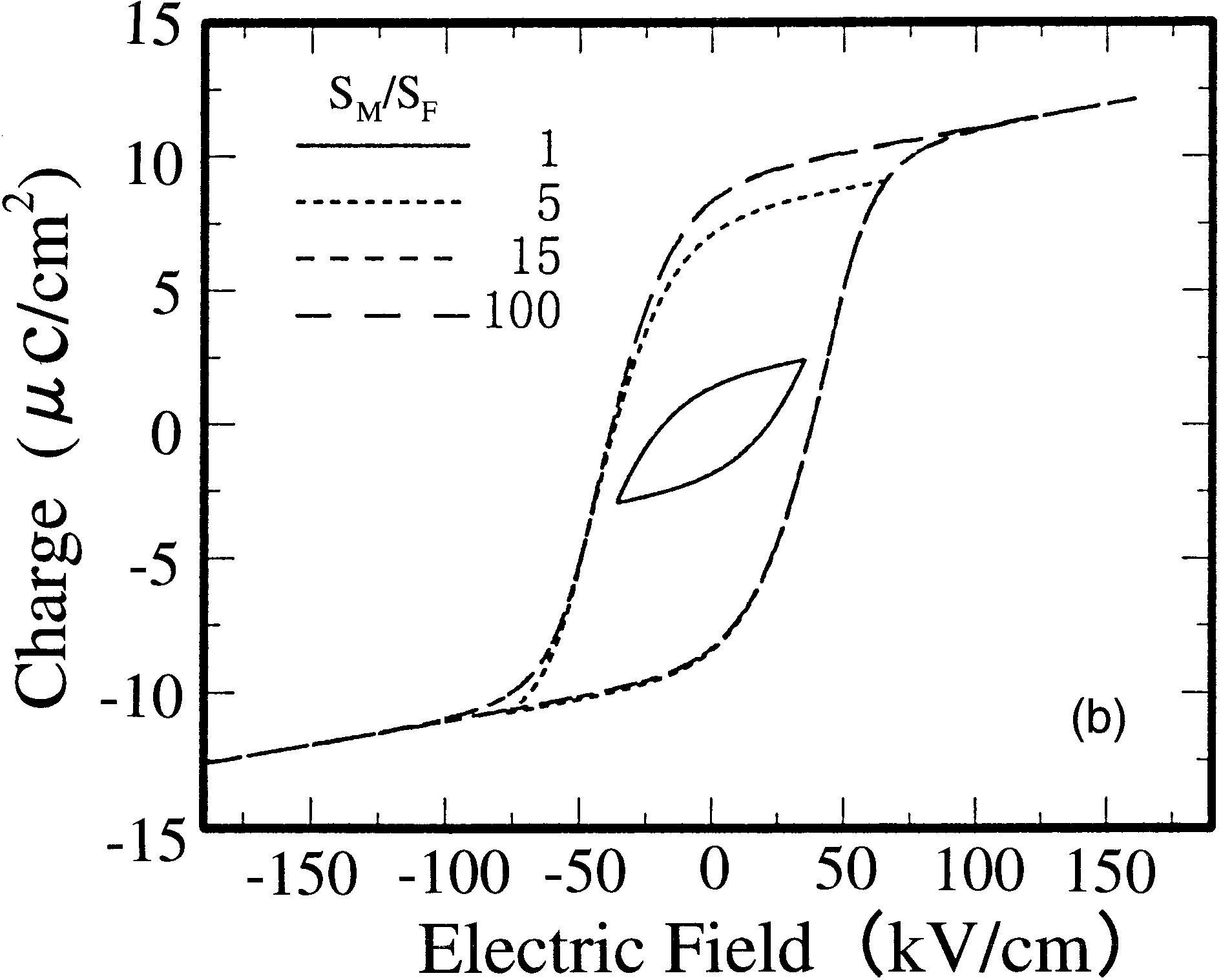


Fig. 5. Calculated (a) *I*D–*V*G characteristics of the MFMIS-FETs and (b) *P*–*E* loops used in the MFMIS-FETs when ±5 V is applied.

teristics of the MFMIS-FETs and the *P*–*E* loops used in the MFMIS-FETs when ±5 V is applied, respectively. The SBT thickness is assumed to be 250 nm. The area ratio, *S*M*/S*F, is varied from 1 to 100. Again, the operation voltage is assumed to be 5 V. It is found that the memory window of the MFMIS structure is as small as 1 V for *S*M*/S*F = 1, whereas the mem-ory window becomes about 2 V for the MFMIS-FETs when the area ratio, *S*M*/S*F is larger than 5. Since the SBT thick-ness is 250 nm and the coercive field is 40 kV/cm, the maxi-mum memory window is 2 V, which agrees with the calcula-tion. It is interesting to note that the used *P*–*E* loops in the MFMIS-FETs are almost saturated when the area ratio *S*M*/S*F is larger than 5. This is consistent with the fact that the mem-ory window is almost constant (2 V) for the MFMIS-FETs with *S*M*/S*F *>* 5. In the MFMIS-FETs with the area ratio *S*M*/S*F of 15, the electric field applied to the SBT layer is as large as 120 kV/cm, which means that completely saturated *P*–*E* hysteresis loops can be used in the MFMIS structure if the area ratio *S*M*/S*F is 15.

According to the above simulations, we fabricated MFMIS-FETs using ferroelectric SBT film and STA/SiON buffer layer, varying the area ratio *S*M*/S*F. The thickness of the SBT film is adjusted from 200–250 nm so that the satu-rated *P*–*E* hysteresis loop can be used with practical *S*M*/S*F

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ratios.

**4.**  **Fabrication and Characterization of Pt/SBT/Pt/STA/**  **SiON/Si MFMIS-FETs**

According to the above discussion, design strategies for ferroelectric-gate FETs using SBT films are (i) MFMIS struc-tures should be selected and (ii) the ferroelectric capacitor area should be designed smaller than the MIS area, so that the saturated *P*–*E* hysteresis loop can be used. Furthermore, to prevent the high operation voltage and reduce the depolar-ization field during the data retention, (iii) the capacitance of the “I” layer should be large enough and (iv) the thickness of the ferroelectric layer should be carefully designed. In addi-tion, (v) it is important that the leakage currents of both ferro-electric and “I” layers are small to improve the data retention characteristics.

To satisfy these conditions, we fabricated p-channel MFMIS-FETs using ferroelectric SBT and STA/SiON insu-lating (“I”) layers. First, field oxide regions were formed in n-(100) Si substrates for device isolation. Then, source and drain regions were formed by BF+ 2ion implantation followed by the activation annealing at 1000◦C for 30 min. Next, after the STA/SiON stacked “I” layer was formed, a Pt floating gate (60 nm) was vacuum-evaporated and pattered by the lift-off process. Then, ferroelectric SBT films were grown by the sol-gel technique on Pt/STA/SiON/Si structures. The thick-ness of the SBT layer used in this work was approximately 250 nm, which is thinner than that (400 nm) in our previous work.8,15)The crystallization of SBT films was carried out by the face-to-face annealing technique at 750◦C.14)Next, Pt gate electrodes were vacuum-evaporated and patterned. Fi-nally, contact holes for source and drain regions were opened by reactive ion etching (RIE) and Al electrodes were formed. The schematic cross section of the fabricated MFMIS-FETs is shown in Fig. 6. Note that in the fabricated MFMIS-FETs, the area of the Pt floating gate is larger than that of the top electrodes. The area ratio *S*M*/S*F was varied from 3 to 15. The channel length and width were 5 *µ*m and 50 *µ*m, respec-tively.

Figure 7 shows experimentally obtained *I*D–*V*G characteris-tics of Pt/SBT/Pt/STA/SiON/Si MFMIS-FETs at a drain volt-age of −0*.*1 V measured with varying the gate voltage sweep 12. Clockwise hysteresis loops due to the ferroelectric nature from ±1*.*5 to ±4*.*0 V. The area ratio *S*M*/S*F of the device is of the SBT films are clearly observed in *I*D–*V*G characteristics as indicated by arrows. The memory window can be obtained even when the applied voltage is ±1*.*5 V. It is interesting to note that the memory window increases with the applied gate voltage and becomes constant when the gate voltage is larger than ±3*.*5 V. This indicates that the saturated *P*–*E* hysteresis

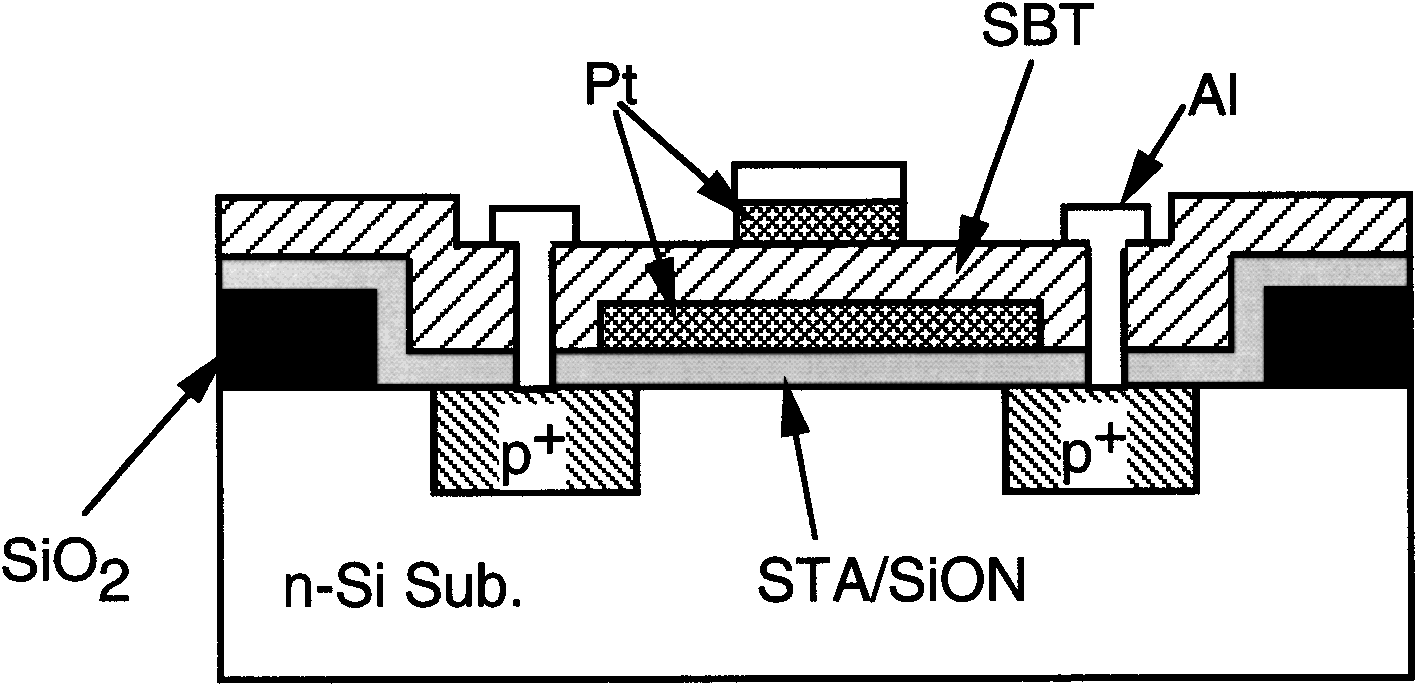


Fig. 6. Schematic cross section of the fabricated MFMIS-FET.

loop of the SBT film is available even when the gate volt-age is as low as ±3*.*5 V, if the area ratio *S*M*/S*F is as large as 12. This is in contrast to our previous work, where about 8 V is necessary to reach the saturation of the memory window. In our previous work, 400 nm SBT films were used in the MFMIS-FETs with an area ratio *S*M*/S*F = 6. Therefore, the reduction of the SBT thickness and large *S*M*/S*F ratios in this work result in the low voltage operation of the MFMIS-FETs. Figure 8 shows how the *I*D–*V*G characteristics of the MFMIS-FETs change with the area ratio *S*M*/S*F. The gate voltage sweep is ±3*.*5 V and the area ratio *S*M*/S*F is varied from 3 to 15. It is found that the memory window is only 0.5 V for the device with *S*M*/S*F = 3, which indicates that only one of the minor *P*–*E* loops is used. On the other hand, when the area ratio *S*M*/S*F is larger than 9, the memory win-dow is almost constant and as large as 1.5 V, which shows the saturated *P*–*E* hysteresis loop is effectively used in the devices with such area ratios. Hence, by increasing the area ratio *S*M*/S*F and reducing the SBT thickness to 250 nm, the MFMIS-FET operating at less than 3.5 V is successfully fab-

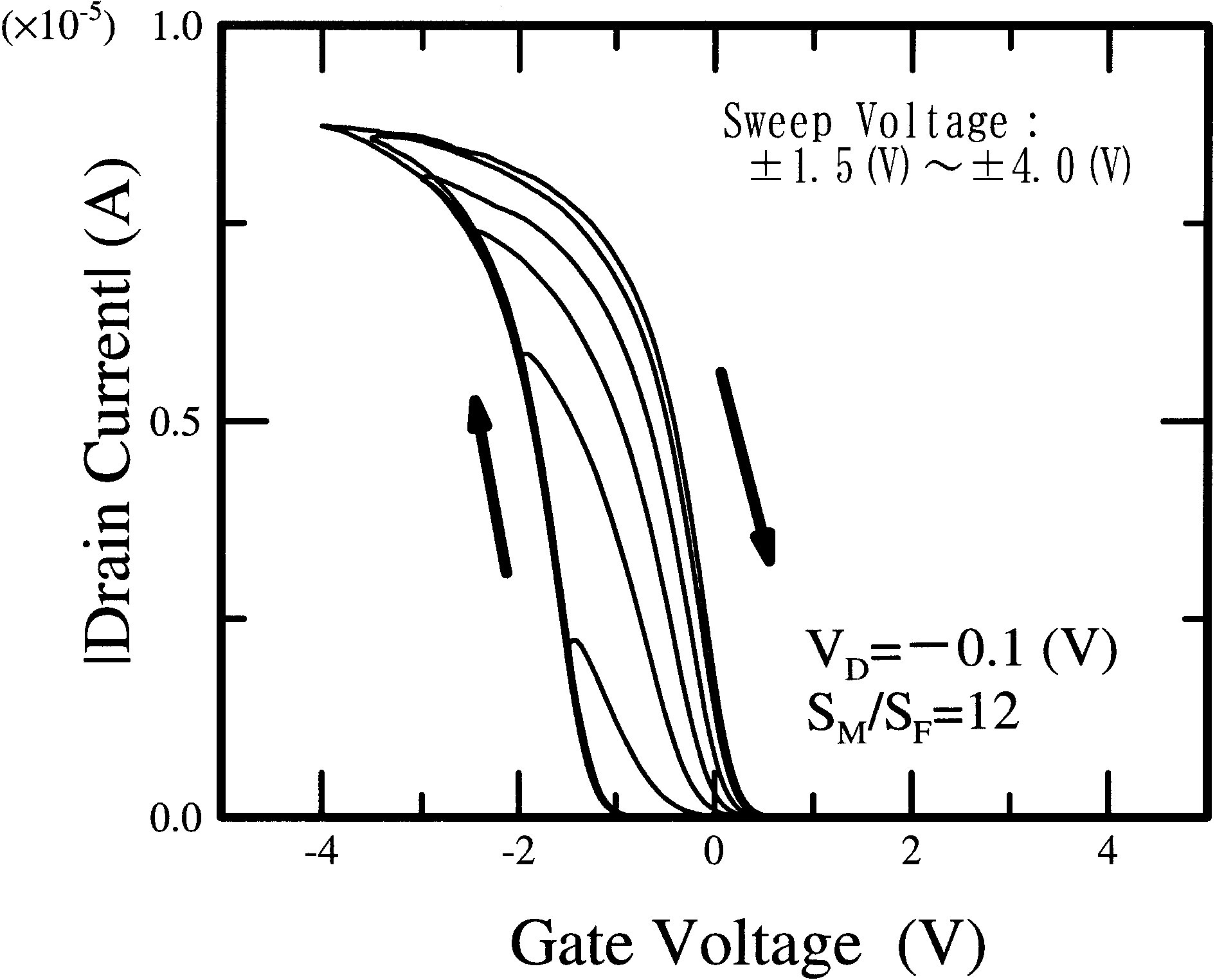


Fig. 7. *I*D–*V*G characteristics of Pt/SBT/Pt/STA/SiON/Si MFMIS-FETs with an area ratio *S*M*/S*F of 12 measured with various gate voltage sweeps at a drain voltage of −0*.*1 V.

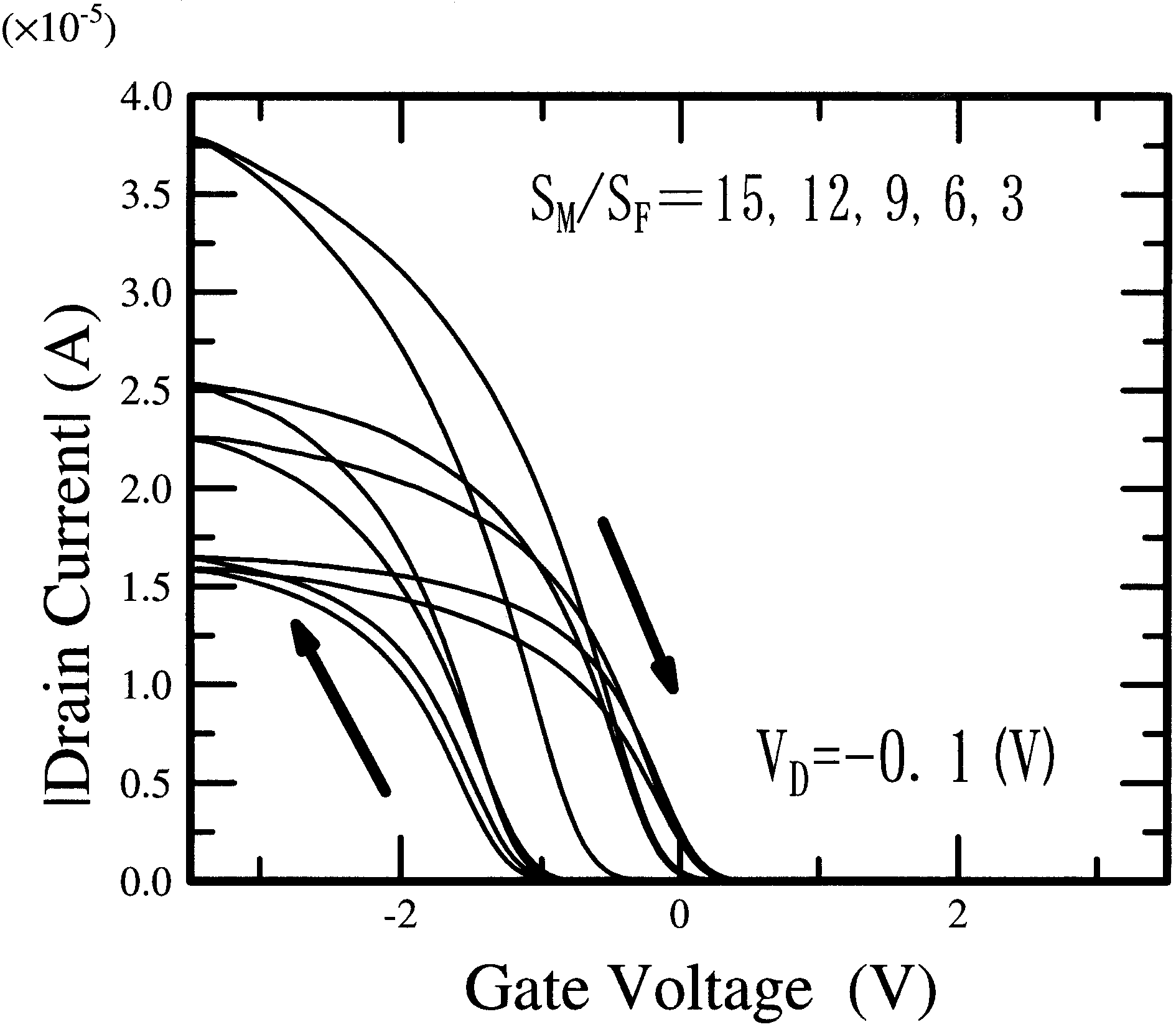


Fig. 8. The area ratio *S*M*/S*F. dependence of *I*D–*V*G characteristics of the MFMIS-FETs.

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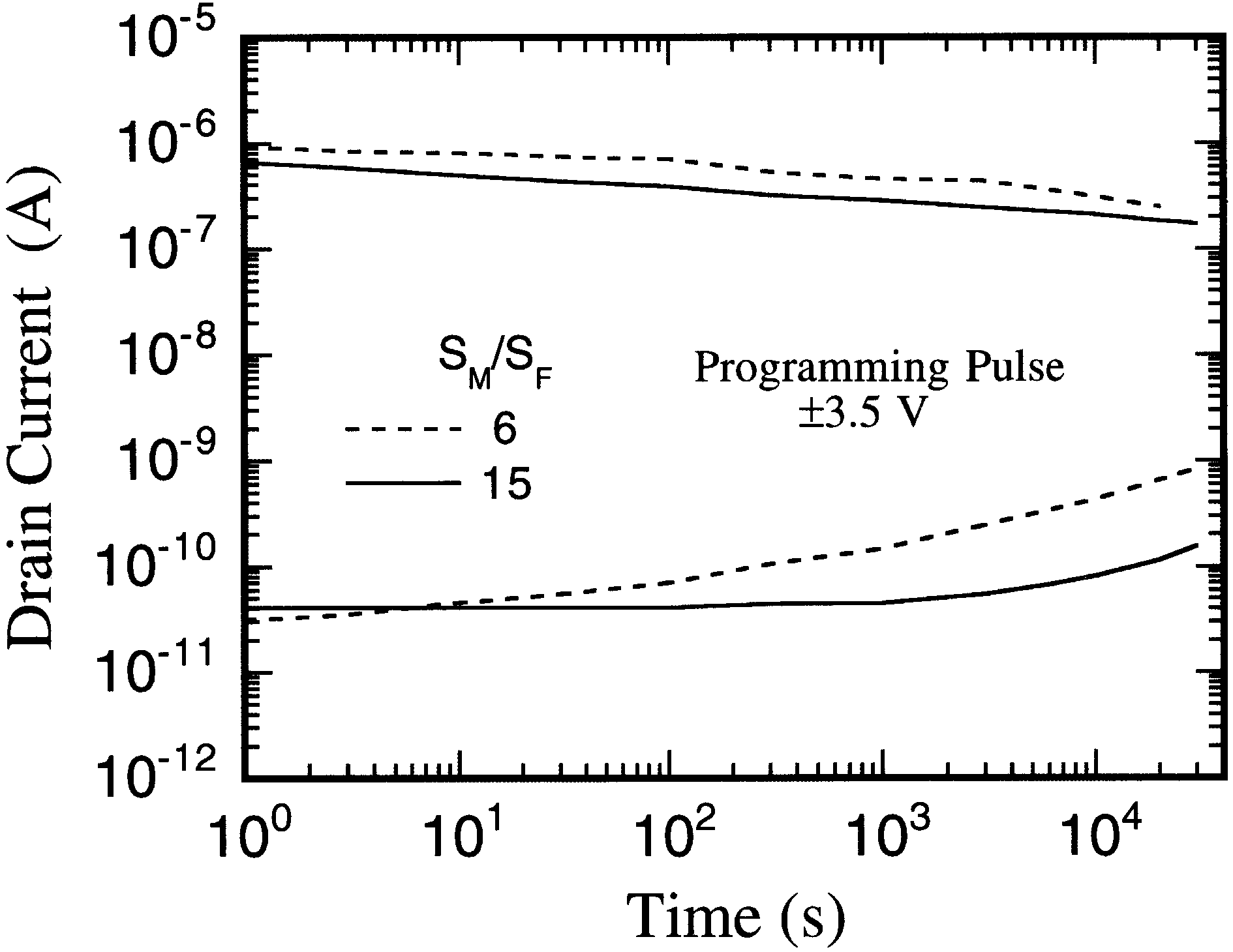


Fig. 9. On and off drain currents of MFMIS-FETs with area ratios *S*M*/S*F of 6 and 15 as a function of the data retention time.

ricated. The gate leakage current is less than 3 × 10−8A/cm2 at a gate voltage of ±3*.*5 V. Next, we examine the data retention characteristics of the fabricated MFMIS-FETs when the small voltage is used to write the data. Figure 9 shows on and off drain currents of MFMIS-FETs with area ratios *S*M*/S*F of 6 and 15 as a func-tion of the data retention time. To measure data retention characteristics, we first applied a ±3*.*5 V programing pulse to write “1” or “0” for 100 ms, then the gate voltage was maintained at −0*.*35 V during a certain retention time, and the drain current was kept measuring at a drain voltage of−0*.*1 V. Hence, the depolarization field is constantly applied to the SBT film during the data retention measurements. It is found that the data retention characteristics can be improved by increasing the area ratio. For the MFMIS-FET with an area ratio *S*M*/S*F of 6, the drain current on/off ratio is initially 3 × 104and is reduced to less than 103after 6000 s (1.7 h). On the other hand, when the area ratio is increased to 15, the drain current on/off ratio is still about 3 orders of magnitude after 10 h have passed, even if the programming pulse is as low as ±3*.*5 V. The electric fields applied to the SBT films when the ±3*.*5 V programming pulse is applied are estimated to be +95 ∼ −70 and +60 ∼ −50 kV/cm for the MFMIS structures with area ratios *S*M*/S*F of 15 and 6, respectively. Hence, by using a large area ratio, a relatively large electric field can be applied to the SBT film in spite of the small oper-ation voltage of ±3*.*5 V, which may result in fairly good data retention characteristics as shown in Fig. 9.

**5.**  **Conclusions**

We have demonstrated that the use of the saturated *P*–*E* hysteresis loop is effective to obtain a long data retention time for MFM-MIS structure diodes. It is shown by the numerical simulation that it is impossible to use the saturated hysteresis

loop of the SBT film in MFIS structures. To utilize the satu-rated *P*–*E* loop, MFMIS structures with a large *S*M*/S*F ratio have to be selected. Then, the MFMIS-FETs using an SBT film and STA/SiON stacked “I” layer have been designed and fabricated. We have demonstrated that fabricated p-channel MFMIS-FETs can operate at a voltage less than 3.5 V. The memory window of 1.5 V was obtained for the device with an area ratio *S*M*/S*F = 15, even if the gate voltage sweep is as small as ±3*.*5 V. It was also found that the fabricated MFMIS-FETs have fairly good data retention characteristics. In conclusion, by increasing the area ratio *S*M*/S*F and reduc-ing the SBT thickness to 250 nm, nonvolatile memory opera-tion of the MFMIS-FETs at as low as ±3*.*5 V is successfully obtained.

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