Vertical Ferroelectric HfO2 FET based on 3-D NAND Architecture: Towards Dense Low-Power Memory

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***Abstract*—** A vertical ferroelectric HfO2 field effect transistor based on 3-D macaroni NAND architecture is reported for the first time. Up to 2 V memory window was obtained after the application of 100 ns program/erase pulses. Flash-like endurance of 104 cycles is reported and first reliability assessments were performed.

the source junction at the substrate and the channel. A HF clean followed by a TMAH etch are then performed to remove the remains of the protective layer. A 20 nm n-type amorphous silicon (4x1019 cm-3) is then deposited as a channel. To crystallize the channel and the FE layer, a 30 min anneal is performed at 900 °C in an ambient mixture of N2 and O2. In the next step, the hole was filled with oxide and then recessed

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| **I.** | **INTRODUCTION** | (hence macaroni structure). Highly doped n-type silicon was |

The memory market is currently in an era of tremendous growth: the big data explosion has yielded the need for more and more data storage. Although 3-D NAND memory is a high density and cost-effective technology, it still suffers from some drawbacks, *i.e.* speed, cell size and power consumption at system level due to required periphery (e.g. charge pumps). Addressing these issues while keeping the advantages of this technology would be very appealing.

Recent years have seen a growing interest in ferroelectric (FE) memory applications. The discovery in 2011 of FE hafnium oxide enabled the emergence of scaled FE devices [1]. Planar HfO2-based FE capacitors and FeFET (Ferroelectric Field Effect Transistor) have received large interest either as a replacement for Dynamic Random-Access Memory (DRAM)

deposited on top of the structure to form the drain and then annealed. Finally, the staircase was formed, followed by metal contacts. A cross-section schematic of the complete test vehicle is shown in Fig. 1b. HR-TEM cross-section of a 100 nm diameter hole can be seen in Fig. 2. A deep recess in the substrate is visible due to the TMAH etch.

In parallel of the macaroni-type FeFET device fabrication, highly-doped full-channel 3-D devices were also made to confirm the presence of ferroelectricity in this configuration and extract FE properties, as previously described [4].

**III.RESULTS AND DISCUSSIONS**

*A.Ferroelectric Capacitor:Material screening*

9.5 nm- and 15 nm-thick Si:HfO2 were deposited in the

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| or for embedded applications [2-3]. A vertical 3-D FE-capacitor | full-channel | configuration | and | characterized | using |

(FeCap) has also been realized using silicon electrodes [4]. Implementation of doped HfO2 - based 3-D FeCaps confirmed the presence of FE properties with 10-year retention [4]. The fabrication of these vertical 3-D FeCaps, using a 3-D NAND architecture, was the first step towards Vertical FeFET (V-FeFET) [5]. Such device could potentially have several benefits over the conventional 3-D NAND memory, such as lower power, periphery reduction, improved endurance and faster operations, while maintaining full CMOS compatibility and

polarization-voltage (P-V) measurements. Cycling dependent P-V and corresponding current-voltage (I-V) characteristics are shown in Fig. 3. Both thicknesses under test exhibited FE behavior accompanied by a slight wake-up. Fig. 4 shows the endurance of these devices up to 105 cycles. An initial increase in remnant polarization was observed which was followed by a stable behavior. No fatigue was observed, as devices were no longer operational after 105 cycles. Both devices have comparable FE characteristics. Due to the presence of several

high-density. etch steps during device fabrication, which could potentially

In this study, a vertical macaroni-type 3-D FeFET with three transistors in series is reported. This is the first demonstration of such device.

**II.DEVICE FABRICATION**

Fig. 1a shows the process sequence for the test device,

damage the FE layer, a 15 nm-thick dielectric was preferred.

*B.V-FeFET:Standard Electrical Characterization*   
 Before investigating V-FeFET memory performance, standard transistor measurements were carried out. A pass voltage of 3 V was applied to both the top and the bottom

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| consisting in a vertical string of three transistors in series with | transistors, | while | the | source | was | grounded. | Output |

a channel length (Lch) of 50 nm. The fabrication steps until FE deposition are same as previous work [4]. Here, silicon was used as dopant in HfO2 to form the FE material, deposited by atomic layer deposition (ALD). A thin a-Si layer was then deposited as gate stack protection from the subsequent etching of the bottom of the hole, required to allow the contact between

characteristics (ID-VD) were recorded (Fig. 5) for a hole diameter of 70 nm. Typically for scaled MOSFET devices, an increase in current was observed at large drain and gate voltages. The ID-VG characteristics are shown in Fig. 6 for multiple devices with 70 nm hole diameter. The gate had negligible leakage current, as shown in the inset. An ON-

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current of ~1 �A was achieved, while maintaining an OFF-current of a few pA, giving an excellent ON/OFF ratio of ~6 decades. The statistical distributions of the threshold voltage (VT), extracted using a constant current (CC) criterion (10 nA), the ON-current ION, taken at VT + 2 V and the subthreshold swing STS are shown in Fig. 7 for various hole diameters. VT and STS distributions were broad, which suggested the presence of a defect-rich HfO2 / Poly-Si interface.

*C.V-FeFET:Memory Characterization*

As charge trapping at the interface can effect proper cell read-out, DC and pulsed ID-VG measurement methodologies were benchmarked. This first technique is relatively slow, as each measurement at a given voltage requires milliseconds. In the presence of traps, this can lead to a degradation of the characteristics and to a smaller FE memory window (MW). Pulsed I-V measurements, which are in the order of microseconds at every voltage, can reduce charge trapping. FE MW is shown here for a vertical macaroni-type FET with a hole diameter of 70 nm, a pass voltage of 3 V and ± 10 V program/erase (PRG/ERS) pulse with a width of 100 ns (Fig. 8). A MW of ~2 V was obtained with pulsed I-V. This was further utilized as the preferred method to characterize memory devices, as DC I-V resulted in an ID-VG degradation (charge trapping) as well as a smaller MW: MW pulsed ~2 V vs MW DC ~0.5 V.

To investigate the optimal operation conditions for the device, ISPP and ISPE on a 70 nm-diameter device were performed and are shown in Fig. 9 and 10, respectively. A ± 10 V with 100 ns pulse length was used to program and erase before the measurements. The ISPP showed a gradual increase in the MW with pulse amplitude, while ISPE yielded a more sudden step. This could be due to the presence of a small number of domains because of the small size of the device. The gradual programming could be the result of some trapping interferences and/or different domain growth kinetics. At larger pulse widths and high voltages, charge trapping starts to

use single-pulse technique [7]. The shift between the rising and falling edges of the pulse (�VT21 = VT2-VT1) is proportional to the number of trapped charges, here electrons (Fig. 13 inset). The trapping process was studied on a transistor in PRG state by changing the pulse width and amplitude. A positive �VT21 shift in ID-VG confirmed the occurrence of electron trapping (Fig. 13a) which increased with both pulse width and amplitude, as shown in Fig. 13b.

Retention measurements were also carried out. Short-term retention at 25 °C (related to FE relaxation) showed a stronger degradation of the PRG state compared to the ERS state (Fig. 14) nicely correlating to the broader VT distributions of the PRG state compared to the ERS equivalent. The latter one stays relatively steady, with degradation occurring at higher voltages. The same remark held true for the PRG state but with a more intense degradation as a possible result of charge trapping and depolarization. Longer retention tests at 85 °C confirmed a larger degradation of the PRG pulse (Fig. 15). A clear separation of states was observed after 100h at 85 °C.

*E.Path for improvements*

The presence of high-k dielectric as the gate oxide results in charge trapping phenomenon, countering the ferroelectric behavior. This is a known issue for HfO2 FeFET [6], which needs to be addressed through process integration optimization. A thick oxide, without special treatment or film improvement, was used, leading to large PRG/ERS voltages. This could be seen as too high for FE, however this corresponds to an electric field of ~ 6.5 MV/cm and is in agreement with the P-V loop shown in Fig. 3. A thinner gate oxide would reduce the operation voltage and additionally improve the reliability, *i.e.* reduce trapping and enhance endurance. Detailed reliability studies are required for better understanding of the device behavior, *i.e.* impact of pass voltages. The potential of 3-D FeFET and its advantages compared to the prior state-of-the-art are presented in Table 1. This technology offers low power high-density memory that decreases the speed gap between the

dominate FE. central processing unit (CPU) and storage.

The evolution of VT with cycling is shown in Fig. 11. Closure of the MW was observed at 104 cycles. A slight wake up period of around 10 cycles was initially observed. This was followed by a decrease in the MW. While the ERS state decreased slightly with cycling, the PRG state was much more impacted by the endurance possibly due to trapping [6]. Fig. 12 shows the PRG and ERS density distributions after 10 cycles. The device-to-device variability may be caused by differences in defect distribution and charge injection as well as variable FE properties, that can be affected by a combination of factors such as film uniformity and mechanical stress. The

**IV.CONCLUSIONS**

A functional vertical macaroni-type 3-D FeFET with three gates was fabricated and characterized for the first time. Memory window up to 2 V was obtained with pulse width of 100 ns. Endurance of 104 cycles and reliability assessments are also reported. A decrease of the FE layer thickness could potentially decrease the operation voltage and increase the endurance and lifetime of these devices. This study paves the way for a high-density high-speed non-volatile memory that reduces the gap between CPU and storage.

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| ERS state was narrower than the PRG, confirming that one state was more stable than the other. Further integration | REFERENCES |

improvements are required to enhance MW characteristics.

*D.V-FeFET: Reliability Consideration*

High fields over the interface can generate defects and can also cause injection of charges into defects, resulting in charge trapping which causes a reliability issue for FeFET devices. A way to study the trapping mechanisms in high-k material is to

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|  | **Source implantation** | | | | | | |  | | | | | | | | | | | | | | | | | | | |  | | | | |
| **Gates deposition** | | | | | | |
| **Vertical memory hole etch** | | | | | | |
| **Fe-HfO2 and a-Si deposition** | | | | | | |
| **Bottom hole opening** | | | | | | |
| **and TMAH** | | | | | | |
| **a-Si channel deposition** | | | | | | |
| **Drain implantation** | | | | | | |
| **Thermal anneal** | | | | | | |
| **Staircase and metal** | | | | | | |
| **contacts formation** | | | | | | |
| **(a)** | | | | | | |
| Figure 1. (a) Process Flow description. (b) Schematic cross-section of the macaroni-type 3-D | | | | | | | | | | | | | | | | | | | | | | | | | | | Figure 2. | | | TEM | | cross- |
| FeFET with three cells in series. | | | | | | | | | | | | | | section (Ø: 100nm) | | | | | | | | | | | | | | | | | | |
| **2) Polarization (**μ**C/cm** | **60**  **40**  **20**  **0** **-20-40-60** | Si:HfO2 : 9.5 nm | | | | | | | | Si:HfO2 : 15 nm | | **4 6** | **8** | **2)- (**μ**C/cm + / Pr Pr** | **25**  **20**  **15**  **10**  **5**  **0** **-5** **-10-15-20** | | |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | |  |  |  |  |  |  |  | |  |  |  |  |  |  |  | | | | | | | |  |  |  |  |  |  |  |  |  |
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| Static | | | | |  |  |
| **-6**  **10** | | Pulsed | | |
| **ID (A)** | **-7**  **10** | | | |
| **PRG** | | **ERS** | | |
| **-8**  **10** | | **MW ~ 2V** | | |
| **-2** | | **-1** | **0** | **1** |
| **VG (V)** | | | | |
| Figure 8. Comparison between DC | | | | | Figure 9. ISPP after -10 V/100 ns erase | Figure 10. ISPE after +10 V/100 ns |
| pulse. A gradual increase is observed | program pulse. The MW increase is |
| ID-VG and Pulsed ID-VG after PRG and | | | | |
| ERS (±10 V – 100 ns). A MW of ~2 V | | | | | with pulse amplitude. Blue: no MW, | more sudden. Blue: no MW, Yellow: |
| Yellow: Max MW | Max MW |
| was measured | | | | |

**0.5**

**0.0**

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| **VT (V)** | **-0.5** | **PRG** |
| **ERS** |

**-1.0**

**-1.5**

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| **0**  **10** | **1 10** | **2 10** | **3 10** | **4**  **10** |

**Cycles**

Figure 11. VT evolution with   
cycling after PRG and ERS. A

larger degradation of PRG is

observed.

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| **VT\_PRG(0) - VT\_PRG(V)** | **0.3** | ***Temp : 25*** °***C*** | | **8V Pulse** | | Figure 12. VT after 10 cycles (±10 V | | | | | | | | Figure 13. (a) Single pulse ID-VG (obtained from |
| **0.2** |
| – 100 ns). ERS distribution is | | | | | | | | rising/falling edge) after PRG for incrementing |
| **10V Pulse** | |
| **0.1** |
| narrower than PRG distribution. | | | | | | | | pulse width tTP, (b) �VT21 vs tTP (�VT extracted |
| **0.0** |
| **-0.1** | (Ø: 70 nm) | | | | | | | | at ID = 4x107 A, pulse width: 100 �s to 10 ms, |
| **-0.2** |
| pulse amplitude: 2 V to 3 V) |
| **-0.3** |
| **VT (V)** | **0.2** | |  |  |  |  |  | | --- | --- | --- | --- | --- | |  |  |  |  |  | | | | | | |
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