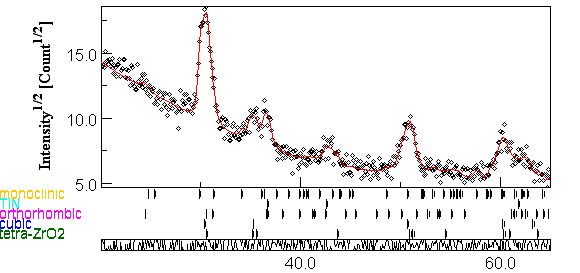
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2019.2902953, IEEE Journal of the Electron Devices Society

On the characterization and separation of trapping and ferroelectric behavior in HfZrO FET   
Md Nur K. Alam\*,1,2, B. Kaczer1, L.-Å. Ragnarsson1, M. I. Popovici1, G. Rzepa3, N. Horiguchi1, M. Heyns1,2, and J.

Van Houdt1,4

1IMEC, Leuven 3001, Belgium; 2Department of Materials Engineering, KU Leuven; 3TU Vienna; 4ESAT, KU Leuven; \*Email: md.nur.kutubul.alam@imec.be

***Abstract:*** *N-channel FETs with ferroelectric (FE) HfZrO gate oxide are fabricated, showing steep subthreshold slope under*

*certain conditions. Possible origins of ID-VG hysteresis, the*

*hysteresis vs. subthreshold slope tradeoff, dependence on the*

*bias voltage and temperature and the competition between*

*trapping and FE behavior are reported and discussed. A band*

*of active traps in the ferroelectric layer responsible for charge*

*trapping during device operation is characterized. Transient*

*ID-VG measurements are introduced to facilitate differentiating*

*between trapping and FE behavior during subthreshold slope*

*measurements.*

**I.**  **Introduction**

The transfer characteristic of MOSFETs has a fundamental thermodynamic limit in its steepness known as “Boltzmann tyranny” that restricts the minimum possible subthreshold slope to ~60 mV/dec at room temperature. In recent years, ferroelectric (FE) FETs have been experimentally demonstrated to break this limit [1] [2] [3] [4] [5] [6] [7] [8]. Despite such successful demonstrations, some critical challenges need to be addressed for the FEFET to be of use to the industry. Firstly, a FE material is needed to be compatible with the existing CMOS processing technology, i.e., deposited by ALD. In addition, as FE films are known to lose its ferroelectric properties below certain critical thickness, the material to be used must possess its ferroelectricity at a thickness that would allow metal gate and gate dielectric (DE) to fit in the fin-to-fin space and gate trench. Previously, doped HfO2 has been demonstrated to meet these criteria. However, in doped HfO2, the required mole fraction for Si, Al, Y, Gd, La and Sr as a dopant are less than 15% to get the FE phase [9]. Such dopants can be used in the thick FE oxide-based devices but may become impractical in ultra-scaled ones.

In this work we therefore use planar n-channel FEFET fabricated by gate-last process with Hf0.5Zr0.5O2 FE gate oxide as it is more scalable. Even though the gate stack is not optimized for steep slope operation [10], the devices show < 60 mV/dec threshold under certain measurement conditions. We discuss possible mechanisms contributing to the device hysteresis, the hysteresis vs. subthreshold slope tradeoff and we report the effect of oxide thickness, lateral scaling, anneal and measurement temperatures, and bias voltage on trapping and polarization behavior [11].

Charge trapping in the gate oxide of FET originates from oxide defects and leads to various degradation effects, such as bias temperature instability (BTI) [12]. These defects can be located at any spatial position within the oxide as well as can have different ionization energies. In this extended work [11] we extract the defect energy band active in our Hf0.5Zr0.5O2 n-channel FEFET from Non-radiative Multi-Phonon (NMP)

theory using BTI-like methodology [13] below the device ferroelectric coercive voltage. Finally, we propose a simple method to separate the trapping and ferroelectric behavior in the FEFET during *ID*-*VG* characterization using transient-current measurements.

|  |  |  |  |
| --- | --- | --- | --- |
| **II.** | **Experimental** | and | electrical |
| The following device fabrication  characterization were employed in this work. | |

*i) Device fabrication*

We used gate-last process for fabricating planar FEFETs. The high-k oxide of 3nm, 5nm and 8nm thickness has been deposited using ALD, followed by the deposition of 10nm TiN on top of the oxide as gate metal. Finally, to crystallize the oxide, post-metallization-annealing was done at 5000C, 5500C and 6000C. The interfacial SiO2 layer has a thickness of 0.8nm. Fabricated devices have the dimensions (width × gate length) of 10m×10m, 1m×1m and 1m×70nm. The GIXRD data shown in Fig. 1 confirm that we have properly crystallized oxide. In the 8nm HfZrO,we have ~40% of the oxide crystallized as orthorhombic phase (the rest are a mixture of other, non-polar phases), needed to induce FE behavior. Al doped HfO2 based FET was fabricated in which the oxide did not show ferroelectric behavior. To compare the performance of FEFETs, we also fabricated other dielectric (DE) FETs of the same device dimensions with HfO2 and SiO2 as gate oxide. Neither of the reference HfO2 stacks received a high-temperature anneal.

|  |  |  |
| --- | --- | --- |
| Intensity1/2 (Count1/2) | 40 | 60 |
| 2 (Degrees) |

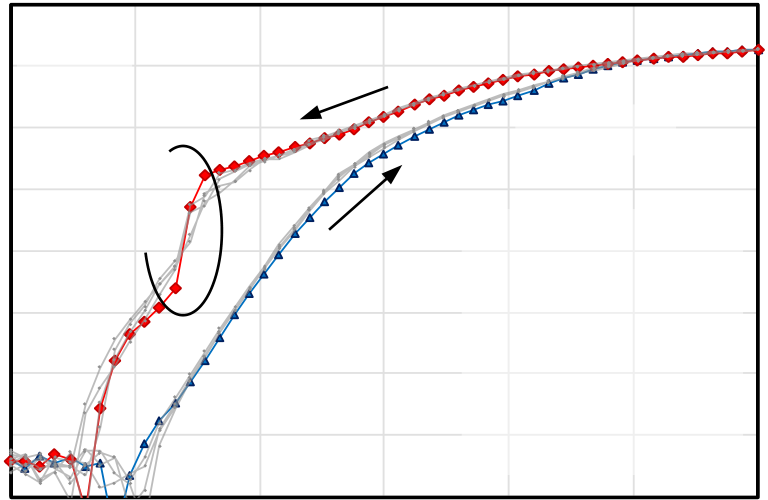
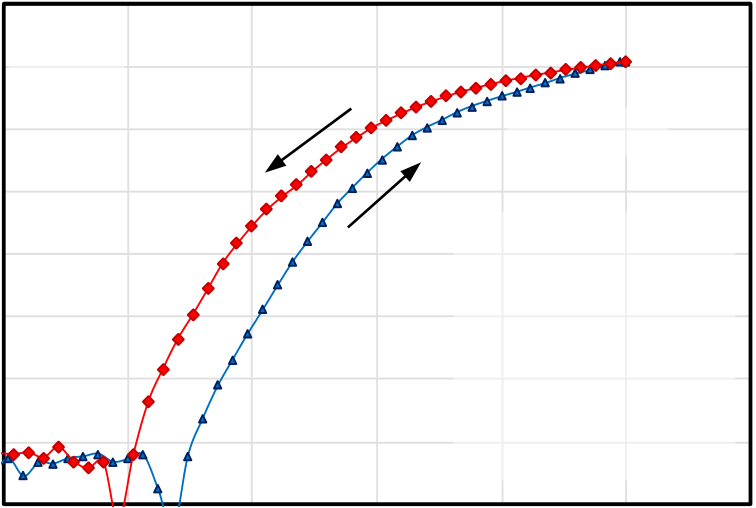
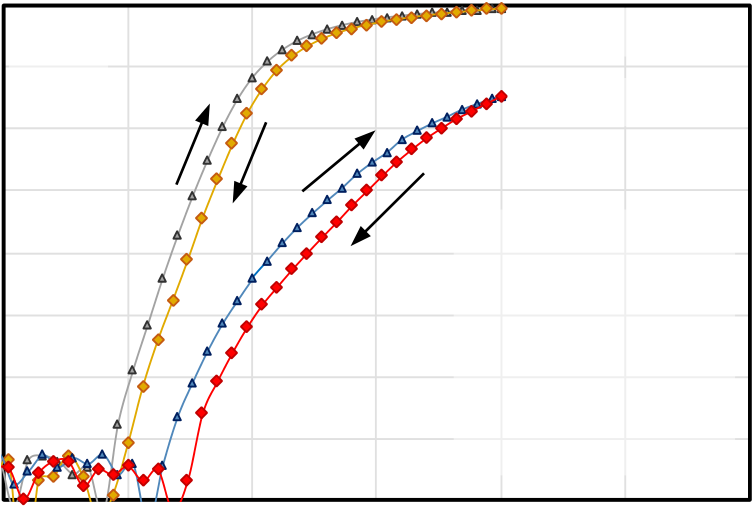
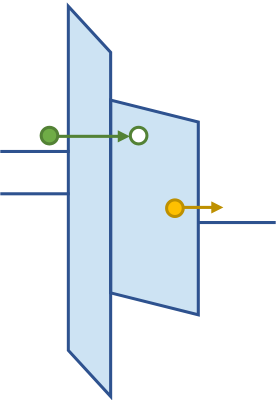
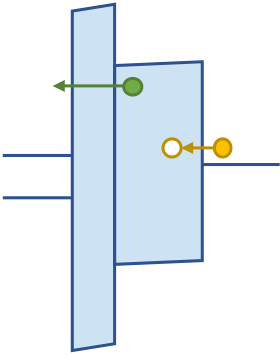
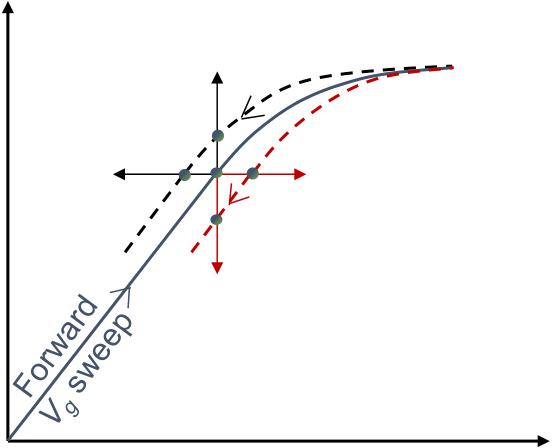
Fig 1: GIXRD spectrum showing crystalline phase of 8nm Hf0.5Zr0.5O2 annealed at 550oC.

*ii) Electrical characterization*

We performed basic FEFET characterization by measuring the *ID-VG* transfer characteristics in the linear regime (drain bias *VD* = 50 mV), sweeping gate bias *VG* from either 0 to *Vm* or -*Vm* to *Vm* and back. Different values of *Vm* have been used

This paper is based on a paper entitled “Investigation of ferroelectric HfZrO FET for steep slope applications,” presented at the 2018 IEEE S3S Conference

2168-6734 (c) 2018 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications\_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2019.2902953, IEEE Journal of the Electron Devices Society

**(a)** During **forward** *VG* sweep **(b)** During **reverse** *VG* sweep (high *VG*) ( low *VG*)

CS e- CS e-

trapping de-trapping GS e-*Vth* > 0 V GS e- trapping de-trapping  
 *Vth* < 0 V   
 TiN Si

high-k   
DE or FE

Interfacial   
SiO2

|  |  |  |
| --- | --- | --- |
| **(c)** | *ID* | GS e-de-trapping CS e-de-trapping |

*Vth* < 0 V

*Vth* > 0 V

|  |  |
| --- | --- |
| • | therefore convoluted or confused with FE polarization switching [19] [20]. When the *Eox* field is removed (during reverse sweep), the trapped charge can get de-trapped (Fig. 2b) [20]. Apart from charge trapping, *Vth*shift may also arise from ionic motion inside the oxide [21]. This latter mechanism is not considered in this study. |

The directions of hysteresis and the impact on the full n-channel FEFET double-sweep *ID*-*VG* characteristic are summarized in Fig. 2c.

**Results and discussion**

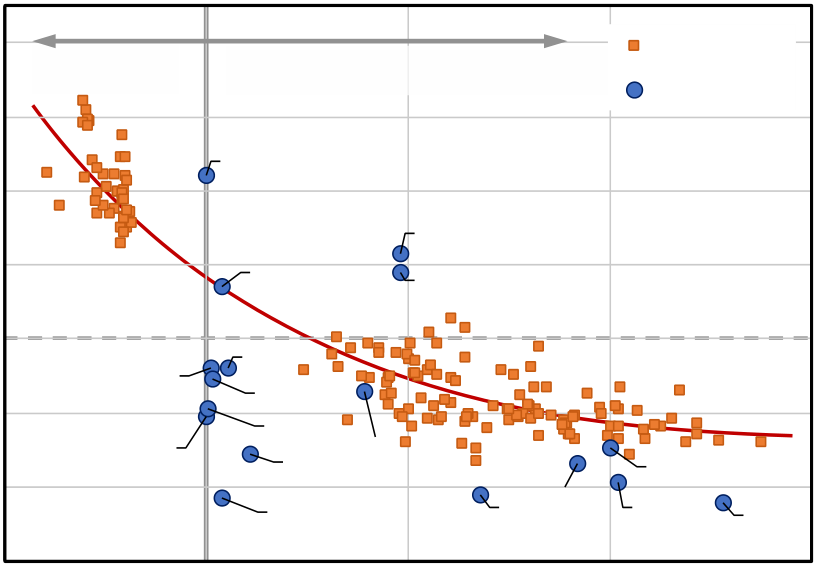
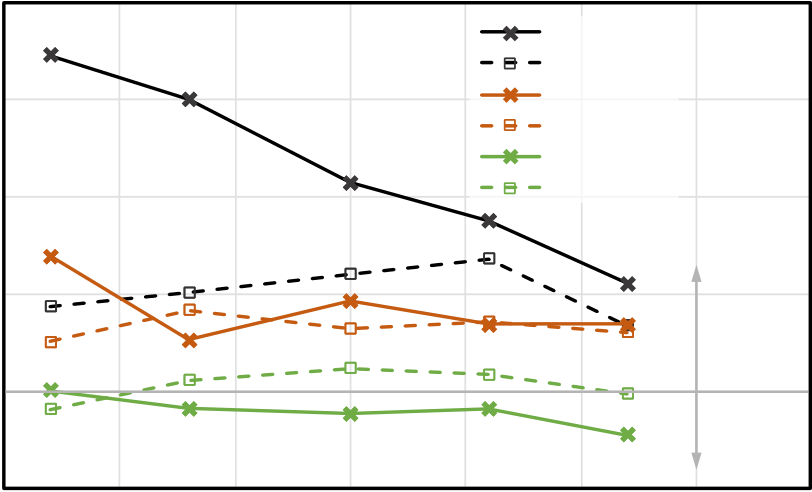
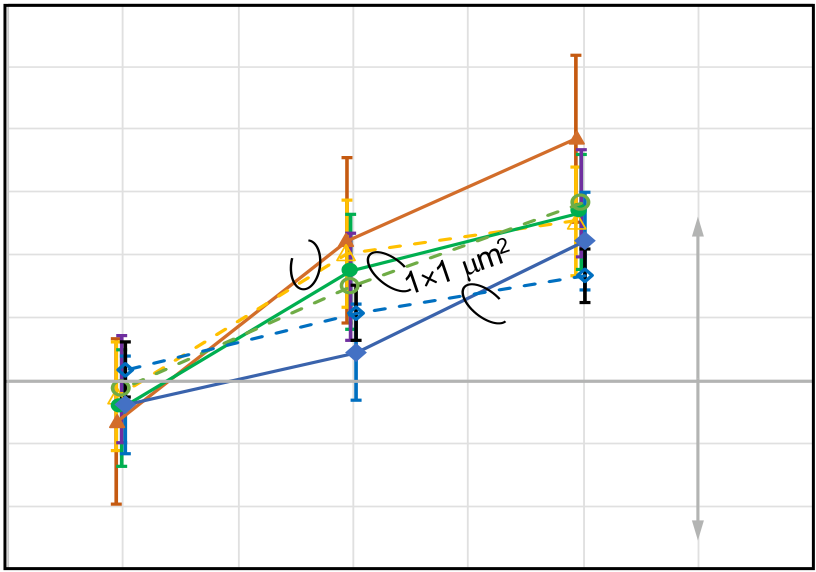
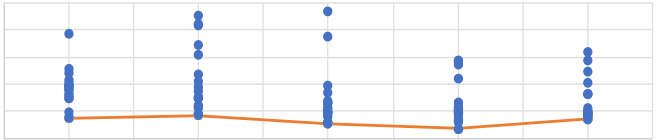
In this section we show the results obtained from the measurements and discuss the physical origin of the observations. The section is divided into three subsections: basic device operation, extraction of the oxide defect bands, and the transient *ID*-*VG* technique.

|  |  |  |  |
| --- | --- | --- | --- |
| CS e-trapping  GS e-trapping  FE depolarization | *A) Basic device operation* | | **DEFET** |
| Fig 2: Direction of threshold voltage shift Δ*Vth* caused by channel side (CS) and gate side (GS) trapping, detrapping and FE depolarization. At constant *VG*, the effects result in change of drain current with time. | 1.00E-05 10-5  1.00E-06 | **(a)** |
| 1.00E-07 10-7 | | **FEFET** |

1.00E-08

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| for the double sweep. For the extraction of defect energy band we used the extended Measurement-Stress-Measurement (MSM) sequence [14]. Finally, as will be discussed in detail below, we have designed a multiple-sweep *transientID-VG* measurement, in which the drain current *ID* is measured as a function of time after every *VG* step. Analysis of the *ID* transients facilitates separating trapping and ferroelectric behavior. | | ***ID* (A)** | 1.00E-09 10-9 | | ***Vm* = 2.0 V** | | | | | | | | |
| *L* = 1 m | | | | | | | | |
| 1.00E-10 | | | *W* = 1 m | | | | | | | | |
| 1.00E-11 10-11 | | | *VD* = 50 mV  *VG / step* = 60 mV | | | | | | | | |
| 1.00E-12 | | | *t / step* = 0.45 s | | | | | | | | |
| 1.00E-13 10-13 | | 0 | 0.5 | | 1 | 1.5 | | | 2 | 2.5 | 3 |
| 1.00E-05 10-5 | |
| 1.00E-06 | | | **(b)** | | | | | | | | |
| **III.** | **Origins of FEFET hysteresis** | 1.00E-07 10-7 | | | **FEFET** | | | | | | | | |
| Several phenomena are known to cause and impact the FEFET transfer characteristics, particularly its hysteresis and the corresponding threshold voltage shift Δ*Vth*. | | 1.00E-08 | | | | | | | | | | | |
| ***ID* (A)** | 1.00E-09 10-9 | | ***Vm* = 2.5 V** | | | | | | | | |
| *L* = 1 m | | | | | | | | |
| 1.00E-10 | | | *W* = 1 m | | | | | | | | |
| • | In response to the oxide electric field *Eox* generated by the application of *VG*, FE dipoles are reoriented along the direction of the field, or in other words, polarize the oxide. When the *Eox* field is removed, the FE experiences a depolarization field as it is connected in series with another capacitor that arises from the Si channel [15] [16] [17]. In addition, presence of non-polar phase in the FE oxide creates the same effect [16]. | 10-11 | | | *VD* = 50 mV  *VG / step* = 60 mV | | | | | | | | |
| 1.00E-12 | | | *t / step* = 0.45 s | | | | | | | | |
| 10-13 | | 0 | **(c)** | 0.5 | 1 | 1.5 | | | 2 | 2.5 | 3 |
| 1.00E-05 10-5 | |
| 1.00E-06 | |
| 1.00E-07 10-7 | | | **FEFET** | | | | | | | | |
| ***ID* (A)** | 1.00E-08 | | Sub 60  mV/dec | | | | ***Vm* = 3.0 V** | | | | |
| 1.00E-09 10-9 | |
| *L* = 1 m | | | | |
| • | In addition to FE polarization, gate-oxide *charging* will typically take place during FEFET operation due to charge carriers tunneling into and out of the insulator preexisting oxide defect centers [18]. Charge trapping/detrapping at the channel side (CS) will generally result in Δ*Vth* with the opposite sign from FE polarization (Fig. 2a) as electrons are trapped during the forward *VG* sweep. On the other hand, detrapping of electrons at the gate side (GS) will result in the same sense of hysteresis as FE polarization and may be |
| 1.00E-10 | | | *W* = 1 m | | | | | | | | |
| 10-11 | | | *VD* = 50 mV  *VG / step* = 60 mV | | | | | | | | |
| 1.00E-12 | | | *t / step* = 0.45 s | | | | | | | | |
| 10-13   0.0 | | | 0.5 | | 1.0 | 1.5 | | 2.0 | | 2.5 | 3.0 |
| ***VG* (V)**  Fig 3: Transfer characteristics of a HfZrO (8 nm) FEFET showing the effect of the maximum sweep value *Vm*. (a) At low *Vm*, hysteresis is likely due to CS trapping; (b) at higher *Vm*, hysteresis from polarization switching dominates; (c) at even higher *Vm*, the same hysteresis sense *with steep subthreshold slope* | | | | | | | | | | | |

2168-6734 (c) 2018 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications\_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2019.2902953, IEEE Journal of the Electron Devices Society

is observed. Stress-Induced Leakage Current (SILC) and significant degradation of the gate oxide is observed at even higher values of *Vm* (not shown). The results are repeatable shown by light gray lines. (a) A non-ferroelectric HfO2 (5nm) DEFET characteristic is shown for comparison.

We start with a fresh ferroelectric FET device, the oxide of which is not woken up by any electric field cycling. Double-sweep *ID-VG* transfer characteristics of this FEFET from 0V to *Vm* = 2.0, 2.5, and 3.0 V are shown in Fig. 3. Hysteresis in the transfer characteristics is clockwise for *Vm* = 2V, which is typical for CS trapping behavior (cf. Fig. 2). When compared against the non-ferroelectric DEFET, the ferroelectric device shows a larger threshold voltage and a poorer SS. As *Vm* is increased, the hysteresis changes direction. This is typically explained as a wakeup (or polarization) of the FE oxide followed by polarization switching. Once the polarization switching dominates, sub 60mV/dec slope is observed but only in the reverse trace of the *VG* sweep. The results are reproducible in repeated measurements.

Since during the forward sweep the FE oxide becomes polarized, it should result in principle in sub 60mV/dec slope as well. We assume that progressive trapping of channel electrons during forward sweep causes a positive shift in *Vth*, which in turn results in poor SS [22]. During the reverse sweep, the depolarization field increases with decreasing *VG*. In addition to that, CS electron de-trapping from oxide defect states takes place in the reverse trace. As a consequence, the steep SS in the reverse trace is observed.

Figure 4 shows the subthreshold slope (SS) obtained in the reverse *VG* trace for different oxide thicknesses, anneal temperatures of the oxide, and for different values of *Vm*. It is clearly noticed that as the *Vm* value increases, the minimum value of SS decreases below 60 mV/dec for all reported samples.

Figure 5 reports the scalability of the device—the average value of hysteresis is plotted, along with its standard deviation for different values of *Vm*, for different device dimensions (width × gate length). Although there is some distribution in the data, the trend clearly shows polarization switching

Vstop 2.47V

|  |  |  |  |
| --- | --- | --- | --- |
| 120  60  20 120  60  40  20  2.5    3 3.5 4 4.5 5 5.5 6 6.5 7 7.5 100 100  2.47 2.83 3.19 3.55 80  60  20 120  60  40  20  2.5    3 3.5 4 4.5 5 5.5 6 6.5 7 7.5 100 100  ***SS* (mV/dec)**   80  60  20 120  60  40  20  2.5    3 3.5 4 4.5 5 5.5 6 6.5 7 7.5 100 100  80  100 100  80  60 60  40  20 20  2.5 3 3.5 4 4.5 5 5.5 6 6.5 7 7.5 *Anneal at*  550 600 500 550 600  *T* (oC) | | | ***Vm* (V)** |
| *tFE* | 5 nm | 8 nm |

Fig 4: Subthreshold slope *SS* for different oxide thicknesses, anneal temperatures, and *Vm*. Red lines connect the minimum values at each *Vm*. 3nm HfZrO does not manifest steep SS in the measured range (not shown).

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 1.2 | | Solid lines: *VG* : –*Vm* to +*Vm* | 1×0.07 m2 | Polarization switching | 3.5 |
| 1 | |
| Dotted lines: *VG* : 0 to +*Vm* |
| ***Hysteresis* Δ*Vth* (V)**  Hysteresis (V) | 0.8  0.6  0.4  0.2  0.0 |
| 10×10 m2 |
| Trapping | | |
| -0.2 | |
| -0.4 | |
| -0.6 | | 2.0 2.25 2.5 2.75 3.0 3.25  Vg max (V)  ***Maximum value of VG sweep Vm* (V)** | | |
| 1.75 | |

Fig 5: Hysteresis of FEFET for different device dimensions as a function of

*Vm*, documenting all device dimensions show stronger FE polarization at larger

*Vm*.

0.8

-3V & 3V

0V & 3V

0.6 -2.5 & 2.5

0V & 2.5V

Polarization switching Trap-  
-2V & 2V

***Hysteresis* (V)**   
 0.4 0V & 2V

0.2

0.0

ping

-0.2

-50 -25 0 25 50 75 100

***Temperature* (oC)**

Fig 6: Hysteresis of FEFET for different *VG* sweep ranges as a function of

temperature, showing the FE polarization becomes stronger at lower

temperature.

behavior dominates over trapping behavior as *Vm* increases,

down to *Lg* = 70nm.

In Fig. 6 it is seen that at lower temperatures the FE

behavior gets stronger. We assume that it is because fewer

oxide traps are filled, as gate oxide trapping is a thermally

activated process. This leads to a weaker influence of trapping

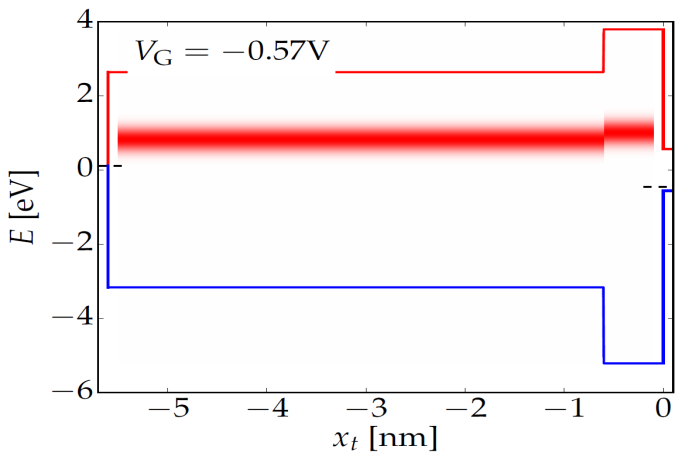
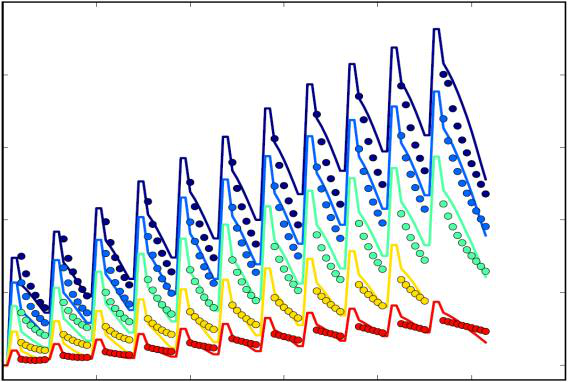
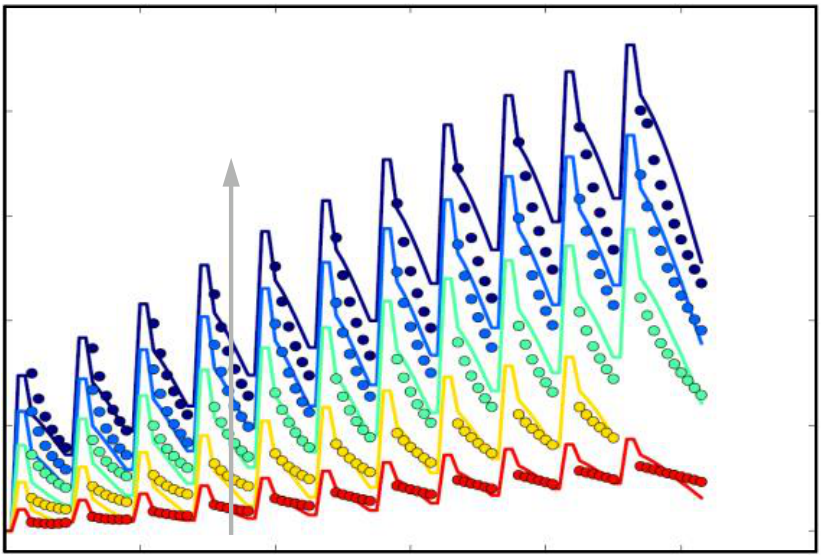
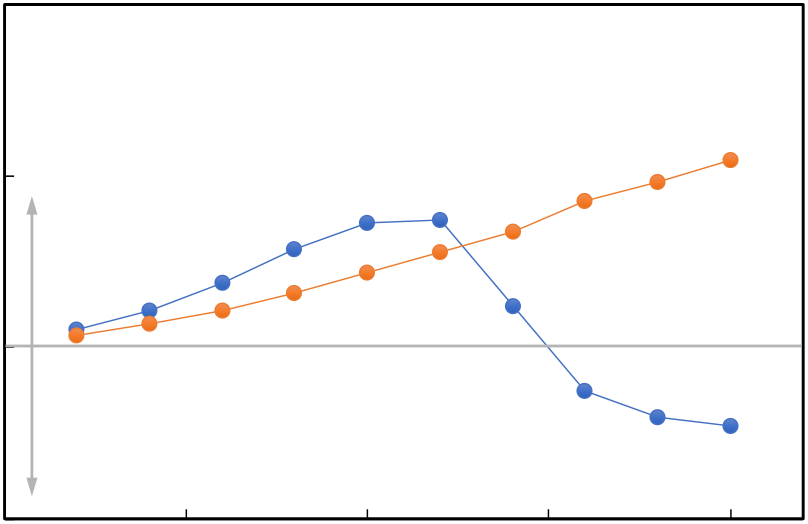
phenomena over the FE behavior.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***Minimum SS* (mV/dec)** | 140 | Trapping | Polarization switching | | [4] | 1.0 | This work | | 1.5 |
| 120 | Literature | |
| 100 | [5] | [4] | | [4] | |
| [4] | |
| 80 |
| [7] | [4] |
| 60 |
| [1]  [6]   [6]   [8] | [3] |
| 40 |
| [6] |
| 20 |
| [8] | [4] | [4] | [2] |
| 0 -0.5 | 0.0 | 0.5 |
| ***Hysteresis* (V)** | |

Fig 7: Hysteresis vs. subthreshold slope tradeoff matches well the trend

observed in the literature. The line is a guide to the eye.

2168-6734 (c) 2018 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications\_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2019.2902953, IEEE Journal of the Electron Devices Society

Our data also indicate a clear hysteresis vs. *SS* tradeoff, shown in Fig. 7. Specifically, we observe that the lower the SS value, the higher the hysteresis and vice versa. The link between SS and hysteresis could lie in *Vm*. We see that in order to get lower SS, higher *Vm* is needed. But higher *Vm* will result in more polarization and a higher hysteresis. We cross check this correlation against other published works by different groups and find a similar trend.

We note that e.g. Lee *et al.* showed nearly zero hysteresis with sub-60mV/dec switching [6]; their result, however, was found to be dependent on measurement speed. It is already established that trapping is a transient phenomenon—the longer the measurement time the more trapping occurs in the oxide. Consequently, variation of measurement speed leads to a variation of the net trapped charge and a subsequent variation of the trapping component of *Vth*. Note in Fig. 2 the trapping and depolarization give *Vth* of opposite sign. It is therefore possible that at a right measurement speed, the two components compensate each other, giving apparently zero hysteresis. In fact, with the increase in measurement speed Lee *et al.* [6] observed larger hysteresis in counter-clockwise direction (less trapping / more depolarization).

*B) Extraction of the defect band*

(“stress”) and discharging (“measurement”) cycles (Fig. 8), originally developed for BTI reliability testing [14]. Briefly, the “stress” phases (*VG* = *Vstress*) with exponentially increasing durations allow to characterize the trap capture time distributions, while measuring the detrapping (“relaxion”) during the “measurement” phase (*VG* = *Vmeas ~Vth*) allows evaluating the trap emission time distributions. Repeating the measurement at multiple *Vstress* voltages and temperatures then enables determining the complete trap properties, including their energy distribution in the Hf0.5Zr0.5O2 oxide band gap [13].

Fig. 9 shows the result of this procedure at a fixed total “stress” time and at increasing stress *VG* values, for a FE HfZrO FET and for a reference HfO2 dielectric DEFET. In case of the reference DEFET, only charge trapping occurs under the application of *Eox*. Larger *Eox* results in more trapping and consequently, *Vth* increases with the increase of *Vstress*. The same trend is observed in our FEFET at lower voltages. Above *Vstress* – *Vth* ~ 1.2 V, *Eox* is high enough for the FE oxide to start polarizing during the stress phase, resulting in negative *Vth* during the measurement phase. The defect band properties in the FE oxide can therefore be extracted from the measurements at *Vstress* – *Vth* < 1.2 V.

|  |  |  |  |
| --- | --- | --- | --- |
| Electrically active defects such as oxygen vacancies are commonly observed in high-k oxides like HfO2, ZrO2 and Hf0.5Zr0.5O2 [23]. Such defects may occur due to the imperfection of the oxide material, presence of grain boundaries, or due to the polycrystalline nature. At non-zero absolute temperature defects may be present even in a perfect crystal due the thermodynamic effects. In order to characterize the active defects in our gate oxide stack, we used a measurement scheme consisting of multiple charging | **Δ*Vth* (mV)** | 200 | *Vstress* – *Vth* = |
| 0.2, 0.4, 0.6, 0.8, 1.0 V |
| 150 |
| 100 |
| 50 |

|  |  |
| --- | --- |
| ***VG***  ***Vstress***  ***Vmeas*** | = *ID* measurement  ***...***  ***time*** |

Fig 8. Schematic of the *VG*bias sequence of trap charging (“stress”) and discharging (“measurement”) phases used to determine the distributions of trap properties.

|  |  |  |  |
| --- | --- | --- | --- |
| **Δ*Vth* (V)** | 0.4 | *T* = 25 oC  *total tstress* = 57 s  *tmeas* = 0.1 s | DE FET |
| 0.2 | Trapping |

0.0

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| -0.2 | 0.0 | Polarization switching | 1.0 | FEFET | 2.0 |
| 0.5 | 1.5 |

***Vstress* – *Vth* (V)**   
Fig 9. Unlike in a reference FET with dielectric (DE) HfO2 (5 nm) oxide, the threshold voltage shift Δ*Vth* (hysteresis) in our FEFET switches sign at high *VG* biases.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0 | 20 | 40 | 60 | 80 | 100 |
| ***time step* ()** | | |

Fig 10. An aggregate plot of *Vth* values of Hf0.5Zr0.5O2 FEFET during measurement phases vs. time steps (symbols), fitted assuming defect bands in Fig. 11 (lines) [13].

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***Energy wrt Si midgap* (eV)** | 4 | |  |  |  | | --- | --- | --- | | *VG* = -0.57 V   *Et*   |  |  | | --- | --- | | Hf0.5Zr0.5O2 | SiO2 | | | | | | | |
| 2 |
| 0 |
| -2 |
| -4 |
| -6 |
| -5 | -4 | -3 | -2 | -1 | 0 |
| ***Depth* (nm)** | | | | | |

Fig 11. Graphical representation of extracted trap bands in FE and the interfacial SiO2.

2168-6734 (c) 2018 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications\_standards/publications/rights/index.html for more information.

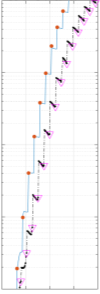
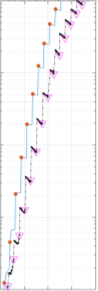
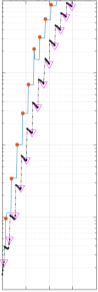
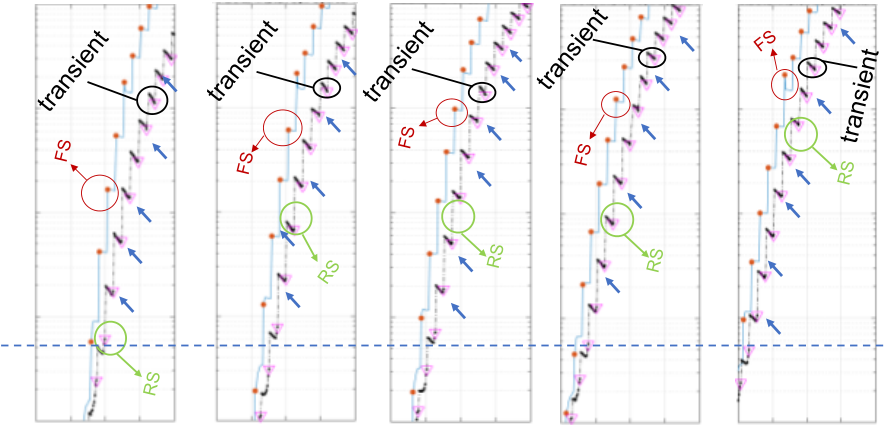
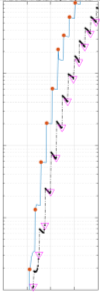
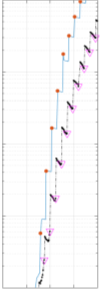
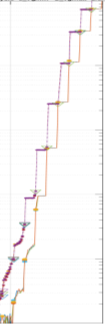
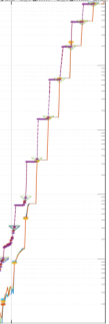
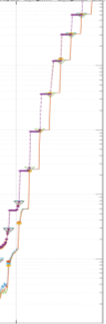
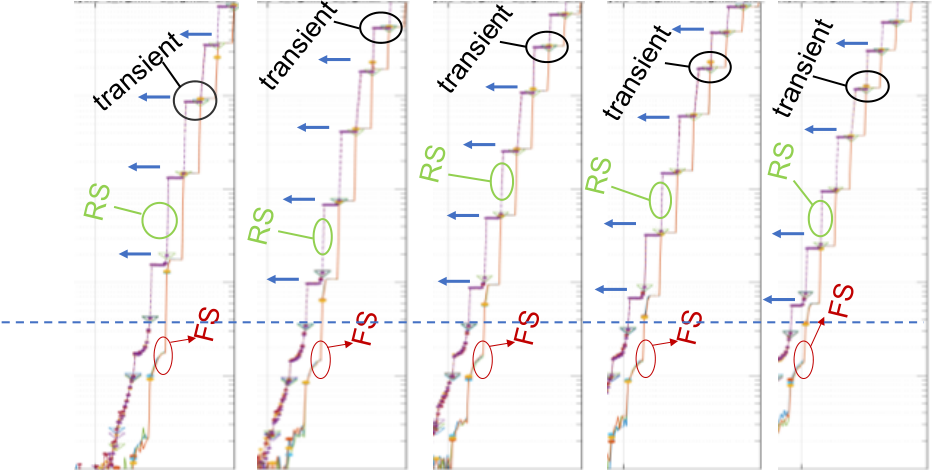
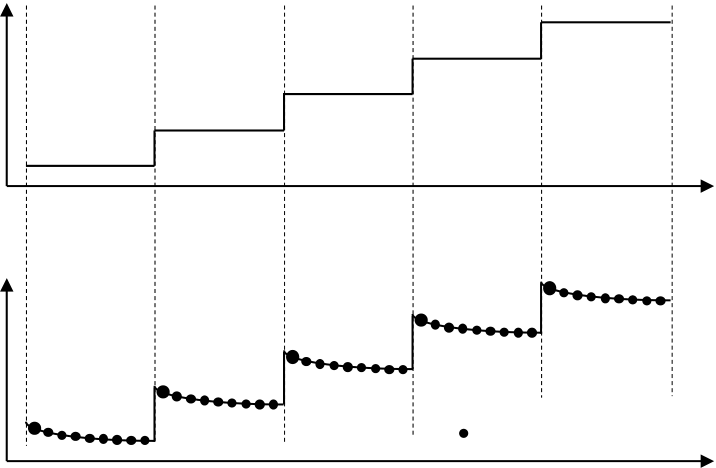
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2019.2902953, IEEE Journal of the Electron Devices Society

Fig. 10 shows *Vth* of Hf0.5Zr0.5O2 FEFET during measurement phases for varying *Vstress*. The measured data are then fitted by 2-state NMP theory incorporated into our “Comphy” tool [24] to extract the defect band properties. Both CS and GS trapping are natively considered. Details of the procedure are available elsewhere [13]. The result is shown in Fig. 11.

TABLEI   
PARAMETERS DESCRIBING THE DEFECT BAND OF HFZRO FERROELECTRIC

|  |  |  |
| --- | --- | --- |
| **Parameter** | OXIDE | **Value** |
| **Trap type** |  | Acceptor |
| 𝑬𝒕 (𝒎𝒆𝒂𝒏) **(w.r.t. Si midgap)** |  | 0.83 eV |
| 𝑬𝒕 (𝒔𝒊𝒈𝒎𝒂) |  | 0.22 eV |
| 𝑵𝒕 |  | 2.6×1020 cm-3 |
| 𝑹 |  | 0.32 |
| 𝑺 (𝒎𝒆𝒂𝒏) |  | 1.93 eV |
| 𝑺 (𝒔𝒊𝒈𝒎𝒂) |  | 1.21 eV |

In addition to the defect band in the HfZrO layer, a defect band in the interfacial SiO2 is also assumed in the fit. Table I then summarizes the parameters describing the defect band in the HfZrO layer (cf. Fig. 11) active at positive *VG* biases (n-channel FET operation), i.e., the traps responsible for counteracting FE polarization switching in our FEFET. We note that the defect band is relatively deep in energy (close to the Si midgap), which is in agreement with the nearly linear *Vth* vs. *Vstress* – *Vth* dependence in Fig. 9 [25]

*C) Transient ID-VG measurements*

To better understand the impact of trapping and polarization switching mechanisms on the *ID*-*VG* sweeps, we introduce the *transientID*-*VG* measurement technique. Shown in Fig. 12, we measure ten *ID* values at ~30 ms steps after every *VG* step of the *ID*-*VG* sweep. Using this technique, we therefore measure *the time dependence of ID after every VG step.* For *visualization purposes* we then map the measured *ID*values (Fig. 12b) onto the gate bias *VG* axis (Fig. 12a) using time as the common variable between them. The trends in the resulting *composite* graph (upward, flat, downward, or a combination) are then compared with the standard *ID*-*VG* (Fig. 2) to find out which effect dominates the operating regime of the device. We next apply the *transientID*-*VG* to SiO2, Al-HfO2 and HfZrO based FETs.

levels, the transient trend is always flat, as well as independent of temperature, owing to the low trap density in SiO2. At *lower ID* levels (~1nA to ~100nA) some upward and downward transients in the forward and reverse *VG* sweeps, respectively, are observed, which we believe may be a signature of weak trapping. At the *lowestID* levels (~10pA to ~1nA) the transients are most likely low current measurement artefacts—they are seen in all our devices and at all measurement conditions.

In an Al-HfO2 based FET, the *ID* transient trend during reverse *VG* sweep is always strongly upward (Fig. 14), consistent with CS detrapping. It is related to the fact that trap density in the high-k oxide is significantly higher as compared to that in SiO2.

Figure 15 then shows the same measurement on a HfZrO based FEFET. At -400C it is seen during the reverse sweep at low *VG* that the trend is again upward in the beginning (a signature of CS de-trapping). Interestingly, we observe in some transients that when some of the trapped charge get detrapped the trend switches its direction in the middle of the transient (inset of Fig. 15). *Hence there is an apparent*

*competition between CS de-trapping and either GS trapping*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 10-6 | -40 oC | -10 oC | 25oC | 55 oC | 85oC |

10-7

|  |  |
| --- | --- |
| ***ID* (A)** | 10-8  10-9 |

10-10

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 10-11 | 0.5 | 1.0 | 0.5 | 1.0 | 0.5 | 1.0 | 0.5 | 1.0 | 0.5 | 1.0 |

***VG* (V)**

Fig. 13: Forward- and reverse-sweep (FS and RS) *transientID*-*VG* characteristics showing transient *ID* at every *VG* step measured at different temperatures on a reference FET with 5nm thick SiO2. In the transient part, *VG* is kept constant (Fig. 12). Downward triangles indicate first current measurement after each *VG* step that corresponds to large symbon in Fig. 12 b. The arrows indicate the *ID* transient trends during reverse sweep. Below the horizontal dotted line (sub nA current), the transients are caused by instrumentation and should be disregarded.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Figure 13 shows this *composite* plot obtained on a *SiO2*-based FET at different temperatures. At *highID* / *highVG* | | | | | | ***ID* (A)** | 10-6 | -40 oC | -10 oC | 25oC | 55 oC | 85oC |
| **(a)** | ***VG,1*** | ***VG,2*** | ***VG,3*** | ***VG,4*** | ***VG,5*** | 10-7 |
| ***VG*** | 10-8 |

10-9

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **(b)** | ***ID*** | ***t*** | 10-10   0.5 | 1.5 | 0.5 | 1.5 | 0.5 | 1.5 | 0.5 | 1.5 | 0.5 | 1.5 |

***VG* (V)**

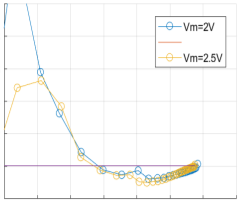
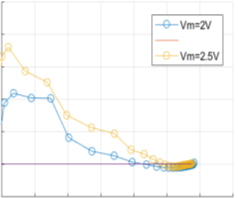
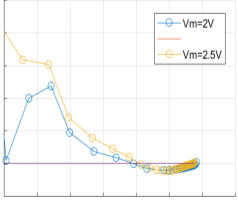
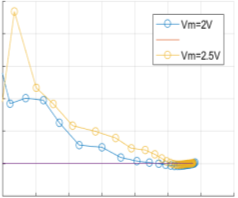
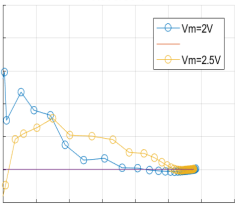
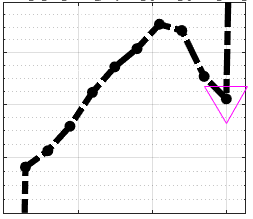
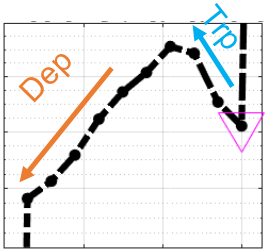
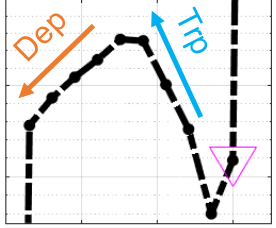
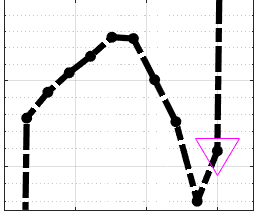
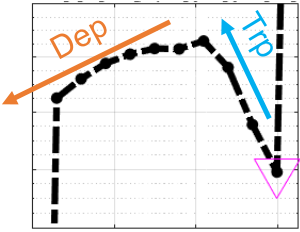
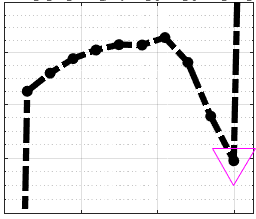
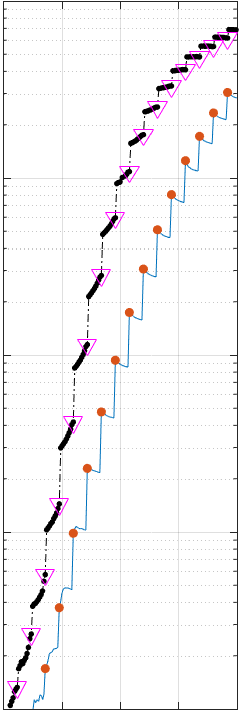
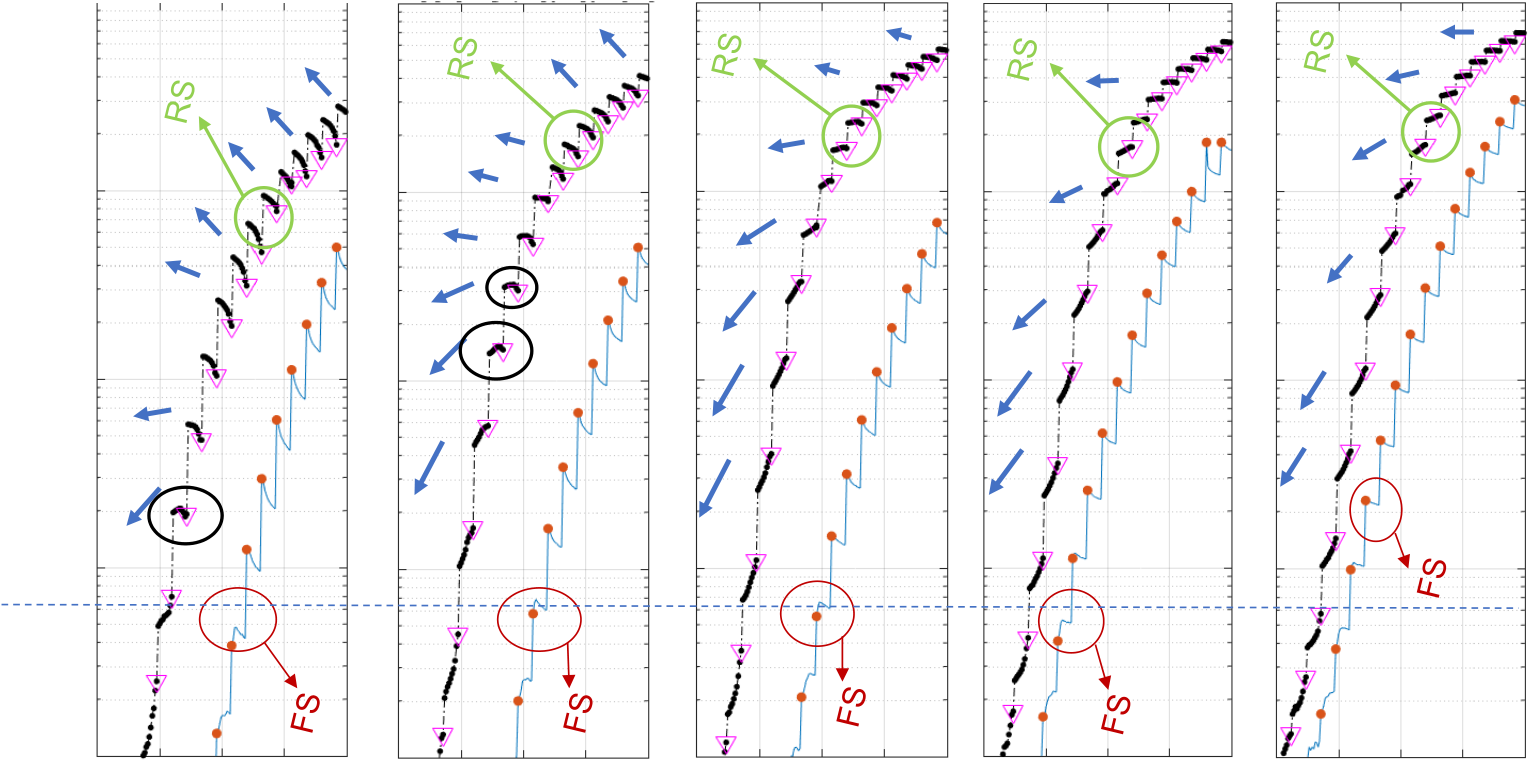
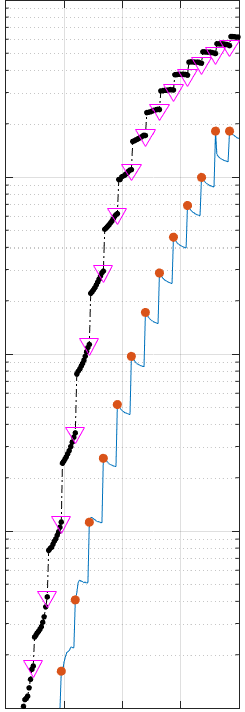
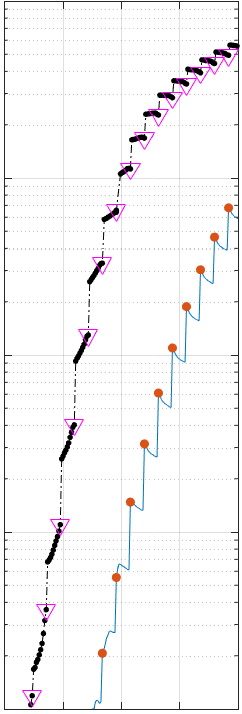
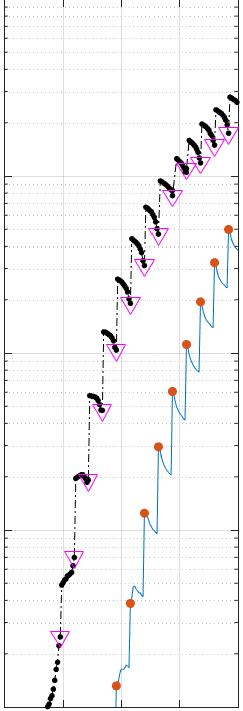
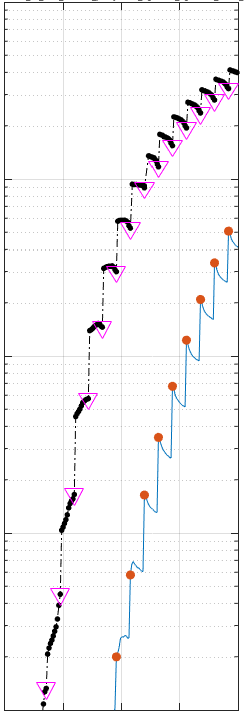
= *ID* measurement

***t***

Fig 12: During the *transientID*-*VG* measument, (a) *VG* is stepped (forward sweep shown) as a function of time, while (b) at each bias value, multiple current measurements are done. (Each first measurement desigated by a larger symbol.)

Fig. 14: Forward- and reverse-sweep (FS and RS) *transientID*-*VG* characteristics of a FET with 8nm thick Al-HfO2 measured at different temperatures. In the transient part, *VG* is kept constant (Fig. 12). Drain current *ID* always increases after every voltage down-step during reverse sweeps (indicated by the arrows) above the horizontal dotted line (sub nA current), consistent with CS detrapping. No steep slope is found in this wafer.

2168-6734 (c) 2018 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications\_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2019.2902953, IEEE Journal of the Electron Devices Society

*or FE depolarization.* Since we don’t observe domination of GS trapping in Al-HfO2 and we assume it is the case in HfZrO as well, we conclude the main cause must be FE depolarization. The trend reversal in the transient *ID*-*VG* happens at low *VG* because the depolarization field increases as *VG* is ramped down [15].

As temperature increases, the depolarization effect becomes visible even at higher *VG* values. It is because with increasing temperature the energy barrier for polarization switching goes down, which results in a decrease of coercive field [26]. Consequently, a lower depolarization field is necessary to cause the depolarization of the polarized oxide.

In Fig. 16 we plot the transient trends during the reverse sweep of *VG* by plotting difference between the logarithm of the 1st and 10th measured *ID* values. The positive values thus represent downward transient (depolarization) while negative values represent trapping. The crossover point from negative to positive value represents the level of current at which the trend reversal of the transient happened in Fig. 15. Figure 16 documents that as temperature increases, depolarization gets prominent at higher current values. In addition, it shows higher values of *Vm* lead to increased depolarization effect. This is most visible at 85oC—the depolarization occurs up to *ID* = ~5×10-8A for *Vm* = 2 V, while it occurs up to *ID* = ~10-6A for *Vm* = 2.5 V.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 10-6 | -40 oC | -10 oC | 25 oC | 55 oC | 85 oC | Dep: Depolarization Trp: Trapping |
| **(i)** |

10-7

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ***ID* (A)** | 10-8 | **(i)** | **(iii)** | **(ii)** | VG=0.36V |
| **(ii)** | VG=0.42V |
| 10-9 |

**(iii)**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 10-10 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | 0.0 | 1.0 | VG=0.48V |
| ***VG* (V)** |

Fig. 15: Forward- and reverse-sweep (FS and RS) *transientID*-*VG* characteristics of a FEFET with 5nm thick HfZrO measured at different temperatures. In the transient part, *VG* is kept constant (Fig. 12). Downward triangles indicate first current measurement after each *VG* step that corresponds to large symbon in Fig. 12 b. s During reverse sweeps (above the horizontal dotted line indicating sub nA current) this wafer showed steep subthreshold slope. The *ID* transients trend changes with the temperature (indicated by the arrows). Insets (i), (ii) and (iii) show the trend reversal of the current transient from CS detrapping to depolarization, at different current level and at two different temperatures.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ***ID*)** | -40 oC | | |  |  |  | -10 oC | | |  |  |  | 25oC | | |  |  |  | 55 oC | | |  |  | 85oC | | |  |  |
| 1.0 | | |
| 0.0 | | |
| **Log(1st *ID*) - Log(10th *ID*)** | -6 | -5 | -4 | -11 -10 -9 | -8 | -7 | -6 | -5 | -4 -11 -10 -9 | -8 | -7 | -6 | -5 | -4 | -11 -10 -9 | -8 | -7 | -6 | -5 | -4 -11 -10 -9 | -8 | -7 | -6 | -5 | -4 |
| 0.6 | | |
| 0.4 | | |
| 0.2 | | |
| 0.0 | | |
| -0.2  -11 -10 -9 | -8 | -7 |
| **Log(1st*ID*)** | | | **Log(1st*ID*)** | | | **Log(1st*ID*)** | | | **Log(1st*ID*)** | | |
| **Log(1st*ID*)** | | |

Fig. 16: The 1st and the 10th measured *ID* values are taken from the reverse sweeps of *transientID*-*VG* measurements. The difference of their logarithms represents the direction of the transients in Fig. 11. Positive values correspond to the transients coming from polarization switching while negative values correspond to detrapping. Results are plotted for different temperatures and *Vm* as a function of log(*ID*).

**Conclusion**s

We have reported HfZrO-based FEFETs scaled down to 70nm gate length. The devices show steep subthreshold slope in reverse *VG* sweep only, along with *Vth* hysteresis. Gate oxide trapping and polarization switching greatly depends on

the bias voltage range and operating temperature. Negligible effect of anneal temperature is observed. A band of active traps in the ferroelectric layer is characterized. Using our *transientID*-*VG* measurement technique we demonstrated the competition between trapping and FE behavior taking place d*uring ID-VG*measurement. This measurement scheme thus

2168-6734 (c) 2018 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications\_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2019.2902953, IEEE Journal of the Electron Devices Society

facilitates understanding of mechanisms impacting the FEFET subthreshold slope.

**Acknowledgments**

The authors gratefully acknowledge input from and discussions with M. Garcia Bardon, S. Clima, P. Matagne, P. Roussel, A. Verhulst, E. D. Litta Y. Xiang, S. McMitchell and J. Franco.

**References**

[1] J. Jo and C. Shin, "Negative Capacitance Field Effect Transistor With Hysteresis-Free Sub-60-mV/Decade Switching," *IEEE Electron Device Letters,* vol. 37, no. 3, pp. 245 - 248, 2016.

[2] J. Zhou, G. Han, Y. Peng, Y. Liu, J. Zhang, Q.-Q. Sun, D. W. Zhang and Y. Hao, "Ferroelectric Negative Capacitance GeSn PFETs With Sub-20 mV/decade Subthreshold Swing," *IEEE Electron Device Letters,* vol. 38, no. 8, pp. 1157 - 1160, 2017.

[3] P. Sharma, K. Tapily, A. K. Saha, J. Zhang, A. Shaughnessy, A. Aziz, G. L. Snider, S. Gupta, R. D. Clark and S. Datta, "Impact of total and partial dipole switching on the switching slope of gate-last negative capacitance FETs with ferroelectric hafnium zirconium oxide gate stack," in *2017 Symposium on VLSI Technology*, 2017.

[4] E. Ko, J. W. Lee and C. Shin, "Negative Capacitance FinFET With Sub-20-mV/decade Subthreshold Slope and Minimal Hysteresis of 0.48 V," *IEEE Electron Device Letters ,* vol. 38, no. 4, pp. 418 - 421, 2017.

[5] M. Si, C.-J. Su, C. Jiang, N. J. Conrad, H. Zhou, K. D. Maize, G. Qiu, C.-T. Wu, A. Shakouri, M. A. Alam and a. P. D. Ye, "Steep-slope hysteresis-free negative capacitance MoS2 transistors," *Nature Nanotechnology,* vol. 13, pp. 24-28, 2018.

[6] M. H. Lee, P.-G. Chen, S.-T. Fan, Y.-C. Chou, C.-Y. Kuo, C.-H. Tang, H.-H. Chen, S.-S. Gu, R.-C. Hong, Z.-Y. Wang, S.-Y. Chen, C.-Y. Liao, K.-T. Chen, S. T. Chang, M.-H. Liao, K.-S. Li and C. W. Liu, "Ferroelectric Al:HfO2 negative capacitance FETs," in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017.

[7] C.-J. Su and et.al., "Ge nanowire FETs with HfZrOx ferroelectric gate stack exhibiting SS of sub-60 mV/dec and biasing effects on ferroelectric reliability," in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017.

[8] J. Zhou, J. Wu, G. Han, R. Kanyang, Y. Peng, J. Li, H. Wang, Y. Liu, J. Zhang, Q.-Q. Sun, D. W. Zhang and Y. Hao, "Frequency dependence of performance in Ge negative capacitance PFETs achieving sub-30 mV/decade swing and 110 mV hysteresis at MHz," in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017.

[9] U. Schroeder, E. Yurchuk, J. Müller, D. Martin, T. Schenk, P. Polakowski, C. Adelmann, M. I. Popovici, S. V. Kalinin and T. Mikolajick, "Impact of different dopants on the switching properties of ferroelectric hafniumoxide," *Japanese Journal of Applied Physics,* vol. 53, no. 851, pp. 08LE02-1, 2014.

[10] A. Saeidi, F. Jazaeri, F. Bellando, I. Stolichnov, C. C. Enz and A. M. Ionescu, "Negative capacitance field effect transistors; capacitance matching and non-hysteretic operation," in *European Solid-State Device Research Conference (ESSDERC)*, Leuven, Belgium, 2017.

[11] M. N. K. Alam, B. Kaczer, L.-Å. Ragnarsson, M. I. Popovici, N. Horiguchi, M. Heyns and J. V. Houdt, "Investigation of ferroelectric HfZrO FET for steep slope applications," in *IEEE SOI-3D-subthreshold microelectronics technology unified conference*, San Francisco, CA, USA, 2018.

[12] T. Grasser, K. Rott, H. Reisinger, M. Waltl, J. Franco and B. Kaczer, "A Unified Perspective of RTN and BTI," in *2014 IEEE International Reliability Physics Symposium*, Waikoloa, HI, USA, 2014.

[13] G. Rzepa, J. Franco, B. O’Sullivan, A. Subirats, M. Simicic, G. Hellings, P. Weckx, M. Jech, T. Knobloch, M. Waltl, P. Roussel, D. Linten, B. Kaczer and T. Grasser, "Comphy — A compact-physics framework for unified modeling of BTI," *Microelectronics Reliability,* vol. 85, pp. 49-65, June 2018.

[14] B. Kaczer, T. Grasser, P. J. Roussel, J. Martin-Martinez, R.

O’Connor, B. J. O’Sullivan and G. Groeseneken, "Ubiquitous relaxation in BTI stressing—New evaluation and insights," in *2008 IEEE International Reliability Physics Symposium*, Phoenix, AZ, USA, 2008.

[15] T. P. Ma and J.-P. Han, "Why is nonvolatile ferroelectric memory field-effect transistor still elusive?," *IEEE Electron Device Letters,* vol. 23, no. 7, pp. 386 - 388, 2002.

[16] S. N. Fedosov and H. v. Seggern, "Back-switching of ferroelectric polarization in two-component systems," *JOURNAL OF APPLIED PHYSICS,* vol. 96, no. 4, pp. 2173-2180, 2004.

[17] R. R. Mehta, "Depolarization fields in thin ferroelectric films," *Journal of Applied Physics,* vol. 44, p. 3379, 1973.

[18] Z. Xu, B. Kaczer, J. Johnson, D. Wouters and G. Groeseneken, "Charge trapping in metal-ferroelectric-insulator-semiconductor structure with SrBi2Ta2O9∕Al2O3∕SiO2 stack," *Journal of Applied Physics,* vol. 96, p. 1614, 2004.

[19] A. Daus, C. Vogt, N. Münzenrieder, L. Petti, S. Knobelspies, G. Cantarella, M. Luisier, G. A. Salvatore and G. Tröster, "Charge Trapping Mechanism Leading to Sub-60-mV/decade-Swing FETs," *IEEE Transactions on Electron Devices,* vol. 64, no. 7, pp. 2789-2795, 2017.

[20] M. Toledano-Luque, B. Kaczer, M. Aoulaiche, A. Spessot, P. Roussel, R. Ritzenthaler, T. Schram, A. Thean and G. Groeseneken, "Analytical model for anomalous Positive Bias Temperature Instability in La-based HfO2 nFETs based on independent characterization of charging components," *Microelectronic*  *Engineering,* vol. 109, pp. 314-317, 2013.

[21] C. M. Osburn and S. I. Raider, "The Effect of Mobile Sodium Ions on Field Enhancement Dielectric Breakdown in SiO2 Films on Silicon," *ECS Journal of The Electrochemical Society,* vol. 120, no. 10, pp. 1369-1376, 1973.

[22] M. Toledano-Luque, R. Degraeve, P. J. Roussel, L.-Å. Ragnarsson, T. Chiarella, N. Horiguchi, A. Mocuta and A. Thean, "Fast Ramped Voltage Characterization of Single Trap Bias and Temperature Impact on Time-Dependent VTH Variability," *IEEE Transactions on Electron Devices,* vol. 61, no. 9, pp. 3139-3144, 2014.

[23] J. X. Zheng, G. Ceder, T. Maxisch, W. K. Chim and W. K. Choi, "First-principles study of native point defects in hafnia and zirconia," *Physical Review B,* vol. 75, p. 104112, 2007.

[24] [Online]. Available: www.comphy.eu.

[25] J. Franco, B. Kaczer, P. J. Roussel, J. Mitard, S. Sioncke, L. Witters, H. Mertens, T. Grasser and G. Groeseneken, "Understanding the suppressed charge trapping in relaxed- and strained-Ge/SiO2/HfO2 pMOSFETs and implications for the screening of alternative high-mobility substrate/dielectric CMOS gate stacks," in *2013 IEEE International Electron Devices Meeting*, Washington, DC, USA, 2013.

[26] D. Zhou, Y. Guan, M. M. Vopson, J. Xu, H. Liang, F. Cao, X. Dong, J. Mueller, T. Schenk and U. Schroeder, "Electric field and temperature scaling of polarization reversal in silicon doped hafnium oxide ferroelectric thin films," *Acta Materialia,* vol. 99, pp. 240-246, 2015.

2168-6734 (c) 2018 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications\_standards/publications/rights/index.html for more information.