IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 63, NO. 9, SEPTEMBER 2016 3501

Charge-Trapping Phenomena in HfO2-Based

FeFET-Type Nonvolatile Memories

Ekaterina Yurchuk, Johannes Müller, *Member, IEEE*, Stefan Müller, Jan Paul, Milan Peši´c, Ralf van Bentum, Uwe Schroeder, and Thomas Mikolajick, *Senior Member, IEEE*

***Abstract*—Ferroelectric field effect transistors (FeFETs) based**

**on ferroelectric hafnium oxide (HfO2) thin films show high**

**potential for future embedded nonvolatile memory applications.**

**However, HfO2 films besides their recently discovered ferro-**

**electric behavior are also prone to undesired charge trapping**

**effects. Therefore, the scope of this paper is to verify the**

**possibility of the charge trapping during standard operation of**

**the HfO2-based FeFET memories. The kinetics of the charge**

**trapping and its interplay with the ferroelectric polarization**

**switching are analyzed in detail using the single-pulse *ID*–*VG***

**technique. Furthermore, the impact of the charge trapping on**

**the important memory characteristics such as retention and**

**endurance is investigated.**

***Index Terms*—Charge-trapping phenomena, data retention,**

**endurance,**  **ferroelectric**  **memories,**  **ferroelectric**  **transistor,**

**HfO2-based FeFET.**

I. INTRODUCTION

**F** recently restored their reputation as potential candidates ERROELECTRIC field effect transistors (FeFETs) have

for future nonvolatile memory application due to the discovery

of the ferroelectricity in HfO2 thin films [1]. Introduction

of this material allows overcoming the main draw-

backs of the conventional perovskite ferroelectric materials

(e.g., PZT and SBT) such as limited device scalability and

incompatibility to the CMOS process. In contrast to the

Manuscript received March 7, 2016; revised May 1, 2016 and June 7, 2016;

accepted July 1, 2016. Date of publication July 22, 2016; date of current

version August 19, 2016. This work was supported in part by the European

Regional Development Fund of the European Commission within the Scope

of Technology Development and in part by the Free State of Saxony. The

review of this paper was arranged by Editor R. Huang. *(Corresponding author:*

*Ekaterina Yurchuk.)*

E. Yurchuk was with NaMLab gGmbH, Dresden 01187, Germany. She is

now with Anvo-Systems Dresden GmbH, Dresden 01109, Germany (e-mail:

ekaterina.yurchuk@gmail.com).

J. Müller and J. Paul are with the Center Nanoelectronic Technologies,

Fraunhofer Institute for Photonic Microsystems, Dresden 01099, Germany

(e-mail: johannes.mueller@ieee.org; jan.paul@cnt.fraunhofer.de).

S. Müller is with NaMLab gGmbH, Dresden 01187, Germany (e-mail:

stefan.mueller@namlab.com).

Germany (e-mail: milan.pesic@namlab.com; uwe.schroeder@namlab.com). M. Peši´c and U. Schroeder are with NaMLab gGmbH, Dresden 01187,

R. van Bentum is with GlobalFoundries Dresden Module One

LLC and Company, KG, Dresden 01109, Germany (e-mail:

ralf.vanbentum@globalfoundries.com).

T. Mikolajick is with NaMLab gGmbH, Dresden 01187, Germany,

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| and | also | with | the | Institute | | of | Semiconductors | | and | Microsystems, | |
| Technische | | Universität | | | Dresden, | | Dresden | 01187, | Germany | | (e-mail: |
| thomas.mikolajick@namlab.com). | | | | | | |

Color versions of one or more of the figures in this paper are available

online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2016.2588439

conventional lead-based ferroelectric materials, HfO2-based films are standard in the current high-*k* metal gate technology and therefore do not require any special integration solutions. Scalability down to the state-of-the-art 28-nm technology node has been recently demonstrated for FeFETs based on HfO2 ferroelectrics [2]. Scaling below the 28-nm technology node can be continued by fabricating FeFETs in nonplanar configurations such as FinFET devices or 3-D memory array architectures [3], [4]. The suitability of ferroelectric HfO2 thin films for 3-D integration has been already proved, as reported elsewhere [5]. Even though the ferroelectric FinFET cell design will certainly require a pitch relaxation due to a thicker gate-stack (5–10 nm) than in logic transistors (∼4 nm), memory cell size can be reduced below the cur-rent state-of-the-art floating-gate devices. Moreover, embedded memory integration will be simplified in the case of using HfO2-based FeFETs, since their fabrication flow is similar to standard high-*k* metal gate transistors [2]. With 2–3 additional masking steps [2] instead of 9–12 required for floating-gate transistors these FeFET memory blocks can be easily processed together with standard logic devices. Moreover, HfO2 films doped with 3.8 mol% of silicon (Si:HfO2) were shown to exhibit ferroelectric properties in a wide temperature of 10 years’ data retention at 150 °C was demonstrated for the range between −100 °C and 200 °C [5]. In addition, a potential Si:HfO2-based ferroelectric transistors [6]. Therefore, it can be concluded that ferroelectric memories based on Si-doped HfO2 might be utilized even in products intended for automotive applications.

Due to the recent discovery of the ferroelectricity in HfO2 thin films [7], a complete understanding of some special phenomena as well as their impact on the device performance are not yet reached. One of such phenomena is the interplay between ferroelectric switching and charge trapping. HfO2 materials are characterized by high intrinsic defect densities (1012–1014cm−2) [8], [9]. The ionic type of bonding that includes electrons from the d-shells [10], [11] in combina-tion with a high coordination number represents the main cause of the high defect concentration in HfO2. These intrinsic defects can serve as electron [8], [11] and/or hole traps [12], [13], and are believed to have a strong impact on the behavior of the high-*k* CMOS logic transistors. The mobility degradation [14], [15], *V*TH instability [8], [16] and reliability issues [17]–[19] (e.g., negative and positive bias temperature instability as well as enhanced stress-induced

0018-9383 © 2016 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications\_standards/publications/rights/index.html for more information.

3502 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 63, NO. 9, SEPTEMBER 2016

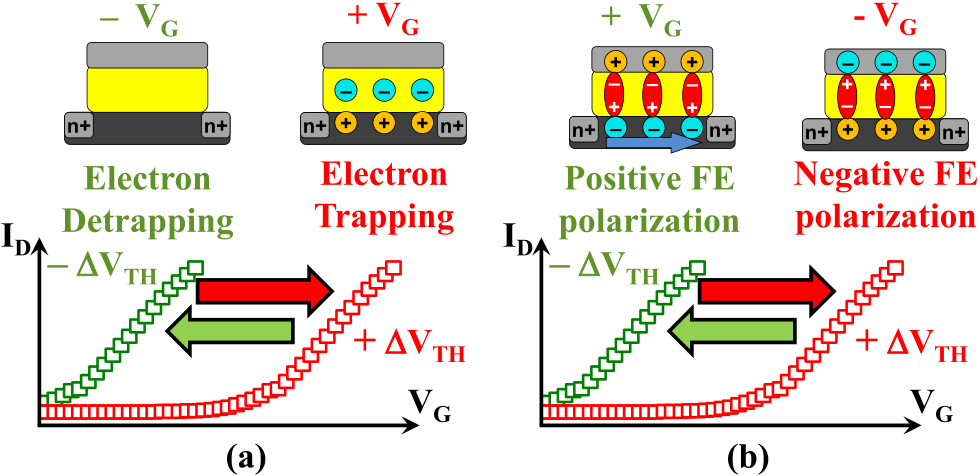


Fig. 1. (a) Impact of trapped electric charges and (b) ferroelectric polar-ization on the threshold voltage of a field effect transistor and shift of its *ID*–*VG* characteristic.

leakage current) are attributed to the intrinsic HfO2 defects. Oxygen vacancies [11], [20], [21] and oxygen interstitial atoms [11], [21], [22] are considered to be the main origin of traps in HfO2-based materials. It has been suggested that oxygen vacancies introduce shallow (*ET* = 0*.*3–1.0 eV) as well as deep electron trap states (*ET >* 1*.*5 eV) into the HfO2 band gap depending on their charging state [9], [19]–[21], [23]. Therefore, an impact of charge trapping on the performance of HfO2-based FeFETs can be expected. As can be seen from Fig. 1 the charge trapping induces *V*TH shift, which is opposite to the *V*TH shift caused by the ferroelectric switching for the same polarity of the gate voltage. For example, electrons trapped within the gate dielectric at positive gate voltage result in a positive shift of the *ID*–*VG* characteristic. On the other side, positive ferroelectric polarization induced by the same positive gate voltage leads to a negative *ID*–*VG* shift. Therefore, a superposition of both mechanisms will result in the reduction of the memory window for FeFET devices. Moreover, parasitic charge trapping effects were argued to cause the endurance degradation of HfO2-based FeFETs [24]. However, no solid evidence of the charge trapping effects in these devices was presented so far. Therefore, the scope of the present paper is to study the trapping phenomena in HfO2-based ferroelectric memory transistors. The trapping kinetics and its interplay with the ferroelectric switching were analyzed. Moreover, we discuss the possibility to eliminate trapping as well as the impact of trapping on retention and endurance as the main memory characteristics.

II. EXPERIMENTAL DETAILS

The HfO2-based FeFETs studied in this paper were manufactured using a state-of-the-art 28-nm high-*k* metal-gate technology [2]. The gate-stack consists of a 1.2-nm interfa-cial SiON layer, 9-nm Si-doped HfO2 (Si:HfO2) layer, and 8-nm TiN metal layer. Devices with three different composi-tions of Si:HfO2 films (3.7, 4.4, and 5.6 mol% SiO2) were manufactured. The gate structure of the studied ferroelectric transistors is very similar to that of a high-*k* metal gate logic transistor. The main difference of a FeFET stack is a thicker and crystalline Si-doped HfO2 film that is used instead of about 2 nm thin amorphous HfO2 layer. All measurements shown in this paper were performed on devices with a

gate width (*WG*) and gate length (*LG*) of 300 and 32 nm, respectively.

The charge-trapping and detrapping within the high-*k* layer of logic transistors are commonly characterized by means of a single-pulse *ID*–*VG* technique [8], [25], [26]. It can provide a time resolution of several nanoseconds [27], which allows to study the fast transient nature of the trapping and detrapping effects within the high-*k* layers. In this paper, we applied the single-pulse technique to examine the trapping phenomena in Si:HfO2-based ferroelectric transistor memories. Due to the similarity of the gate-stack structure of the studied devices to logic transistors, similar time constants for trapping and detrapping processes in the range of several microseconds or even less are expected.

The single-pulse measurements were performed on a tran-sistor structure, which was connected in an inverter circuit configuration with a load resistance [26]. A stress pulse was applied to the gate (*VG*), whereas the drain is biased at a constant voltage. An oscilloscope was used to sense simultaneously the voltages at the drain that is later converted into a drain current (*ID*). This measurement procedure allowed recording the *ID*–*VG* characteristics directly at the rising and falling edges of a gate stress pulse. Thereby the time delay between the stressing and the sensing and, therefore, the amount of charge possibly lost during this delay were practically eliminated. A quantitative estimation of the amount of charge trapped during the stress pulse was made from the threshold voltage shift (*�V*TH) of the *ID*–*VG* characteristics as proposed in [28]. The measurement setup used in this paper allowed exploiting the single gate pulses with rise/fall transition times of 500 ns, while the drain voltage was set to 300 mV in order to maximize the signal-to-noise ratio. The *V*TH values were extracted using a constant drain current criterion *I*TH of 3 · 10−6A · *(WG/LG)* [29], [30].

III. RESULTS AND DISCUSSION

*A. Device Behavior Dependent on the Si:HfO2 Composition*

The composition of Si:HfO2 has a strong influence on the crystalline structure of the films and, as a result, on their electrical properties. SiO2 doping of 3–4 mol% enables the stabilization of a ferroelectric phase (orthorhombic Pbc21) and, thus, obtaining the ferroelectric behavior in HfO2 films [7], [31]. The same trend was observed for transistor structures, including HfO2 layers with varying silicon con-tent (3.7, 4.4, and 5.6 mol% SiO2) (Fig. 2). The response of the *ID*–*VG* characteristics on the negative (−6 V) and positive (+6 V) gate pulses of 100 ns length changed depend-ing on the composition of the gate insulator. Devices with Si:HfO2 layers containing 3.7 and 4.4 mol % SiO2 showed an *ID*–*VG* shift opposite to the polarity of the applied gate pulses, which is characteristic for ferroelectric switching. HfO2 layers with 5.6 mol% SiO2, on the other hand, exhibited a prevailing charge trapping properties. Here, the *ID*–*VG* characteristics shifted in the direction similar to the polarity of the applied gate pulse. A more extended range of compositions for Si:HfO2 used as a gate dielectrics of CMOS transistors was

YURCHUK *et al.*: CHARGE-TRAPPING PHENOMENA IN HfO2-BASED FeFET-TYPE NONVOLATILE MEMORIES 3503

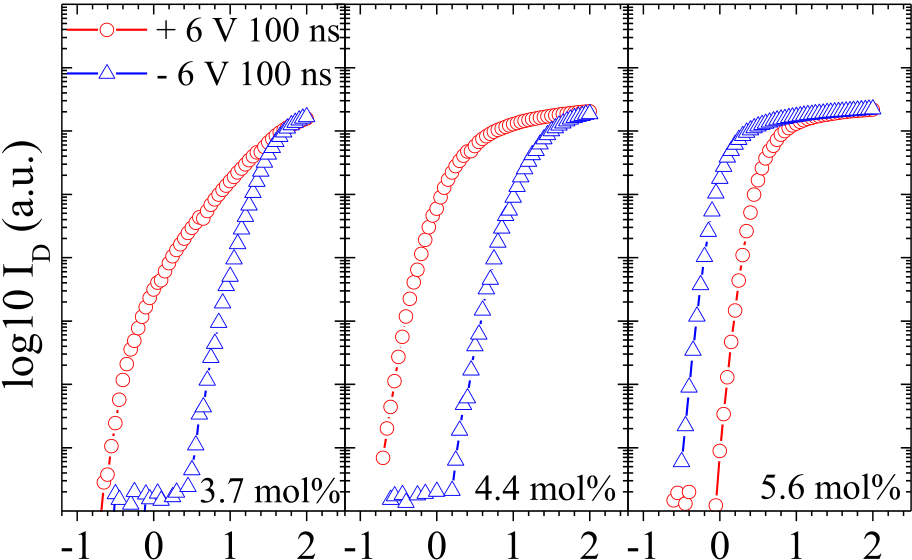


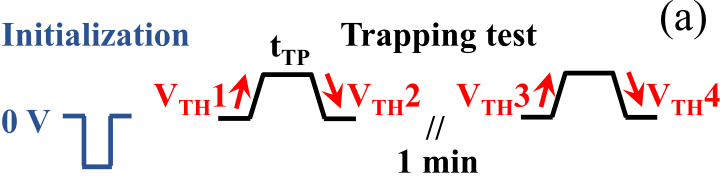
  

Fig. 2. *ID*–*VG* characteristics after positive (+6 V for 100 ns) and negative (−6 V for 100 ns) gate pulses for devices with different compositions of Si:HfO2 layer (3.7, 4.4, and 5.6 mol% SiO2).

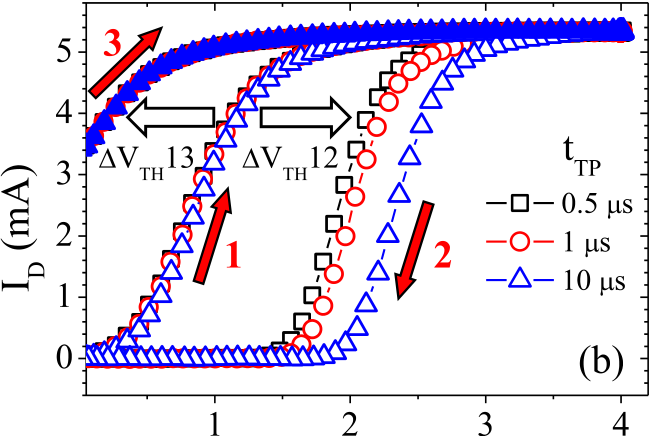
studied in [32]. In addition, here the ferroelectric behavior could be identified only in devices containing HfO2 films with compositions stabilizing a ferroelectric phase. Transistors manufactured in the present work demonstrated the most dis-tinct ferroelectric properties for the HfO2 doped with 4.4 mol% SiO2 (Fig. 2). Therefore, all further studies on the interaction between the ferroelectric switching and charge trapping will be performed on devices with this film composition.

*B. Trapping in Si:HfO2-Based FeFET Devices*

The interplay between the ferroelectric switching and charge trapping in HfO2-based FeFET devices was studied using the single-pulse *ID*–*VG* technique. The gate pulse sequence depicted in Fig. 3(a) was used for this purpose. At first a neg-ative pulse of −6 V was applied for 100 ns in order to estab-lish a saturated negative polarization state. It was followed by two consecutive single-pulses with positive amplitude to analyze the electron trapping superimposed on the ferroelec-tric polarization switching. The first positive pulse switched the ferroelectric polarization to the positive state. From the *V*TH shift between the *ID*–*VG* characteristics obtained on the rising (*V*TH1) and falling (*V*TH2) edges of this pulse the dom-inating mechanism, ferroelectric switching (*�V*TH *<* 0) or parasitic electron trapping (*�V*TH *>* 0), could be identified. The second single-pulse was applied with a time delay of









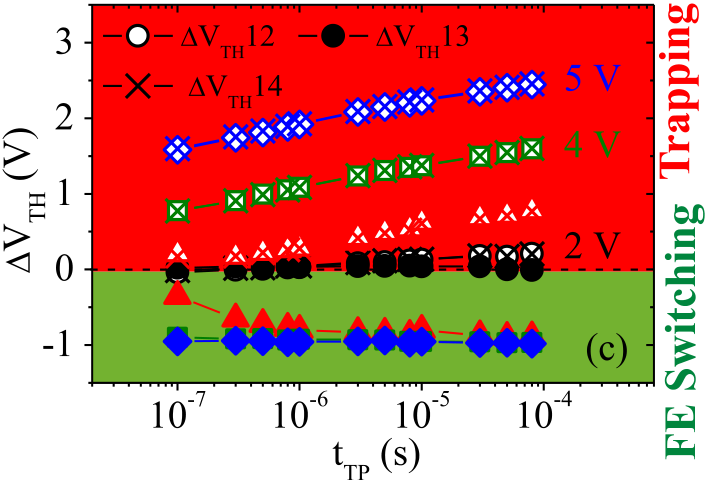


Fig. 3. Study of the superposition of the ferroelectric switching and charge trapping in Si:HfO2-based FeFET cells. (a) Experimental gate pulse sequence. (b) *ID*–*VG* characteristics measured on the rising (1) and falling (2) edges of the first single-pulse as well as after a delay of 1 min (3) for positive pulsewidth of 0.5, 1 and 10 *μ*s. (c) *V*TH shift directly after the pulse (*�V*TH12), after a delay of 1 min (*�V*TH13) and directly after the second positive pulse (*�V*TH14) as a function of pulsewidth for different pulse amplitudes.

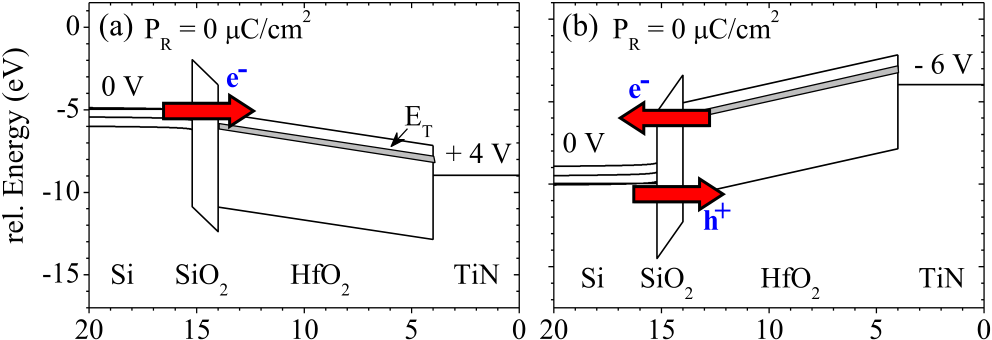
of one minute. The *ID*–*VG* characteristics on the rising edge of the second pulse (3) were shifted negatively with respect to the characteristic (1). This negative shift can be explained only in terms of ferroelectric polarization switching and not by electron detrapping only, especially if the latter occurs at zero gate voltages as in our case. The ferroelectric switching occurred during the first positive pulse simultaneously to the electron trapping. When the electron detrapping process has set in after 1-min delay, a positive ferroelectric polarization

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| one minute. *V*TH3 and *V*TH4 are the threshold voltage values extracted on its rising and falling edges, respectively. Fig. 3(b) shows the results of a trapping test for single-pulses with an | determined the final *V*TH shift [Fig. 1(b)]. | | | | | | | | | |
| Furthermore, | | the | same | measurements | | | procedure | | was |
| performed | with | positive | | pulses | of | varying | | amplitude | |

amplitude of +4 V and three different pulsewidths of 0.5, 1, and 10 *μ*s. These pulse conditions were identified in previous studies [6], as sufficient for establishing a positive ferroelec-tric polarization state (ON memory state) of the HfO2-based ferroelectric memory transistors with a gate-stack similar to that studied in this paper. For all tested pulsewidths the *ID*–*VG* characteristics obtained on the falling edge of the first pulse (2) exhibited a positive shift with respect to the charac-teristic obtained on their rising edges (1) [Fig. 3(b)]. Therefore, in all cases, the electron trapping was the dominant mecha-nism. The sign of the shift changed, however, after a delay

(from 2 to 5 V) and width (from 100 to 100 *μ*s). A neg-ative polarization state was reestablished each time before the positive double single-pulse sequence by applying an initialization pulse of −6 V for 100 ns. Fig. 3(c) shows the *V*TH shift directly after the first (*�V*TH12) and the second (*�V*TH14) positive pulses as well as after a delay of one minute (*�V*TH13) versus the single-pulsewidth (*t*TP) for dif-ferent pulse amplitudes. *�V*TH12 was positive for amplitudes above 2 V, which indicated the prevalence of the trapped electron charge directly after the applied positive pulse. The positive *V*TH shift grew for higher pulse amplitudes and

3504 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 63, NO. 9, SEPTEMBER 2016



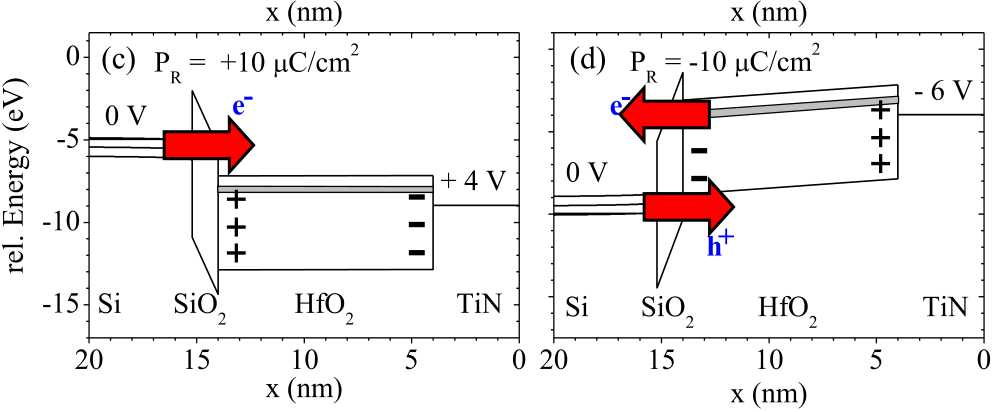


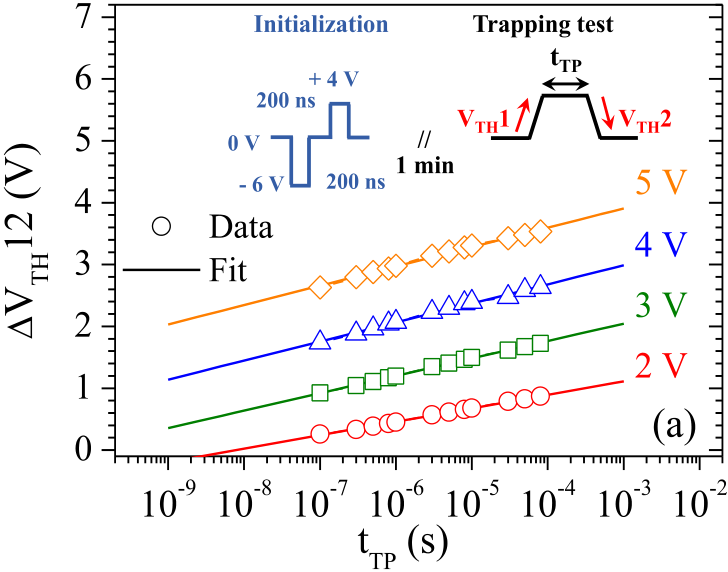
Fig. 4. Energy band diagrams of the p-Si/SiO2/HfO2/TiN stack under positive (+4 V) and negative (−6 V) gate voltage, representing erase and program operation of the Si:HfO2-based FeFET memory cell. (a) and (b) Case of a paraelectric HfO2 (*PR* = 0 *μ*C/cm2) and (c) and (d) ferroelectric HfO2 (*PR* = 10 *μ*C/cm2). The directions of the electron (e−) and hole (h+) flows are shown by arrows. The arrow size represents the tunneling probability.

widths, evidencing an increasing amount of trapped electrons. This response of *V*TH shift to the pulse amplitude and widths is typical for charge trapping mechanism [26]. The *�V*TH13, on the other hand, was negative for all pulses. Here, the ferroelectric polarization charge exceeded the trapped electron charge, when the detrapping processes have set in after a delay of one minute. Saturation of the *�V*TH13 observed for high positive pulse amplitudes and long pulses can be attributed to the characteristic saturation of the ferroelectric polarization. A saturated nature of the ferroelectric polarization and nonsaturated behavior of the charge trapping can explain the nonlinear behavior of the memory window with respect to pulsewidth and amplitude that was reported in previous studies of the HfO2-based FeFETs [33]. Superimposition of charge trapping on the ferroelectric polarization switching was proposed as an explanation for the observed memory window behavior. This assumption could be confirmed in this paper by implementation of the single-pulse technique. In addition this paper shows that the charge trapping occurs and superimposes with the ferroelectric switching already at pulsewidths shorter than 1 *μ*s.

Another interesting observation is that the charge trap-ping in the studied Si:HfO2-based FeFETs correlated with the ferroelectric switching [Fig. 3(c)]. Almost no trapping (*�V*TH12 = 0) was detected for 2 V, where also no fer-roelectric switching took place (*�V*TH13 = 0). An electron trapping started at 3 V (*t*TP about 1 *μ*s) and corresponded with the completion of the ferroelectric switching (saturation of *�V*TH13). In order to clarify the impact of ferroelectric

|  |
| --- |
| remnant polarization (*PR*) on the charge-trapping behavior of the gate-stack we performed a simulation of the energy band |

diagram using software of reference [30]. Fig. 4 shows the results of the simulation for a p-Si/SiO2/HfO2/TiN gate-stack under a positive (+4 V) and negative (−6 V) gate voltage for two cases: (a, b) paraelectric HfO2 layer (*PR* = 0 *μ*C/cm2)



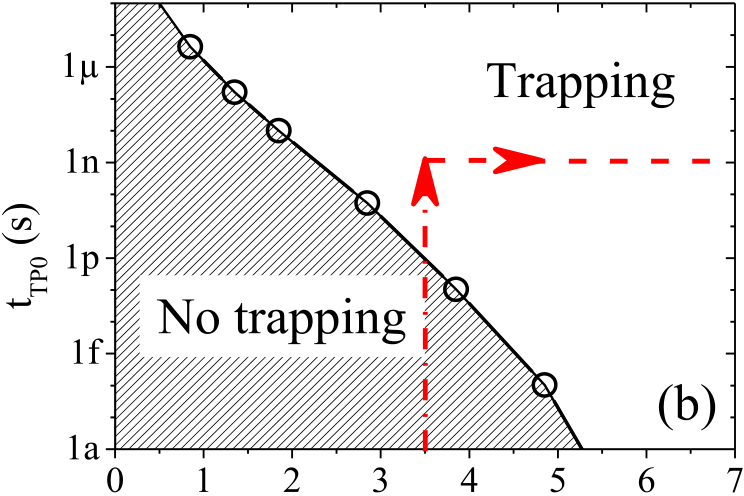




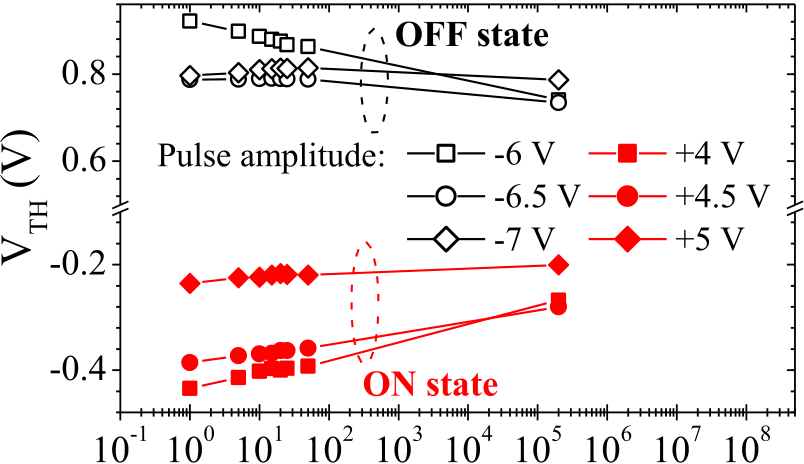
Fig. 5. Trapping characteristics of the Si:HfO2 FeFET structures in a positively polarized state. (a) *�V*TH between the rising and falling edges of a trapping pulse as a function of the pulsewidth for varying gate voltages: experimental data (symbols) and fit (lines). Inset: experimental gate pulse sequence. (b) Trapping onset time (*t*TP0) as a function of the gate voltage.

and (c, d) ferroelectric HfO2 layer (*PR* First of all it can be seen, that charge injection from the = 10 *μ*C/cm2).

transistor channel via Fowler–Nordheim or direct tunneling has a higher probability due to a thinner potential barrier than injection from the gate. The cause is 1.2 nm thin interfacial SiON layer and its stronger band banding resulting from a lower relative permittivity (∼3.9) than that of HfO2 (∼25). Moreover, in comparison to the high-*k* gate-stack with a nonferroelectric HfO2 layer [Fig. 4(a), (b)], the channel charge injection into the ferroelectric transistor [Fig. 4(c), (d)] is fur-ther enhanced. The internal fields induced by the polarization charge at the SiON/HfO2 interface alter the effective thickness of the tunneling barrier and, thus, the injection probability. The positive ferroelectric polarization established at positive gate voltages assists the electron injection. Under negative gate voltages a negative polarization is induced, which facilitates hole injection (h+) into the HfO2 and back tunneling of trapped electrons at the same time. Therefore, steady transfer of charges through the interfacial layer is inevitable in the ferroelectric stack under alternating program/erase pulses.

In the next step, an estimation of the pulsewidth corre-sponding to the onset of the electron trapping at positive voltages was performed. The trapping behavior of the FeFET structure with a positively polarized Si:HfO2 layer was used for this purpose under the assumption that the ferroelectric switching preceded the charge trapping. This assumption was

YURCHUK *et al.*: CHARGE-TRAPPING PHENOMENA IN HfO2-BASED FeFET-TYPE NONVOLATILE MEMORIES 3505



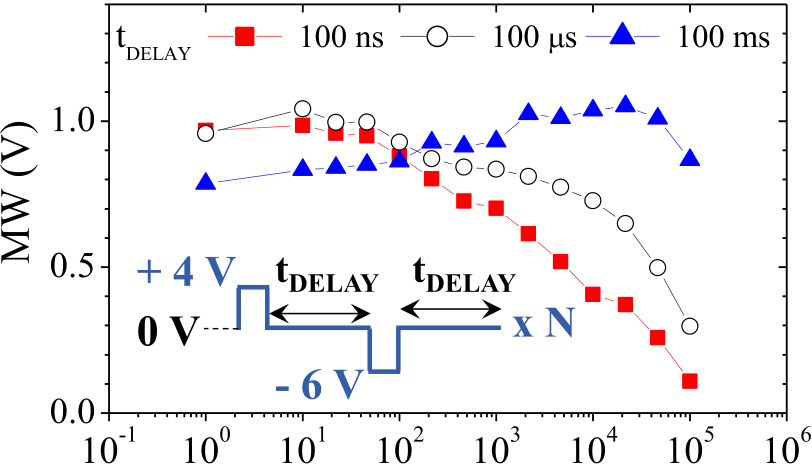


Fig. 6. Retention characteristics of Si:HfO2-based FeFET cells at 30 °C

after program/erase pulses with varying amplitude.

Fig. 7. Endurance behavior of the Si:HfO2-based FeFET cells: Memory

window as a function of the number of program/erase cycles with varying

time delay between pulses (*t*DELAY) of 100 ns, 100 *μ*s and 100 ms.

Inset: gate pulse sequence used for endurance testing.

supported by the equality of the trapped charge during the

first switching and the second nonswitching single pulses [*�V*TH12 = *�V*TH14 see Fig. 3(c)]. Therefore, the analyses were performed using the pulse sequence shown in the inset of Fig. 5(a). Before each trapping pulse, a positive polarization state was reestablished with a combination of a negative (−6 V for 200 ns) and a positive (+4 V for 200 ns) pulses. A time delay of 1 min between the initialization pulse sequence and a trapping single-pulse allowed the detrapping processes to set in. The resulting trapping characteristics (*�V*TH12) are shown as a function of the trapping pulsewidth for varying pulse voltages [Fig. 5(a)]. The experimental data (symbols) were extrapolated (lines) to the zero *�V*TH12. The intersection with the time axis gives the pulsewidth that corresponds to the onset of trapping (*t*TP0).

This *t*TP0 is equivalent to the critical trapping time intro-duced in [16]. The voltage dependence of the *t*TP0-value [Fig. 5(b)] identifies two ranges for operation conditions with excluded or comprised parasitic charge trapping. It becomes obvious that for erase voltages above 3.5 V applied for sev-eral nanoseconds ferroelectric switching cannot be separated from the accompanying charge trapping. For the conventional perovskite ferroelectrics polarization switching is normally significantly faster than the charge trapping. In case of the studied FeFET devices it seems not to apply. The reason of the unusually fast trapping is a combination of the high electric field required for polarization switching in HfO2-based ferroelectrics (1–3 MV/cm) and a thin interfacial layer of the transistor gate-stack.

*C. Impact of Trapping on the Device Performance*

From the trapping analyses it can be seen that the charge trapping cannot be completely excluded during the standard erase operation. Therefore, it is expected to impact the per-formance of the HfO2-based FeFET memories. Thus, the influence of trapping on the retention and endurance properties of these devices was examined in this paper.

As it was clearly seen form Fig. 3, charge trapping and fer-roelectric switching cannot be separated in a given sample just by changing the operation conditions of the cell. In order to achieve nonvolatile retention the ferroelectric switching effect needs to dominate over charge trapping. This state is achieved

after retention time of a few seconds, when significant part of the trapped charges has detrapped. Fig. 6 shows the nonvolatile retention characteristics for program/erase pulses with varying amplitudes. The width of all program/erase pulses used was constant and amounted to 100 ns. A reduced memory window appears to be a consequence of an increased program and erase amplitude. For higher program/erase voltages the *V*TH shifted to more negative/positive values, indicating an enhancement of the hole/electron trapping, respectively. These trapped charges within the HfO2 layer compensated the ferroelectric polariza-tion and resulted in reduced ferroelectric memory window. On the other hand, the time dependent *V*TH decay decreased for both memory states with increasing amplitudes of the program/erase voltages. This can be explained by the lowering of the depolarization field as a result of the compensation of the ferroelectric polarization by trapped charges, which led to more stable retention behavior.

Limited endurance properties of HfO2-based FeFETs were previously argued to originate from parasitic charge trap-ping [24]. A continuous charge transport through the inter-facial SiON layer was assumed during program/erase cycling. This results in the wear-out of the interfacial layer, which, in turn, leads to a deterioration of the memory window. An exper-imental evidence of a strong electron trapping at typical erase operation conditions has been demonstrated in this paper. This justifies the endurance model proposed in [24]. Moreover, in order to get better insight into the correlation between the electron trapping and endurance an impact of the time delay between the erase and program pulses was studied (Fig. 7). The memory cell was continuously stressed with alternating program (−6 V for 100 ns) and erase pulses (+4 V for 100 ns). After a certain number of program/erase pulses the memory cell was set in turns into programmed and erased state and a corresponding memory window (MW) was determined. The endurance characteristics were measured for stress sequences which differed by time delays (*t*DELAY) between the program and erase pulses (100 ns, 100 *μ*s, and 100 ms). A slowing down of the memory window degradation was observed for longer delay times. This behavior can be again explained in terms of charge trapping. For short *t*DELAY the detrapping of most of the electrons that were trapped during positive

3506 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 63, NO. 9, SEPTEMBER 2016

erase pulse occurs under a negative voltage of the subsequent program pulse. From the reliability studies of the high-*k* gate stacks it is known that detrapping under negative voltages leads to degradation of the interfacial layer [34]. According to the anode hole injection theory [35] the damage of the interfacial layer is mainly caused by hot holes injected from the silicon substrate into the gate-stack. At negative voltages these holes

|  |
| --- |
| become more deleterious since they exhibit higher energies |

|  |
| --- |
| gained from the electrons tunneling-back into the substrate |

also with higher energies. For longer *t*DELAY electrons that were captured during the erase pulse had sufficient time to be detrapped at 0 V before the subsequent negative program pulse. Therefore, the interfacial layer was less damaged in this

|  |
| --- |
| latter case due to lower energies of the tunneling-back elec- |

trons and, thus, lower energies of the injected holes. As a result the endurance behavior improved visibly for longer delay times (Fig. 7). Endurance capability of 105program/erase cycles was achieved with *t*DELAY of 100 ms.

IV. CONCLUSION

HfO2-based FeFETs reveal high potential for future embedded memory applications. Their main advantages in comparison to ferroelectric transistors based on perovskite ferroelectrics are full CMOS compatibility and better scaling capability. In order to get better understanding of the device behavior the charge trapping phenomena in FeFETs based on Si:HfO2 ferroelectric thin films were studied in this paper. Experimental evidence for the charge trapping superimposing the ferroelectric polarization switching during standard device operation was demonstrated using the single-pulse technique. The characteristic trapping times in the studied ferroelectric gate stacks were shorter than those known for the standard high-*k* metal gate stacks [25]. We argue that the main cause of this behavior is the ferroelectric polarization of Si:HfO2 layers that significantly enhances the trapping rate. Modification of the gate-stack structure or/and use of the HfO2 layer with lower ferroelectric polarization will be required for the complete mitigation of the parasitic trapping during device operation. Furthermore, the charge trapping was shown to have a strong impact on the main memory characteristics such as data retention and endurance. The trapped charges improve on the one hand the data retention due to reduction of the depolar-ization field. They are, however, at the same time responsible for the limited endurance capability. The detrapping of the trapped charges is a deleterious effect which triggers the degradation of the interfacial layer in the gate-stack. As a result the endurance characteristics are strongly dependent on the time delay between the erase and program pulses. If detrapping is allowed to set in before the pulse of the opposite polarity is applied, the endurance capability can be extended from 104to 105program/erase cycles.

REFERENCES

[1] International Technology Roadmap for Semiconductors, *Report ‘Emerg-ing Research Devices’ (Edition 2013 Full version)*. Washington, DC, USA: Semiconductor Industry Association, 2013, pp. 12–13.

[2] J. Müller *et al.*, “Ferroelectricity in HfO2 enables nonvolatile data storage in 28 nm HKMG,” in *Proc. Symp. VLSI Technol. (VLSIT)*,

[3] R. Katsumata *et al.*, “Pipe-shaped BiCS flash memory with 16 stacked layers and multi-level-cell operation for ultra high density storage devices,” in *Proc. Symp. VLSI Technol.*, Jun. 2009, pp. 136–137.

[4] J. Jang *et al.*, “Vertical cell array using TCAT(terabit cell array transistor) technology for ultra high density NAND flash memory,” in *Proc. Symp. VLSI Technol.*, Jun. 2009, pp. 192–193.

[5] J. Müller *et al.*, “Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories,” in *Proc.*

*IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, Dec. 2013, pp. 10.8.1–10.8.4.

[6] E. Yurchuk *et al.*, “HfO2-based ferroelectric field-effect transistors with 260 nm channel length and long data retention,” in *Proc. 4th IEEE Int. Memory Workshop (IMW)*, May 2012, pp. 1–4.

[7] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger,“Ferroelectricity in hafnium oxide thin films,” *Appl. Phys. Lett.*, vol. 99, no. 10, p. 102903, 2011.

[8] A. Kerber *et al.*, “Characterization of the VT-instability in SiO2/HfO2 gate dielectrics,” in *Proc. 41st Annu. IEEE Int. Rel. Phys. Symp.*, Dallas, TX, USA, Mar./Apr. 2003, pp. 41–45.

[9] G. Bersuker *et al.*, “Mechanism of electron trapping and characteristics of traps in HfO2 gate stacks,” *IEEE Trans. Device Mater. Rel.*, vol. 7, no. 1, pp. 138–145, Mar. 2007.

[10] G. Bersuker *et al.*, “Effect of pre-existing defects on reliability assess-ment of high-*k* gate dielectrics,” *Microelectron. Eng.*, vol. 44, nos. 9–11, pp. 1509–1512, 2004.

[11] J. Robertson, “High dielectric constant gate oxides for metal oxide Si transistors,” *Rep. Prog. Phys.*, vol. 69, no. 2, pp. 327–396, Dec. 2006. [12] Y. P. Feng, A. T. L. Lim, and M. F. Li, “Negative-*U* property of oxygen vacancy in cubic HfO2,” *Appl. Phys. Lett.*, vol. 87, no. 6, p. 062105, 2005.

[13] W.-T. Lu *et al.*, “The characteristics of hole trapping in HfO2/SiO2 gate dielectrics with TiN gate electrode,” *Appl. Phys. Lett.*, vol. 85, no. 16, pp. 3525–3527, 2004.

[14] G. Bersuker *et al.*, “Interfacial layer-induced mobility degradation in high-*k* transistors,” *Jpn. J. Appl. Phys.*, vol. 43, no. 11B, pp. 7899–7902, 2004.

[15] C. D. Young *et al.*, “Charge trapping and device performance degra-dation in MOCVD hafnium-based gate dielectric stack structures,” in *Proc. 42nd Annu. IEEE Int. Rel. Phys. Symp.*, Apr. 2004, pp. 597–598. [16] C. D. Young *et al.*, “Interfacial layer dependence of HFSI*x*O*y* gate stacks on VT instability and charge trapping using ultra-short pulse in characterization,” in *Proc. 43rd Annu. IEEE Int. Rel. Phys. Symp.*, Apr. 2005, pp. 75–79.

[17] G. Ribes *et al.*, “Review on high-*k* dielectrics reliability issues,” *IEEE*  *Trans. Device Mater. Rel.*, vol. 5, no. 1, pp. 5–19, Mar. 2005.

[18] R. Degraeve *et al.*, “Review of reliability issues in high-*k*/metal gate stacks,” in *Proc. 15th Int. Symp. Phys. Failure Anal. Integr. Cir-cuits (IPFA)*, Jul. 2008, pp. 1–6.

[19] K. Torii *et al.*, “Physical model of BTI, TDDB and SILC in HfO2-based high-*k* gate dielectrics,” in *IEDM Tech. Dig.*, Dec. 2004, pp. 129–132. [20] J. L. Gavartin, D. M. Ramo, A. L. Shluger, G. Bersuker, and B. H. Lee, “Negative oxygen vacancies in HfO2 as charge traps in high-*k* stacks,” *Appl. Phys. Lett.*, vol. 89, no. 8, p. 082908, 2006.

[21] N. A. Chowdhury and D. Misra, “Charge trapping at deep states in Hf–silicate based high-*k* gate dielectrics,” *J. Electrochem. Soc.*, vol. 154, no. 2, pp. G30–G37, 2007.

[22] A. Foster, F. L. Gejo, A. L. Shluger, and R. M. Nieminen, “Vacancy and interstitial defects in hafnia,” *Phys. Rev. B*, vol. 65, no. 17, p. 174117, May 2002.

[23] H. Takeuchi, H. Y. Wong, D. Ha, and T.-J. King, “Impact of oxygen vacancies on high-*k* gate stack engineering,” in *IEDM Tech. Dig.*, Dec. 2004, pp. 829–832.

[24] E. Yurchuk *et al.*, “Origin of the endurance degradation in the novel HfO2-based 1T ferroelectric non-volatile memories,” in *Proc.*

*IEEE Int. Rel. Phys. Symp. (IRPS)*, Waikoloa, HI, USA, Jun. 2014, pp. 2E.5.1–2E.5.5.

[25] C. D. Young, D. Heh, R.-N. Choi, B.-H. Lee, and G. Bersuker, “The pulsed I*d*-V*g* methodology and its application to the electron trapping characterization of high-*k* gate dielectrics,” *J. Semicond. Technol. Sci.*, vol. 10, no. 2, pp. 79–99, 2010.

[26] C. Leroux *et al.*, “Characterization and modeling of hysteresis phenom-ena in high *K* dielectrics,” in *IEDM Tech. Dig.*, Dec. 2004, pp. 737–740. [27] C. D. Young *et al.*, “Ultra-short pulse current–voltage characterization of the intrinsic characteristics of high-*k* devices,” *J. Appl. Phys.*, vol. 44,

Jun. 2012, pp. 25–26. no. 4S, pp. 2437–2440, 2005.

YURCHUK *et al.*: CHARGE-TRAPPING PHENOMENA IN HfO2-BASED FeFET-TYPE NONVOLATILE MEMORIES 3507

[28] D. Heh, C. D. Young, R. Choi, and G. Bersuker, “Extraction of the threshold-voltage shift by the single-pulse technique,” *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 734–736, Aug. 2007.

[29] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. Hoboken, NJ, USA: Wiley, 2006.

[30] A. Ortiz-Conde, F. J. G. Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, “A review of recent MOSFET threshold voltage extrac-tion methods,” *Microelectron. Rel.*, vol. 42, nos. 4–5, pp. 583–596,

[33] E. Yurchuk *et al.*, “Impact of scaling on the performance of HfO2-based ferroelectric field effect transistors,” *IEEE Trans. Electron Devices*, vol. 61, no. 11, pp. 3699–3706, Nov. 2014.

[34] A. Kerber and E. Cartier, “A fast four-point sense methodology for extraction of circuit-relevant degradation parameters,” *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 912–914, Sep. 2010.

[35] M. A. Alam, J. Bude, and A. Ghetti, “Field acceleration for oxide breakdown—Can an accurate anode hole injection model resolve the

Apr./May 2002. E vs. 1/E controversy?” presented at the 38th Annu. IEEE Int. Rel.

[31] E. Yurchuk *et al.*, “Impact of layer thickness on the ferroelectric behaviour of silicon doped hafnium oxide thin films,” *Thin Solid Films*, vol. 533, pp. 88–92, Apr. 2013.

[32] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger,“Ferroelectricity in hafnium oxide: CMOS compatible ferroelectric field effect transistors,” in *IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2011, pp. 24.5.1–24.5.4.

Phys. Symp., San Jose, CA, USA, Apr. 2000, pp. 21–26.

Authors’ photographs and biographies not available at the time of publication.