Lab 02 - First Verilog

In this lab, you've learned how to do an initial and simple design in Verilog to learn the Vivado tooling and process involved in RTL/FPGA design.

Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Lab Summary

In this lab we learned the basics of Verilog, running our first simulation and program on a Basys3 board. Our first task was to write a basic simulation program to turn on LEDs when certain switches were activated. We then simulated this program in Verilog verifying our code was correct. After that, the Basys3 board was hooked up to our laptops and the program was ran successfully on the board.

Lab Questions

1 - Describe the stages of building a Verilog project in Vivado.

Step 1: create a new project
Step 2: add Verilog files
Step 3: write the code for the Verilog file
Step 4: add constraints
Step 5: load the correct board
Step 6: under Simulation select Run Simulation, select behavioral simulation
Step 7: generate bitstream
Step 8: open hardware manager
Step 9: select open target and auto connect
Step 10: plug in the correct board

2 - What is the value in looking at the elaborated design schematic?

Looking at the elaborated design schematic is a good way to perform a sanity check. It checks to see if the code is interpreted correctly, helps in debugging and validation, and gives resource awareness.

3 - Why should we simulate our designs frequently? What does the simulation do?

We simulate our designs frequently to catch bugs, verify design intent, and save time in development. Simulation is often the fastest and safest way to verify our Verilog design. The simulation executes our code, generates waveforms, and runs testbenches.

Code Submission

https://github.com/HenrikAckler/ece230L