

HIGH-PERFORMANCE, LOW-CURRENT SIGFOX™ GATEWAY

Features

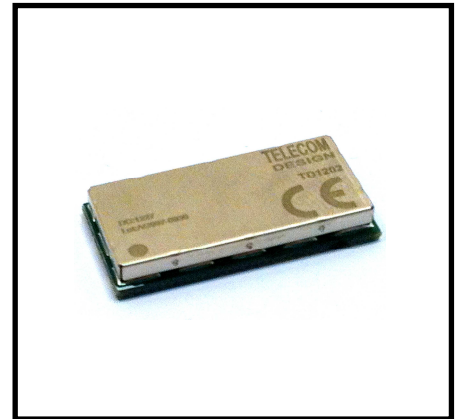
- SIGFOX™ certified
- Frequency range = ISM 868 MHz
- Receive sensitivity = -126 dBm
- Modulation
 - (G)FSK, 4(G)FSK, GMSK
 - OOK
- Max output power
 - +14 dBm
- Low active radio power consumption
 - 13/16 mA RX
 - 37 mA TX @ +10 dBm
- Power supply = 2.3 to 3.3 V
- LGA25 (25.4x12.7x3.81mm) Land Grid Array package
- Available in several conditioning methods

Applications

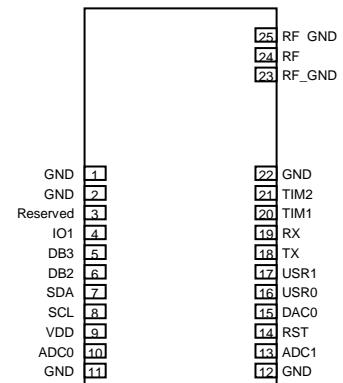
- SIGFOX™ transceiver (fully certified)
- Sensor network
- Health monitors
- Remote control
- Home security and alarm
- Telemetry
- Industrial control

Description

Telecom Design's TD1202 devices are high performance, low current SIGFOX™ gateways. The combination of a powerful radio transceiver and a state-of-the-art ARM Cortex M3 baseband processor achieves extremely high performance while maintaining ultra-low active and standby current consumption. The TD1202 device offers an outstanding RF sensitivity of –126 dBm while providing an exceptional output power of up to +14 dBm with unmatched TX efficiency. The TD1202 device versatility provides the gateway function from a local Narrow Band ISM network to the long-distance Ultra Narrow Band SIGFOX™ network at no additional cost. The broad range of analog and digital interfaces available in the TD1202 module allows any application to interconnect easily to the SIGFOX™ network. The LVTTTL low-energy UART, the I²C bus, the multiple timers with pulse count input/PWM output capabilities, the 2 high-resolution/high-speed ADCs and single DAC, along with the numerous GPIOs can control any kind of external sensors or activators. Featuring an AES encryption engine and a DMA controller, the powerful 32-bit ARM Cortex-M3 baseband processor can implement highly complex and secure protocols in an efficient environmental and very low consumption way.



Pin Assignments



Patents pending

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Functional Block Diagram

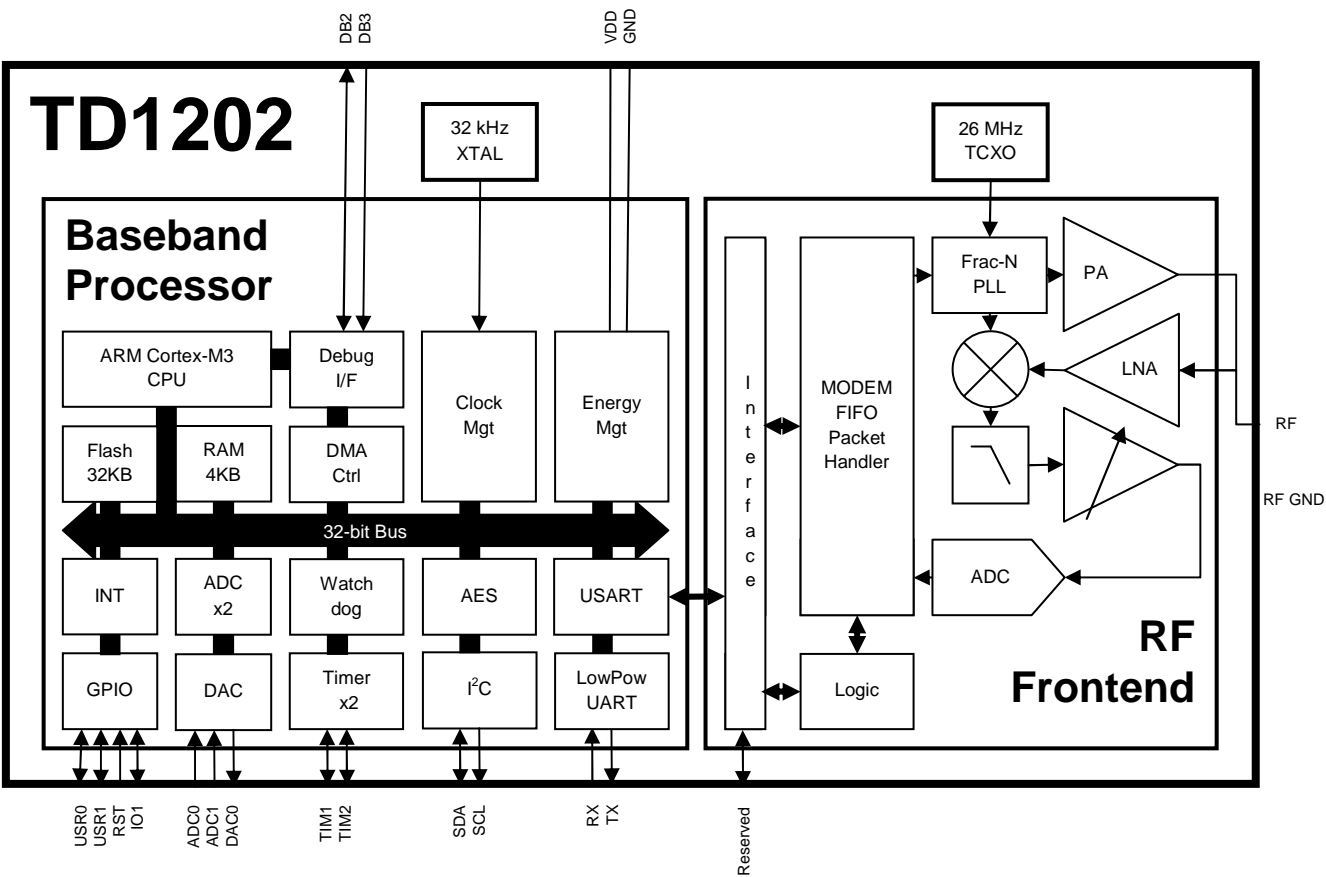


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1 Electrical Specifications

Table 1. Absolute Maximum Ratings

Parameter	Value	Units
V_{DD} to GND	0 to +3.3	V
Instantaneous $V_{RF-peak}$ to GND on RF Pin	-0.3 to +8.0	V
Sustained $V_{RF-peak}$ to GND on RF Pin	-0.3 to +6.5	V
Voltage on Digital Inputs	0 to V_{DD}	V
Voltage on Analog Inputs	0 to V_{DD}	V
RX Input Power	+10	dBm
Operating Ambient Temperature Range T_A	-30 to +75	°C
Storage Temperature Range T_{STG}	-40 to +125	°C
Maximum soldering Temperature	260	°C
Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Power Amplifier may be damaged if switched on without proper load or termination connected. TX matching network design will influence TX $V_{RF-peak}$ on RF pin. Caution: ESD sensitive device.		

Table 2- DC Power Supply Characteristics¹

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Range ²	V _{DD}		2.3	3.0	3.3	V
Power Saving Mode	I _{Sleep}	Sleep current using the 32 kHz crystal	1.0	1.6	6.0	μA
Active CPU Mode	I _{Active}	CPU performing active loop @ 14 MHz	2.55	3.0	3.45	mA
Active CPU Mode + RX Mode Current ²	I _{RX}		—	13	16	mA
Active CPU Mode + TX Mode Current ²	I _{TX +14}	+14 dBm output power, 868 MHz, 3.3 V	—	49	—	mA
	I _{TX +10}	+10 dBm output power, 868 MHz, 3.3 V	—	37	—	mA

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section in “1.1. Definition of Test Conditions” on page 5.
2. Guaranteed by qualification. Qualification test conditions are listed in the “Qualification Test Conditions” section in “1.1. Definition of Test Conditions” on page 5.

Table 3. Transmitter RF Characteristics¹

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TX Frequency Range ²	F _{TX}		868.0	—	869.7	MHz
Modulation Deviation Range ³	Δf	868.0-869.7 MHz	—	1.5	—	MHz
Modulation Deviation Resolution ³	F _{RES}	868.0-869.7 MHz	—	28.6	—	Hz
Frequency Error ²	F _{ERR_25}	868.0-869.7 MHz, 25°C, 3.3 V	—	±2	—	kHz
	F _{ERR_M20}	868.0-869.7 MHz, -20°C, 3.3 V	—	±3	—	kHz
	F _{ERR_55}	868.0-869.7 MHz, 55°C, 3.3 V	—	±3	—	kHz
Average Conducted Power ²	P _{AVCDP1}	-20°C to 55°C, 868.0 MHz to 868.6 MHz, 3.3 V	—	—	14	dBm
	P _{AVCDP2}	-20°C to 55°C, 868.6 MHz to 868.7 MHz, 3.3 V	—	—	10	dBm
	P _{AVCDP3}	-20°C to 55°C, 868.7 MHz to 869.2 MHz, 3.3 V	—	—	14	dBm
	P _{AVCDP4}	-20°C to 55°C, 869.2 MHz to 869.25 MHz, 3.3 V	—	—	10	dBm
	P _{AVCDP5}	-20°C to 55°C, 869.25 MHz to 869.3 MHz, 3.3 V	—	—	10	dBm
	P _{AVCDP6}	-20°C to 55°C, 869.3 MHz to 869.4 MHz, 3.3 V	—	—	10	dBm
	P _{AVCDP7}	-20°C to 55°C, 869.65 MHz to 869.7 MHz, 3.3 V	—	—	14	dBm
Transient Power ²	P _{TP}	868.0-869.7 MHz, 25°C, 3.3 V, 4800 bps, deviation 2500 Hz, cable loss 0.2 dB, antenna gain 2 dBi	—	—	3	dB
Adjacent Channel Power ²	P _{ACP_25}	868.0-869.7 MHz, 25°C, 3.3 V, 4800 bps, deviation 2500 Hz, cable loss 0.2 dB, antenna gain 2 dBi	—	-50	—	dBm
	P _{ACP_M20}	868.0-869.7 MHz, -20°C, 3.3 V, 4800 bps, deviation 2500 Hz, cable loss 0.2 dB, antenna gain 2 dBi	—	-51	—	dBm
	P _{ACP_55}	868.0-869.7 MHz, 55°C, 3.3 V, 4800 bps, deviation 2500 Hz, cable loss 0.2 dB, antenna gain 2 dBi	—	-50	—	dBm
Spurious Emissions ²	P _{OB_TX1}	Frequencies < 30 MHz, 868.0-869.7 MHz, 25°C, 3.3 V, 4800 bps, deviation 2500 Hz, cable loss 0.2 dB, antenna gain 2 dBi	—	-82	—	dBm
	P _{OB_TX2}	Frequencies < 1 GHz, 868.0-869.7 MHz, 25°C, 3.3 V, 4800 bps, deviation 2500 Hz, cable loss 0.2 dB, antenna gain 2 dBi	—	-58	—	dBm
	P _{OB_TX3}	Frequencies > 1 GHz, 868.0-869.7 MHz, 25°C, 3.3 V, 4800 bps, deviation 2500 Hz, cable loss 0.2 dB, antenna gain 2 dBi	—	-37	—	dBm

Notes:

3. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section of “1.1. Definition of Test Conditions” on page 5.
4. Guaranteed by qualification. Qualification test conditions are listed in the “Qualification Test Conditions” section in “1.1. Definition of Test Conditions” on page 5.
5. Guaranteed by component specification.

Table 4. Receiver RF Characteristics¹

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RX Frequency Range ²	F _{RX}		868.0	—	869.7	MHz
Synthesizer Frequency Resolution ³	F _{RES}	868.0-869.7 MHz	—	28.6	—	Hz
Blocking ²	2M _{BLOCK}	Frequency offset ± 2 MHz, 868.0-869.7 MHz, 25°C, 3.3 V	—	38	—	dB
	10M _{BLOCK}	Frequency offset ± 10 MHz, 868.0-869.7 MHz, 25°C, 3.3 V	—	62	—	dB
Spurious Emissions ²	P _{OB_RX1}	From 9 kHz to 1 GHz, 868.0-869.7 MHz, 25°C, 3.3 V	—	-84	—	dBm
	P _{OB_RX2}	From 1 GHz to 6 GHz, 868.0-869.7 MHz, 25°C, 3.3 V	—	-70	—	dBm
RX Sensitivity ³	P _{RX_0.5}	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, $\Delta f = \pm 250$ Hz)	—	-126	—	dBm
	P _{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, $\Delta f = \pm 20$ kHz)	—	-110	—	dBm
	P _{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, $\Delta f = \pm 50$ kHz)	—	-106	—	dBm
	P _{RX_125}	(BER < 0.1%) (125 kbps, GFSK, BT = 0.5, $\Delta f = \pm 62.5$ kHz)	—	-105	—	dBm
	P _{RX_500}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, $\Delta f = \pm 250$ kHz)	—	-97	—	dBm
	P _{RX_9.6}	(BER < 0.1%) (9.6 kbps, GFSK, BT = 0.5, $\Delta f = \pm 2.4$ kHz)	—	-110	—	dBm
	P _{RX_1M}	(BER < 0.1%) (1 Mbps, GFSK, BT = 0.5, $\Delta f = \pm 1.25$ kHz)	—	-88	—	dBm
	P _{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)	—	-109	—	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)	—	-104	—	dB
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)	—	-99	—	dBm
RSSI Resolution ³	RES _{RSSI}		—	± 0.5	—	dB

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section of "1.1. Definition of Test Conditions" on page 5.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions" section in "1.1. Definition of Test Conditions" on page 5.
3. Guaranteed by component specification.

Table 5. All Digital I/O (except DB1) DC & AC Characteristics¹

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Low Voltage ²	V _{IOIL}		—	—	0.3V _{DD}	V
Input High Voltage ²	V _{IOIH}		0.7V _{DD}	—	—	V
Output High Voltage ²	V _{IOOH}	Sourcing 6 mA, VDD = 3.0V, Standard Drive Strength	0.95V _{DD}	—	—	V
		Sourcing 20 mA, VDD = 3.0V, High Drive Strength	0.9V _{DD}	—	—	V
Output Low Voltage ²	V _{IOOL}	Sinking 6 mA, VDD=3.0V, Standard Drive Strength	—	—	0.05V _{DD}	V
		Sinking 20 mA, VDD=3.0V, High Drive Strength	—	—	0.1V _{DD}	V
Input Leakage Current ²	I _{IOLEAK}	High Impedance I/O connected to GND or V _{DD}	—	—	±25	nA
I/O Pin Pull-Up Resistor ²	R _{PU}		—	40	—	kΩ
I/O Pin Pull-Down Resistor ²	R _{PD}		—	40	—	kΩ
Internal ESD Series Resistor ²	R _{IOESD}		—	200	—	Ω
Pulse Width of Pulses to be Removed by the Glitch Suppression Filter ²	t _{IOGLITCH}		10	—	50	ns
Output Fall Time ²	t _{IOOF}	0.5 mA Drive Strength and Load Capacitance C _L = 12.5 to 25 pF	20+0.1C _L	—	250	ns
		2 mA Drive Strength and Load Capacitance C _L = 350 to 600 pF	20+0.1C _L	—	250	ns
I/O Pin Hysteresis (V _{IOTHR+} - V _{IOTHR-}) ²	V _{IOHYST}	V _{DD} = 2.3 to 3.3 V	0.1V _{DD}	—	—	V

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section of “1.1. Definition of Test Conditions” on page 5.
2. Guaranteed by component specification.

Table 6. DB1 Digital I/O DC & AC Characteristics¹

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Low Voltage ²	V_{DB1IL}		—	—	$0.3V_{DD}$	V
Input High Voltage ²	V_{DB1IH}		$0.7V_{DD}$	—	—	V
Output High Voltage ²	V_{DB1OH}	Sourcing 7.4 mA, $V_{DD} = 3.3V$, Drive Strength = HL	$0.8V_{DD}$	—	—	V
Output Low Voltage ²	V_{DB1OL}	Sinking 8.5 mA, $V_{DD} = 3.3V$, Drive Strength = HL	—	—	$0.2V_{DD}$	V
Input Leakage Current ²	$I_{DB1LEAK}$	High Impedance I/O connected to GND or V_{DD}	—	—	± 10	μA
Input Capacitance ²	C_{DB1IN}		—	2	—	pF
Output Rise Time ²	t_{DB1OR}	$0.1V_{DD}$ to $0.9V_{DD}$, $C_L = 10$ pF, Drive Strength = HH	—	2.3	—	ns
Output Fall Time ²	t_{DB1OF}	$0.9V_{DD}$ to $0.1V_{DD}$, $C_L = 10$ pF, Drive Strength = HH	—	2	—	ns
Notes:						
1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section of “1.1. Definition of Test Conditions” on page 5.						
2. Guaranteed by component specification.						

Table 7. ADC DC & AC Characteristics¹

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range ²	V_{ADCIN}	Single Ended	0	—	V_{REF}	V
		Differential	$-V_{REF}/2$	—	$V_{REF}/2$	V
Common Mode Input Range ²	$V_{ADCCMIN}$		0	—	V_{DD}	V
Input Current ²	I_{ADCIN}	2 pF Sampling Capacitors	—	<100	—	nA
Analog Input Common Mode Rejection Ratio ²	$CMRR_{ADC}$		—	65	—	dB
Average Active Current ²	I_{ADC}	10 ksps/s 12 bit, Internal 1.25 V Reference, Warmup Mode = 0	—	67	—	μ A
		10 ksps/s 12 bit, Internal 1.25 V Reference, Warmup Mode = 1	—	63	—	μ A
		10 ksps/s 12 bit, Internal 1.25 V Reference, Warmup Mode = 2	—	64	—	μ A
Current Consumption of Internal Voltage Reference ²	I_{ADCREf}		—	65	—	μ A
Input Capacitance ²	C_{ADCIN}		—	2	—	pF
Input ON Resistance ²	R_{ADCIN}		1	—	—	M Ω
Input RC Filter Resistance ²	$R_{ADCFILT}$		—	10	—	k Ω
Input RC Filter/Decoupling Capacitance ²	$C_{ADCFILT}$		—	250	—	fF
ADC Clock Frequency ²	f_{ADCCLK}		—	—	13	MHz
Conversion Time ²	$t_{ADCCONV}$	6 bit	7	—	—	ADC CLK Cycles
		10 bit	11	—	—	ADC CLK Cycles
		12 bit	13	—	—	ADC CLK Cycles
Acquisition Time ²	t_{ADCACQ}	Programmable	1	—	256	ADC CLK Cycles
Required Acquisition Time for $V_{DD}/3$ Reference ²	$t_{ADCACQVDD3}$		2	—	—	μ s

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section of “1.1. Definition of Test Conditions” on page 5.
2. Guaranteed by component specification.

Table 7. ADC DC & AC Characteristics¹ (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Startup Time of Reference Generator and ADC Core in NORMAL Mode ²	t_{ADCSTART}		—	5	—	μs
Startup Time of Reference Generator and ADC Core in KEEPADCWARM Mode ²			—	1	—	μs
Offset Voltage ²	$V_{\text{ADCOFFSET}}$	After calibration, single ended	—	0.3	—	mV
		After calibration, differential	—	0.3	—	mV
Thermometer Output Gradient ²	$T_{\text{GRAD}}_{\text{ADCTH}}$		—	-1.92	—	mV/°C
			—	-6.3	—	ADC Codes / °C
Differential Non-Linearity (DNL) ²	DNL_{ADC}		—	± 0.7	—	LSB
Integral Non-Linearity (INL), End Point Method ²	INL_{ADC}		—	± 1.2	—	LSB
No Missing Codes ²	MC_{ADC}		11.999 ³	12	—	bits
Gain Error Drift ²	GAIN_{ED}	1.25V Reference	—	0.01 ⁴	0.033 ⁵	%/°C
		2.25V Reference	—	0.01 ⁴	0.03 ⁵	%/°C
		1.25V Reference	—	0.2 ⁴	0.07 ⁵	LSB/°C
		2.25V Reference	—	0.2 ⁴	0.62 ⁵	LSB/°C

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the “Production Test Conditions” section of “1.1. Definition of Test Conditions” on page 5.
2. Guaranteed by component specification.
3. On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbor codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.
4. Typical numbers given by $\text{abs}(\text{Mean}) / (85 - 25)$.
5. Max number given by $(\text{abs}(\text{Mean}) + 3 \times \text{stddev}) / (85 - 25)$.

Table 8. DAC DC & AC Characteristics¹

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage Range ²	V_{DACOUT}	V_{DD} voltage reference, Single Ended	0	—	V_{DD}	V
Output Common Mode Voltage Range ²	V_{DACCM}		0	—	V_{DD}	V
Active Current Including References for 2 Channels ²	I_{DAC}	500 ksps/s 12 bit	—	400	—	μA
		500 ksps/s 12 bit	—	200	—	μA
		100 ksps/s 12 bit NORMAL	—	38	—	μA
Sample Rate ²	SR_{DAC}		—	—	500	ksps
DAC Clock Frequency ²	f_{DAC}	Continuous Mode	—	—	1000	kHz
		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
Clock Cycles per Conversion ²	$CYC_{DACCONV}$		—	2	—	DAC CLK Cycles
Conversion Time ²	$t_{DACCONV}$		2	—	—	μs
Settling Time ²	$t_{DACSETTLE}$		—	5	—	μs
Signal to Noise Ratio (SNR) ²	SNR_{DAC}	500 ksps, 12 bit, single ended, internal 1.25V reference	—	58	—	dB
		500 ksps, 12 bit, single ended, internal 2.5V reference	—	59	—	dB
Signal to Noise-Pulse Distortion Ratio (SNDR) ²	$SNDR_{DAC}$	500 ksps, 12 bit, single ended, internal 1.25V reference	—	57	—	dB
		500 ksps, 12 bit, single ended, internal 2.5V reference	—	54	—	dB
Spurious-Free Dynamic Range(SFDR) ²	$SFDR_{DAC}$	500 ksps, 12 bit, single ended, internal 1.25V reference	—	62	—	dB
		500 ksps, 12 bit, single ended, internal 2.5V reference	—	56	—	dB
Offset Voltage ²	$V_{DACOFFSET}$	After calibration, single ended	—	2	—	mV
Differential Non-Linearity ²	DNL_{DAC}		—	± 1	—	LSB
Integral Non-Linearity ²	INL_{DAC}		—	± 5	—	LSB
No Missing Codes ²	MC_{DAC}		—	12	—	bits

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions" section of "1.1. Definition of Test Conditions" on page 5.
2. Guaranteed by component specification.

1.1 Definition of Test Conditions

1.1.1 Production Test Conditions:

- $T_A = + 25^{\circ}\text{C}$
- $V_{DD} = +3.3 \text{ VDC}$
- Production test schematics (unless noted otherwise)
- All RF input and output levels referred to the pins of the TD1202 module

1.1.2 Qualification Test Conditions:

- $T_A = -30 \text{ to } +75^{\circ}\text{C}$ (Typical $T_A = 25^{\circ}\text{C}$)
- $V_{DD} = +2.3 \text{ to } 3.3 \text{ VDC}$ (Typical $V_{DD} = 3.0 \text{ VDC}$)
- Using TX/RX Split Antenna reference design or production test schematic
- All RF input and output levels referred to the pins of the TD1202 module

2 Functional Description

The TD1202 devices are high-performance, low-current, wireless SIGFOX™ gateways. The wide operating voltage range of 2.3–3.3 V and low current consumption make the TD1202 an ideal solution for battery powered applications. The TD1202 operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion mixer to downconvert the 2-level FSK/GFSK or OOK/ASK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance $\Delta\Sigma$ ADC allowing filtering, demodulation, slicing, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is output to the baseband CPU by reading the 64-byte RX FIFO.

A single high precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO is generated by an integrated VCO and $\Delta\Sigma$ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates from 0.123 kbps to 1 Mbps. The TD1202 operates in the frequency bands of 868.0–869.7 MHz with a maximum frequency accuracy step size of 28.6 Hz. The transmit FSK data is modulated directly into the $\Delta\Sigma$ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The power amplifier (PA) supports output power up to +14 dBm with very high efficiency, consuming only 37 mA at +10 dBm. The integrated power amplifier can also be used to compensate for the reduced performance of a lower cost, lower performance antenna or antenna with size constraints due to a small form-factor. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. A highly configurable packet handler allows for autonomous encoding/decoding of nearly any packet structure.

As both the local Narrow Band ISM network and the long-distance Ultra Narrow Band SIGFOX™ network can be addressed seamlessly, the TD1202 device provides a natural gateway function at no additional cost. Thus, the same TD1202 module can be used both for local RF communication with peer modules, and also connect to the wide-area SIGFOX™ RF network.

The broad range of analog and digital interfaces available in the TD1202 module allows any application to interconnect easily to the SIGFOX™ network. The LVTTTL low-energy UART, the I²C bus, the multiple timers with pulse count input/PWM output capabilities, the 2 high-resolution/high-speed ADCs and single DAC, along with the numerous GPIOs can control any kind of external sensors or activators. Featuring an AES encryption engine and a DMA controller, the powerful 32-bit ARM Cortex-M3 baseband processor can implement highly complex and secure protocols in an efficient environmental and very low consumption way. This unique combination of a powerful 32-bit ARM Cortex-M3 CPU including innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of intelligent peripherals allows any application to connect to the SIGFOX™ network.

The application shown in Figure 1 shows the minimum interconnection required to operate the TD1202 module.

Basically, only the 5 GND, 2 RF_GND, V_{DD}, TX, RX and RF antenna pin connections are necessary. The RST (reset) pin connection is not mandatory and this pin can be left floating if not used.

A 10 μ F/6.3V decoupling capacitor must be added as close as possible to the V_{DD} pin.

The TX/RX pins are LVTTTL-compatible and feature internal pull-up resistors.

A 50 Ω matched RF antenna must be connected to the RF pin.

The connection of a super-blue LED with series current-limiting resistor of 220 Ω on pin TIM2 is recommended in order to display the bootloader status at boot time.

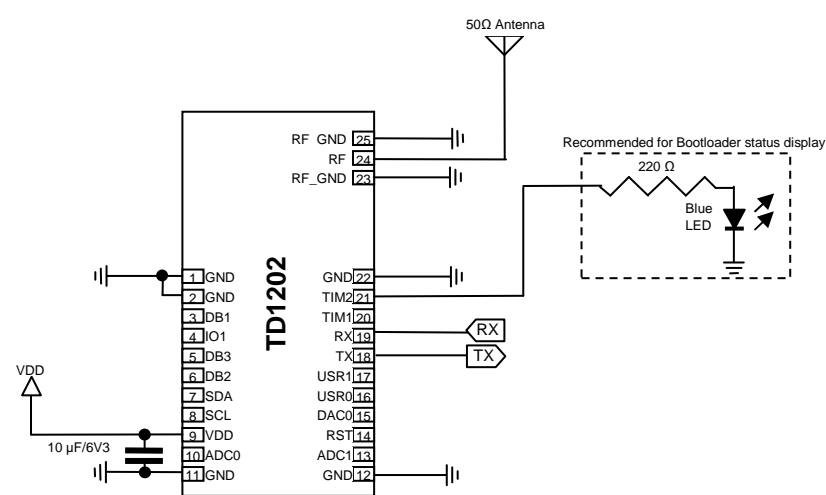


Figure 1. Typical Application

3 Module Interface

3.1 Low-Power UART (Universal Asynchronous Receiver/Transmitter)

The TD1202 communicates with the host MCU over a standard asynchronous serial interface consisting of only 2 pins: TX and RX. The TX pin is used to send data from the TD1202 module to the host MCU, and the RX pin is used to receive data into the TD1202 module coming from the host MCU.

This interface allows two-way UART communication to be performed in low energy modes, using only a few μA during active communication and only 150 nA when waiting for incoming data.

This serial interface is designed to operate using the following serial protocol parameters:

- LVTTTL electrical level
- 9600 bps
- 8 data bits
- 1 stop bit
- No parity
- No hardware/software flow control

This interface operates using LVTTTL signal levels to satisfy the common interface to a low power host MCU. If an EIA RS232-compliant interface voltage level is required, an RS232 level translator circuit must be used. It is also possible to use a common USB/UART interface chip to connect to an USB bus.

Over this serial interface, the TD1202 device provides a standard Hayes “AT” command set used to control the module using ASCII readable commands and get answers, as well as to send or receive data.

The list of available commands with their corresponding arguments and return values, a description of their operation and some examples are detailed into the “*TD1202 Reference Manual*”.

3.2 I²C bus

As a convenience, the TD1202 module is equipped with a popular I²C serial bus controller that enables communication with a number of external devices using only two I/O pins: SCL and SDA. The SCL pin is used to interface with the I²C clock signal, and the SDA pin to the I²C data signal, respectively. When not used for I²C bus, these 2 pins can be configured to perform other functions using “AT” configuration commands, please refer to the “*TD1202 Reference Manual*” for details.

The TD1202 module is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode (Sm), fast-mode (Fm) and fast-mode plus (Fm+) speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. Both 7-bit and 10-bit addresses are supported, along with extensive error handling capabilities (clock low/high timeouts, arbitration lost, bus error detection).

The operation of this interface is controlled by the mean of Hayes “AT” commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the “*TD1202 Reference Manual*”.

3.3 Timer/Counter

The TD1202 provides an interface to an integrated timer/counter using the TIM1 and TIM2 pins. Each individual pin can be configured independently as either a capture input or a compare/PWM output to the 16-bit internal timer/counter. When not used for timer/counter operation, these 2 pins can be configured to perform other functions using “AT” configuration commands, please refer to the “*TD1202 Reference Manual*” for details.

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The timer consists in a counter that can be configured to up-count, down-count, up/down-count (continuous or one-shot) or perform as a quadrature decoder if using both TIM1 and TIM2 as inputs with signals that are 90° out of phase.

The timer also contains 2 output channels, that can be configured as either an output compare or single/double slope PWM (Pulse-Width Modulation) outputs routed to the TIM1 and TIM2 pins.

The operation of this interface is controlled by the mean of Hayes “AT” commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the “TD1202 Reference Manual”.

3.4 ADC (Analog to Digital Converter)

The TD1202 provides an interface to an integrated low-power SAR (Successive Approximation Register) ADC, capable of a resolution of up to 12 bits at up to 1 Msps or 6 bits at up to 1.86 Msps. The ADC0 and ADC1 pins provide the external interface to the ADC. When not used for ADC operation, these 2 pins can be configured to perform other functions using “AT” configuration commands, please refer to the “TD1202 Reference Manual” for details.

Along with these 2 ADC0 and ADC1 analog input channels, the ADC also provides an internal temperature, VDD, and GND input channel that may be used to get a digital representation of analog temperature or voltage values. It is also possible to loopback the analog output of the integrated DAC (see section 3.5, “DAC (Digital to Analog Converter)”).

The internal ADC provides an optional input filter consisting of an internal low-pass RC filter or simple internal decoupling capacitor. The resistance and capacitance values are given in the electrical characteristics for the device, named R_{ADCFILT} and C_{ADCFILT} respectively.

The reference voltage used by the ADC can be selected from several sources, including a 1.25 V internal bandgap, a 2.5 V internal bandgap, V_{DD} , a 5 V internal differential bandgap or unbuffered $2V_{\text{DD}}$.

Additionally, to achieve higher accuracy, hardware oversampling can be enabled. With oversampling, each selected input is sampled a number of times, and the results are filtered by a first order accumulate and dump filter to form the end result. Using 16x oversampling minimum, it is thus possible to achieve result resolution of up to 16 bits.

The operation of this interface is controlled by the mean of Hayes “AT” commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the “TD1202 Reference Manual”.

3.5 DAC (Digital to Analog Converter)

The TD1202 provides an interface to an integrated DAC that can convert a digital value to a fully rail-to-rail analog output voltage with 12-bit resolution at up to 500 ksps. The DAC may be used for a number of different applications such as sensor interfaces or sound output. The analog DAC output is routed to the DAC0 pin. When not used for ADC operation, this pin can be configured to perform other functions using “AT” configuration commands, please refer to the “TD1202 Reference Manual” for details.

The reference voltage used by the DAC can be selected from several sources, including a 1.25 V internal bandgap, a 2.5 V internal bandgap, or V_{DD} .

The internal DAC provides support for offset and gain calibration, and contains an automatic sine generation mode as well as a loopback output to the ADC (see section 3.4, “ADC (Analog to Digital Converter)”).

3.6 GPIO (General Purpose Input/Output)

Apart from the TX and RX UART pins, and the RF pins, all signal pins are available as general-purpose inputs/outputs. This includes of course the generic USR0, USR1, DB1 and IO1 pins, but also the ADC0, ADC1,

DAC0, SCL, SDA, DB2, DB3 pins when not used for their main function. This configuration can be performed using “AT” commands, please refer to the “TD1202 Reference Manual” for details.

All the USR0, USR1, IO1, ADC0, ADC1, DAC0, SCL, SDA, DB2, DB3 (i.e. not including DB1) pins can be configured individually as tristate (default reset state), push-pull, open-drain, with/without pull-up or pull-down resistor, and with a programmable drive strength (0.5 mA/2 mA/6 mA/20 mA).

When configured as inputs, these pins feature an optional glitch suppression filter and full (rising, falling or both edges) interrupt with wake-up from low-power mode capabilities. Of course, the pin configuration is retained even when using these low-power modes.

As it is internally connected to the RF frontend, the DB1 does not feature interrupt capabilities, and the alternate functions available on this pin are more related to RF, please refer to the “TD1202 Reference Manual” for details.

The operation of the GPIOs is controlled by the mean of Hayes “AT” commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the “TD1202 Reference Manual”.

3.7 RST (Reset)

The TD1202 module features an active-low RST pin. This pin is held high by an internal pull-up resistor, so when not used, this pin can be left floating.

3.8 Debug

The TD1202 module devices include hardware debug support through a 2-pin serial-wire debug interface. The 2 pins DB2 and DB3 are used for this purpose. The DB2 pin is the ARM Cortex-M3's SWDIO Serial Wire data Input/Output. This pin is enabled after a reset and has a built in pull-up. The DB3 pin is the ARM Cortex-M3's SWCLK Serial Wire Clock input. This pin is enabled after reset and has a built-in pull down. When not used for debug operation, these 2 pins can be configured to perform other functions using “AT” configuration commands, please refer to the “TD1202 Reference Manual” for details.

Although the ARM Cortex-M3 supports advanced debugging features, the TD1202 devices only use two port pins for debugging or programming. The systems internal and external state can be examined with debug extensions supporting instruction or data access break- and watch points.

For more information on how to enable the debug pin outputs/inputs the reader is referred to Section 28.3.4.1 (p. 457), the ARM Cortex-M3 Technical Reference Manual and the ARM CoreSight™ Technical Reference Manual.

3.9 RF Antenna

The TD102 support a single-ended RF pin with 50 Ω characteristic impedance for connecting a matched-impedance external antenna. This pin is physically surrounded by 2 RF GND pins for better noise immunity.

3.10 VDD & GND

The TD1202 provides 5 GND pins and 2 RF_GND pins: all of them must be connected to a good ground plane.

A 10 μ F/6.3 V decoupling capacitor should be placed as closed as possible to the single VDD pin.

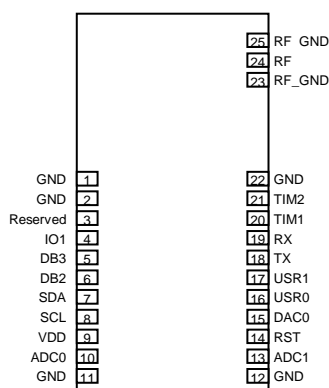
4 Bootloader

The TD1202 module contains an integrated bootloader which allows reflashing the module firmware either over the RX/TX UART connection, or over the air using the built-in RF transceiver.

The bootloader is automatically activated upon module reset. Once activated, the bootloader will monitor the UART/RF activity for a 200 ms period, and detect an incoming update condition.

If the update condition is met, the TD1202 will automatically proceed to flash the new firmware with safe retry mechanisms, or falls back to normal operation.

5 Pin Descriptions



Pin	Pin Name	I/O	Description
1	GND	GND	Connect to PCB ground
2	GND	GND	Connect to PCB ground
3	Reserved	I/O	Reserved pin – Do not connect
4	IO1	I/O	General Purpose Low-Power Digital I/O This pin may be configured to perform various functions.
5	DB3	I	SWDCLK (SWD Clock) Signal This signal provides the SWD clock signal to the integrated TD1202 ARM® CPU. This pin may be configured to perform various functions.
6	DB2	I/O	SWDIO (SWD Data I/O) Signal This signal provides the SWD programming/debugging signal interface to the integrated TD1202 ARM® CPU. This pin may be configured to perform various functions.
7	SDA	I/O	General Purpose Low-Power Digital I/O This pin may be configured to perform various functions, including the I ² C DATA (SDA) function.
8	SCL	I/O	General Purpose Low-Power Digital I/O This pin may be configured to perform various functions, including the I ² C clock (SCL) function.
9	VDD	VDD	+2.3 to +3.3 V Supply Voltage Input The recommended VDD supply voltage is +3.0V. Connect a 10 µF capacitor as close as possible to this input.
10	ADC0	I/O	General Purpose Low-Power Digital I/O This pin may be configured to perform various functions, including the ADC analog input #0 function.
11	GND	GND	Connect to PCB ground
12	GND	GND	Connect to PCB ground
13	ADC1	I/O	General Purpose Low-Power Digital I/O This pin may be configured to perform various functions, including the ADC analog input #1 function.
14	RST	I	Active Low RESET input signal This signal resets the TD1202 module to its initial state. If not used, this signal can be left floating, as it is internally pulled up by an integrated resistor.
15	DAC0	I/O	General Purpose Low-Power Digital I/O This pin may be configured to perform various functions, including the DAC analog output #0 function.

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16	USR0	I/O	General Purpose Low-Power Digital I/O This pin may be configured to perform various functions.
17	USR1	I/O	General Purpose Low-Power Digital I/O This pin may be configured to perform various functions.
18	TX	O	Low-Power UART Data Transmit Signal This signal provides the UART data going from the TD1202 module out to the host application processor. This signal is internally pulled up by an integrated resistor.
19	RX	I	Low-Power UART Data Receive Signal This signal provides the UART data coming from the host application processor going to the TD1202 module. This signal is internally pulled up by an integrated resistor.
20	TIM1	I/O	General Purpose Low-Power Digital I/O This pin may be configured to perform various functions, including the timer input capture / output compare #1 function.
21	TIM2	I/O	General Purpose Low-Power Digital I/O This pin may be configured to perform various functions, including the timer input capture / output compare #2 function.
22	GND	GND	Connect to PCB ground
23	RF_GND	GND	Connect to PCB ground
24	RF	RF	50 Ω Antenna Connection
25	RF_GND	GND	Connect to PCB ground

6 Ordering Information

Part Number	Description	Package Type	Operating Temperature
TD1202-C32	ISM SIGFOX™ gateway 32K Flash/4KRAM TCXO	LGA25 Pb-free	-30° to +75°C

The TD1202-C32 ISM SIGFOX™ gateway module is available in several conditionings.

Please contact Telecom Design for more information.

7 Package Outline

Figure 2 illustrates the package details for the TD1202.

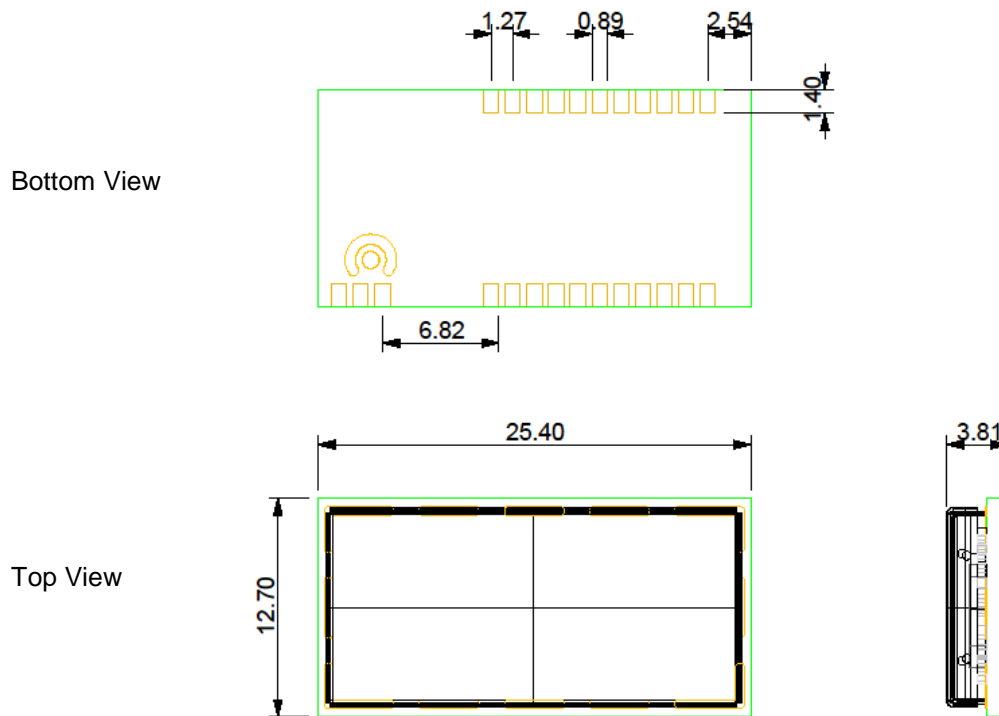


Figure 2. 25-Pin Land Grid Array (LGA)

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.

8 PCB Land Pattern

Figure 3 illustrates the PB land pattern details for the TD1202.

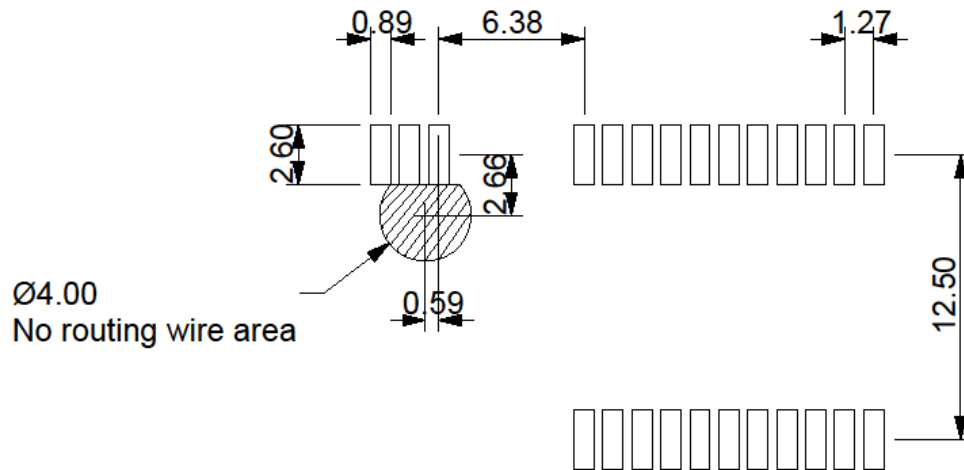


Figure 3. PCB Land Pattern

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.

DOCUMENT CHANGE LIST

Revision 1.0

- First Release

NOTES:

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