Phase-locked loops for motor-speed control

How to design systems, using inexpensive digital ICs, to regulate speeds up to 0.002 percent

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Although the primary application for phase-locked loops has been in frequency synchronization of receivers, a lesser known application area may turn out to be almost equally important—the precise control of motor speed. By locking onto a reference frequency, speed accuracies of 0.002 percent are possible, which represents almost a hundredfold improvement over earlier methods of speed regulation.

The conventional method of motor-speed control is with analog servos. Now the low cost of digital integrated circuits makes the digital approach of phase-locked loops economical. Motors of any size can be controlled with this technique. Once the characteristics of the motor have been incorporated into the response of the phase-locked loop, the only difference is the size of the output transistor. Especially suitable for phase-locked loops are systems in which motors must be synchronized to each other or to an existing clocking signal. An example of the former is a conveyor for materials handling; of the latter, a drive for a computer peripheral such as a disk unit.

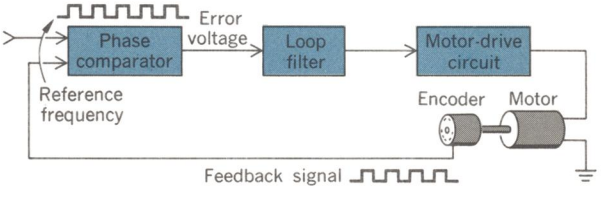
Phase-locked loops date back 40 years to the "homodyne" receiver, where they provided for the synchronous reception of two radio signals. The first widespread use of phase-locked loops occurred in television receivers for synchronizing the horizontal and vertical sweep oscillators to transmitted sync pulses. Later, narrowband phase-locked receivers were used in tracking weak satellite signals because they offered excellent noise immunity. However, it was not until the past few years, when phase-locked loops could be assembled with integrated circuits, that they became economical enough for applications requiring precise control of motor speed and they became relatively simple to design into systems.

A basic phase-locked loop is shown in Fig. 1. Its circuit functions include: the motor itself, an encoder to produce digital pulses representing motor speed, a phase detector to compare the motor speed with a reference frequency, a loop filter to reject noise and determine dynamic performance, and a motor-drive circuit to raise the power level and provide additional control.

Many of these functions are available as integrated circuits and it is possible for the engineer who has little experience in motor-speed control to design a phase-locked loop. Such a system behaves as a servo loop in that it senses motor speed, compares it with a reference, and generates correction signals to compensate for deviations from the reference value. This is shown in the diagram. However, in circuit configuration it bears a strong resemblance to a frequency synthesizer, since its purpose is to generate and regulate a specified frequency. Therefore, the method of design is similar to that for a frequency synthesizer, as we shall see.

The design procedure is concerned mainly with the circuits that control and interface the basic integrated circuit elements, to assure that the loop response meets the criteria for properly controlling the speed of the motor being used. Since this is potentially an oscillatory system, the approach lies in developing a circuit that behaves according to a root-locus diagram specified by the designer, the characteristics of which are satisfied in the design of the loop filter. Basic theory related to this design method is covered in a number of servomechanism textbooks (one such text is listed in the box on p. 62).

[1] Basic phase-locked loop for motor-speed control. A signal proportional to motor speed is compared with a reference. If motor speed is incorrect, the resulting error signal returns the speed to the correct value.



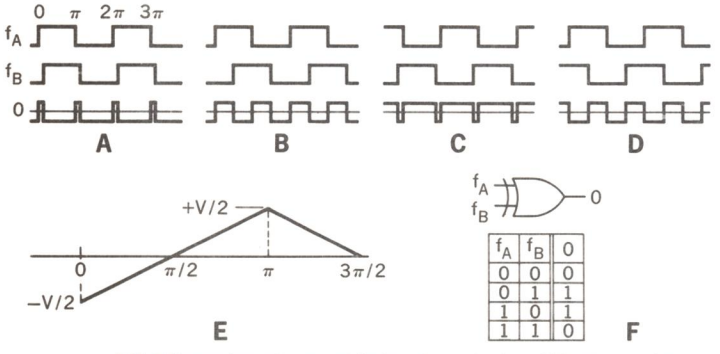
For further information

Chestnut, Mayer, *Servomechanisms and Regulating System Design* (vol. 1). New York: Wiley, 1959.

Gardner, F. M., *Phaselock Techniques.* New York: Wiley, 1966.

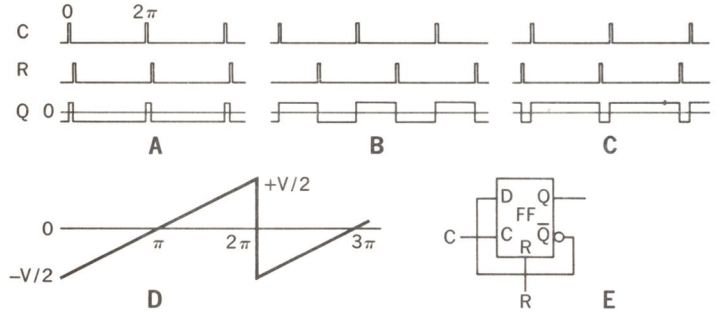
Nash, G , "Phase-locked loop design fundamentals," Appl. Note AN-535, Motorola Semiconductor Products, Inc., Phoenix, Ariz., 1970.

A key difference between phase-locked loops and conventional servos is that the reference input for a phase-locked loop is a periodic signal rather than a fixed voltage. The feedback signal is provided by an encoder assembly that generates a pulse stream whose frequency is proportional to motor speed. The phase comparator detects any difference in frequency or phase and generates an error voltage proportional to the difference. The error voltage then changes the motor speed to reduce the difference between the reference and feedback signals. The important loop parameters, such as acquisition time, capture range, lock-in range, etc., are discussed extensively in the literature on phase-locked loops (see the box to the left). It is sufficient to say here that the motor speed can be synchronized to the reference frequency with extreme accuracy.



[2] Triangular characteristic of exclusive-OR phase detector. This curve results from plotting the average value of the gate output signal as a function of the phase difference between the two input waveforms. Each of the ladder diagrams shows the various combinations of input conditions, which are summarized in the truth table. The bottom row of each ladder diagram shows the gate output produced by the two input signals drawn above it.

[3] Sawtooth characteristic of edge-triggered flip-flop. This circuit is reset once each cycle by the reference input R and is toggled once each cycle by the feedback input signal C. A plot of the average value of the output waveform as a function of the input phase difference results in the sawtooth waveform illustrated.



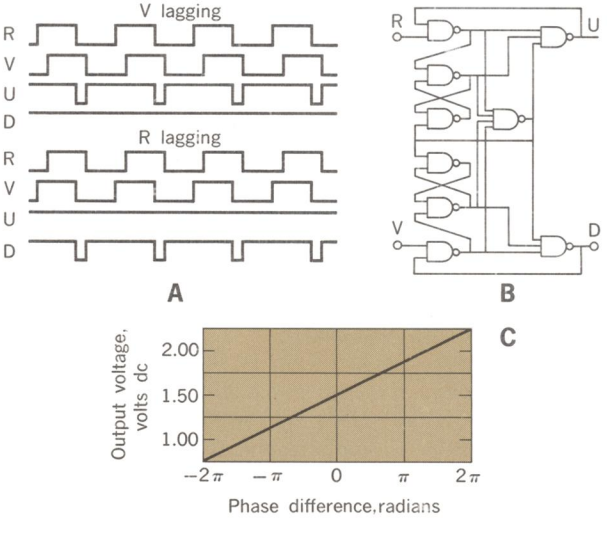
Phase detectors

Three types of digital phase detectors are presently in use: the exclusive-OR circuit, the edge-triggered flip-flop, and a logic gate configuration that behaves in a manner similar to that of the flip-flop, but has some advantages. All three types are found in phase-locked loop ICs. However, some phase-locked-loop circuits use analog detectors.

The triangular characteristic typical of exclusive-OR phase detectors, showing output voltage as a function of phase shifts, is illustrated in Fig. 2. This characteristic results from plotting the average value of the gate output signal as a function of the phase difference between the two input waveforms. Row 3 of each of the ladder diagrams shows the gate output signal for various input-signal phase differences (rows 1 and 2). Note that most standard logic families operate between ground and a fixed positive or negative voltage. However, to aid in visualizing the average value, the midpoint of the gate output voltage swing has been referenced to ground in row 3. For instance, in Fig. 2B, f_A is shown lagging f_B by 90 degrees ($\pi/2$ radians), and the gate is designed so that the average value of the output is zero. As the phase difference is increased toward π radians, the average value of the output approaches a maximum value of $V/2$ volts and is just equal to $V/2$ volts for π radians. Any further increase in input phase difference leads to a decreasing output, until at $3\pi/2$ radians the average value is again zero.

A slightly more complicated digital approach that responds with greater linearity utilizes an edge-

[4] Phase-frequency detector characteristics. The transfer characteristic is similar to the flip-flop phase detector, but has an even wider linear operating range. This circuit avoids both the harmonic sensitivity and the duty-cycle problems encountered with other digital methods.



triggered flip-flop as the phase detector. The circuit shown in Fig. 3 is reset once each cycle by the reference input R and is toggled once each cycle by the feedback input signal C. A plot of the average value of the output waveform as a function of input phase difference produces the sawtooth characteristic of Fig. 3D. In addition to the obviously wider linear range, this approach has significantly better pull-in, tracking, and hold-in characteristics compared with systems using a sinusoidal or triangular phase detector in the circuit.

The two digital methods just described share a common feature—they are sensitive to harmonics in that they can cause the loop to lock to frequencies that are very nearly integral multiples of the desired reference frequency. Although this is used to advantage in some digital mixing schemes, it can be troublesome in synchronization applications such as motor-speed control. An additional characteristic of both these circuits is their sensitivity to changing duty cycles of the input signals. For the exclusive-OR circuit, any deviation from a 50 percent duty cycle results in an extraneous phase error and can also cause the flip-flop phase detector to be improperly triggered, unless precautions are taken. In this type of circuit, the reset input is usually asynchronous and overrides the clock input. Should the R input signal still be high (due to a greater than 50 percent cycle input, for instance) when a C input clock occurs, the circuit will not toggle. This can be circumvented by converting all the input positive-transitions to very short pulses.

A third digital technique is available to avoid both the harmonic sensitivity and the duty-cycle problem. The transfer characteristic, shown in Fig. 4, is similar to that of the flip-flop phase detector, but has an even wider linear operating range. The circuit shown is the phase-detector portion of the MC4344/4044 phase-frequency detector, an integrated circuit specifically designed for digital phase detector and frequency discriminator applications. (Phase-locked-loop ICs made by other manufacturers are discussed in the box below.) The package contains an additional quadrature phase detector similar in operation to the exclusive-OR gate, that can be used for indicating loss of lock in the loop controlled by the main phase detector. Circuits for converting the digital outputs of the phase detector to a suitable analog error voltage are also included.

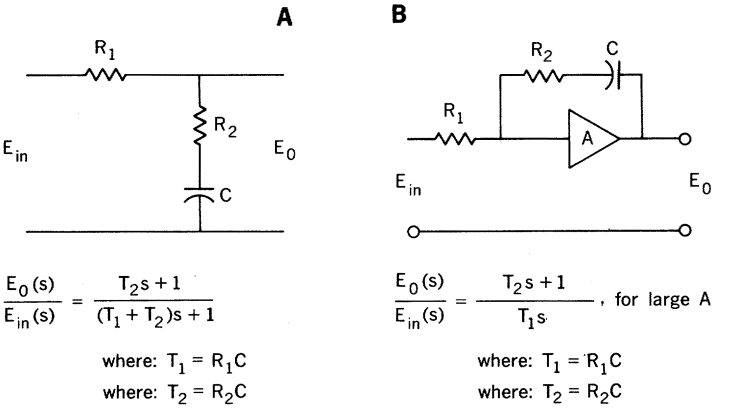
The technique used to avoid harmonic sensitivity is unusual. For a particular phase condition only one of the two output lines is active. For instance, if the feedback signal V (variable) lags the reference R in frequency, a signal is present on the U (up) output line (see rows 1 through 4 of Fig. 4). Conversely, if R lags V, the correction signal appears on the D (down) output line (rows 5 through 8). The circuit responds only to negative transitions of the input signals and locks the loop (zero phase difference) when the negative transitions on both input lines coincide. For this condition, both output lines are high. For any other condition, the average value of the signal on one of the output lines is proportional to the phase or frequency difference between the input signals.

In addition to being independent of duty cycle and insensitive to harmonics, this technique of separating the error commands has another advantage. Unlike loops using other phase detectors, the pull-in range using this method is limited only by the characteristics of the controlled variable. In a frequency synthesizer, for example, this means that the voltage-controlled oscillator can be pulled to any frequency within its range. Of greater interest here is that in speed-control applications, motors can be taken from standstill to the desired operating speed under full control of the loop.

Loop filter

The basic function of the loop filter is to remove noise and high-frequency components from the error voltage. It also has a major role in determining the stability and dynamic performance of the loop. Passive filters such as that shown in Fig. 5A are suitable for many applications. Generally better performance is possible with active filters, but at the added expense of an amplifier. A widely used active filter and its transfer function are shown in Fig. 5B. The effects of this configuration on system performance are covered in the design discussion below, where a typical type 2 second-order system is considered. Type number refers to the number of poles located at the origin of the root-locus plot and the order number refers to the exponent of the highest power of LaPlace operator s appearing in the characteristic equation of the system performance.

[5] Typical loop filters. Passive filters such as shown in A are suitable for many applications. However, better performance is usually possible with active filters that have the added expense of an amplifier, as shown in B.



Who makes phase-locked-loop ICs

In addition to the circuits mentioned in the article, phase-locked-loop ICs are available from Signetics, Exar, Harris Semiconductor, and RCA Semiconductor. All are applicable to motor-speed control, but there are some differences among them. Most have built-in voltage-controlled oscillators, which are bypassed for this application because the motor provides this function. All contain either an analog or digital detector.

System design considerations

In controlling motor speed, motor specifications are determined by the mechanical load, required speed range, etc. If the control signal is digital, it makes sense to utilize the advantages of a digital phase detector and the gain of the phase detector is then fixed. This leaves the designer with only the loop filter and the gain of the motor-control circuits as design variables. Their effects on system performance can be studied in a number of ways; however, the root-locus approach is a good one. The root locus is a complex plane plot of the poles of the characteristic equation as a function of system gain. The location of the poles is closely related to closed-loop performance, and theoretically can be used to determine both the transient and steady-state response of any system.

System characteristics are often specified in terms of the parameters used to describe the transient response of an oscillatory system. A brief review of the relationship between these parameters and closed-loop pole location in the complex plane is needed before describing the operation of a specific system. The conventional damped oscillatory, transient response to a step input is shown in Fig. 6A. The natural frequency of oscillation is defined as $\beta = 2\pi/T$, and the decay rate α is defined as the rate at which the transient response is attenuated. A more commonly used parameter is the decrement factor, or damping ratio ζ. It is defined as the ratio of damping rate to the undamped natural frequency ω_n, where ω_n herewith is defined as

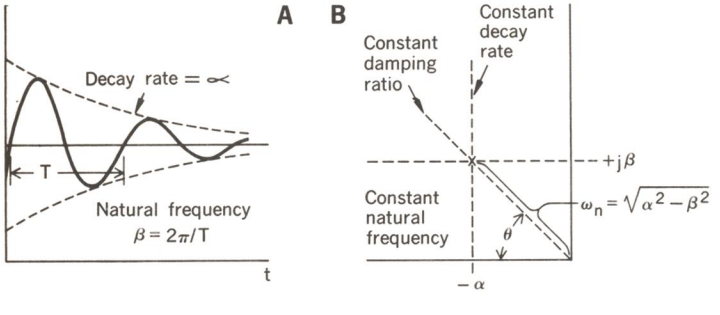
$$\omega_n = \sqrt{\alpha^2 + \beta^2}$$

The closed-loop pole located at $s = \alpha + j\beta$ in Fig. 6B, shows the pole position in terms of the transient parameters. This pole corresponds to a transient term of the form $Ae^{(\alpha + j\beta)t}$, where α is the decay rate and β is the natural frequency. As shown there, all poles located on a given vertical line will decay at the same rate—the further to the left of the imaginary axis, the faster the decay. All poles on a particular horizontal line will have the same natural frequency of oscillation —the further above the real axis, the higher the frequency. From the earlier definition, $\zeta = \alpha/\sqrt{\alpha^2 + \beta^2} = \cos\theta$, and lines radiating from the origin represent lines of constant damping ratios. Large ratios are located near the negative real axis and small ratios are near the positive real axis.

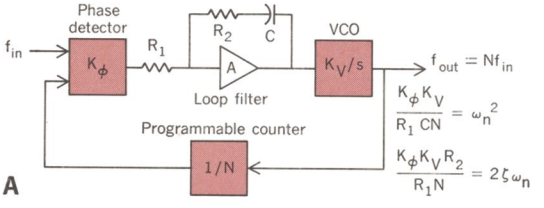
Consider the box below where a simple frequency synthesizer is shown. As suggested at the onset, let us pursue the frequency synthesizer example to gain further insight into the design of an actual motor-speed-control system. Using a frequency synthesizer for this example is not irrelevant, since it is almost a perfect analog to the motor-speed-control loop. The difference is that the motor substitutes for the voltage-controlled oscillator (VCO).

The transfer characteristic of the VCO is K_v radians/s/V, with respect to frequency. However, phase, not frequency, is the parameter of primary interest, and since phase is equal to the integral of frequency, a $1/s$ term must be included in the transfer function. In a root-locus plot, this term is represented by an open-loop pole at the origin. The active filter described earlier is used and it introduces a second

[6] Relationship between transient response and pole location. The oscillatory response of a damped oscillatory system to a step input is shown in A. The closed-loop pole is shown at the intersection of the dashed lines in B, where the constant damping ratio equals the constant decay rate.



Frequency synthesizer design



$$GH = K_\phi \cdot \frac{R_2Cs + 1}{R_1Cs} \cdot \frac{K_v}{s} \cdot \frac{1}{N} = \frac{K(R_2Cs + 1)}{R_1Cs^2}$$

where

$$K = \frac{K_\phi K_v}{N}$$

The characteristic equation is then:

$$1 + GH = 1 + \frac{K(R_2Cs + 1)}{R_1Cs^2} = 0 = R_1Cs^2 + KR_2Cs + K$$

or

$$s^2 + K\frac{R_2}{R_1}s + \frac{K}{R_1C} = 0$$

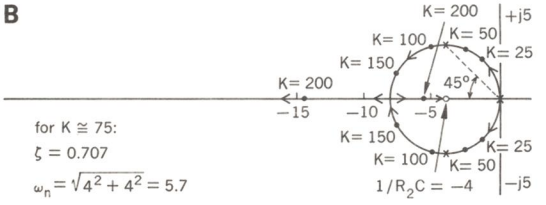
Let $R_2/R_1 = 1/10$ for effective filtering and let $R_2C = 1/4$ in order to position the open-loop zero at the desired location. Then

$$\frac{1}{(R_1/10)C} = \frac{1}{4} \text{ or } \frac{1}{R_1C} = 2.5$$

Substituting these results into the characteristic equation gives

$$s^2 + 0.1\,Ks + 2.5\,K = 0$$

The root locus as a function of gain is then:



pole at the origin and a zero at $-1/R_2C$ on the negative real axis. The resulting root locus is also shown in the box and, as mentioned earlier, is a useful aid in visualizing the effects of circuit changes on system operation. Location of the closed-loop poles varies with loop gain as plotted in the box. The damping ratio and the undamped natural frequency for the assumed pole positions can be obtained directly from such a diagram and are shown here. For ease of understanding, a simple case was chosen.

The initial step in determining specific values for the filter components and loop gain is to interpret the system requirements in terms of the transient response parameters in the following manner: (1) specify the frequency above which high-frequency components of the reference signal must be removed; (2) determine the time limit for reaching the operating point; (3) consider the maximum overshoot, if necessary. These factors mean that loop bandwidth, acquisition time, and overshoot are important system parameters. The resulting requirements can be expressed in terms of ω_n and ζ from the standard type 2 second-order transient response curves found in basic control textbooks.

If there is a maximum overshoot requirement, then a particular damping ratio ζ must be selected to meet it. However, if the peak overshoot is not specified, it is reasonable to assume a damping factor of 0.707 (slightly underdamped), which also simplifies calculations. The acquisition time requirements then determine the value of ω_n. For instance, if the VCO frequency must be within 2.5 percent of its final value in 30 ms, moving on the $\zeta = 0.707$ curve to the point where the transient response does not exceed 2.5 percent gives an approximate $\omega_n t$ of 6.0. Therefore, ω_n is $6/t$, or 200 radians.

For a second-order system, ω_n is related to bandwidth by

$$\omega_{-3\text{dB}} = \omega_n \left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2}$$

and $\omega_{-3\text{ db}} = 2.06\ \omega_n$ for a damping ratio of 0.707. The value of ω_n selected on an acquisition time basis must be checked against bandwidth to insure that the error voltage will be adequately filtered. In applications where loop bandwidth is the primary system parameter, the design procedure should begin with the bandwidth equation, by first assuming a reasonable value for the damping ratio, calculating ω_n, and then checking acquisition time and overshoot with the curves. However, since good filtering and fast acquisition are conflicting requirements, the design must usually be a compromise.

After ζ and ω_n have been determined, the actual circuit values can be calculated using the equations shown in the box on page 64. The equations were derived by equating coefficients of the specific characteristic equation to those of the standard form in terms of ω_n and ζ.

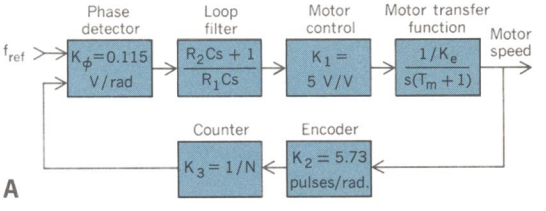
Designing a motor-speed control

Now let us relate the frequency synthesizer design approach described above to motor-speed control. All of the techniques mentioned apply to motor-speed controls, with one exception: the VCO is replaced by a motor and, therefore, the design is complicated by the more complex motor transfer function, as shown in the box below. Since phase (motor displacement) is being compared with a reference by the loop, a $1/s$ term relating displacement to angular velocity is included in the transfer function and replaces the VCO open-loop pole at the origin. The motor introduces two additional poles on the negative real axis, one at $-1/T_m$ and another at $-R/L$. The pole produced by the electrical time constant, R/L, has negligible effect in most cases of practical interest, so only the mechanical time constant need be considered. This leads to the characteristic equation shown in the box.

If the zero introduced by the filter is much closer to the origin than the motor pole, the root locus takes the form shown in the box. As indicated there, the motor pole has very little effect on the response for small values of loop gain. Stated another way, this means that the loop has very little control over the motor.

A more representative case is shown in Fig. 7A, where the motor pole is closer to the origin. Of interest here is that with a fixed filter there are two operating points for a given damping ratio.

Phase-locked-loop motor-speed-control design



A

The open-loop transfer function GH is

$$GH = K_\phi \cdot \frac{(R_2Cs+1)}{R_1Cs} \cdot K_1 \cdot \frac{1/K_e}{s(T_ms+1)} \cdot K_2 \cdot K_3$$

$$GH = \frac{K(R_2Cs+1)}{R_1Cs^2(T_ms+1)}$$

where

$$K = \frac{KK_1K_2K_3}{K_e} = 52 \text{ for } N = 1$$

The characteristic equation is then:

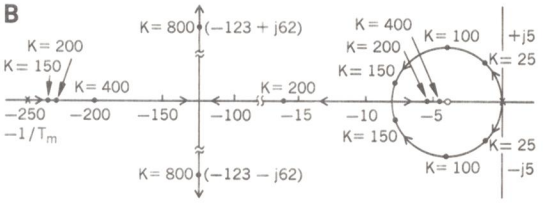
$$1 + GH = s^3 + \frac{1}{T_m}s^2 + K\frac{R_2}{R_1}s + \frac{K}{R_1CT_m} = 0$$

The specific values shown correspond to the design example of Fig. 9.

From manufacturer's data: $K_e = 0.063$ V/rad/s, $T_m = 40$ ms.

From Fig. 9: $R_2/R_1 = 1/10$, $R_1C = 4$, and $K = 52$ (for $N = 1$).

$$1 + GH = s^3 = 25s^2 + 0.1\,Ks + 6.25\,K = 0$$



The loop gain can be adjusted to locate the closed-loop poles on the circular portion of the locus with a narrow bandwidth. This results in good filtering, but slow acquisition. On the other hand, if the gain is increased so that the poles are positioned on the same damping ratio radial and on the vertical part of the locus, then ω_n is larger, acquisition time is faster, and filtering of the error voltage is less effective.

The relative distances of the filter zero and the motor pole from the origin also affect the system response. In Fig. 7B, the motor pole remains at -25 as in Fig. 7A, but the filter zero has been moved from -2.5 to -4.0. As gain increases, the closed-loop pole on the negative, real axis now forces the circular plot to open, with the other two closed-loop poles moving away from the real axis, as shown. This is still an acceptable design configuration and will be stable for normal values of gain, since there are no closed-loop poles in the right half of the complex plane.

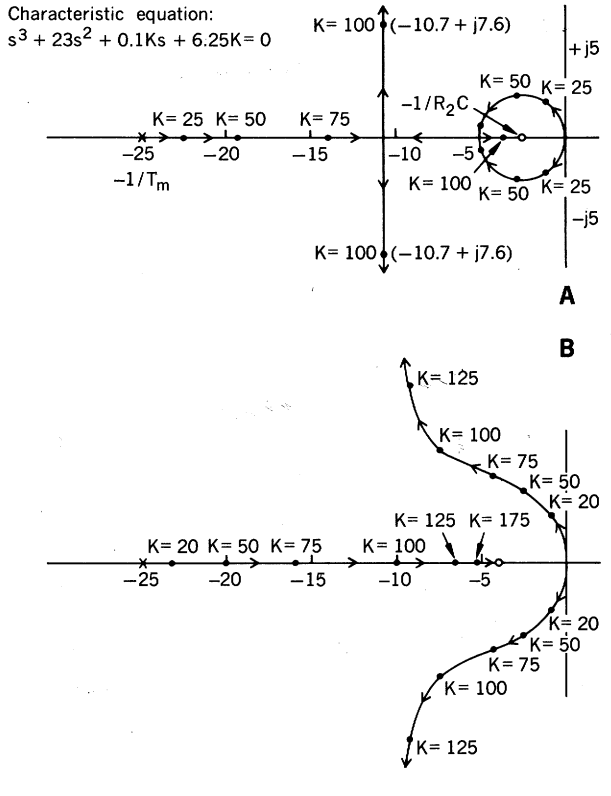
The root locus can also be used to quickly evaluate the effect of changing filter characteristics. If the filter characteristic $F(s) = (R_2Cs + 1)/R_1Cs$ is written as $F(s) = R_2/R_1 + 1/R_1Cs$, it may be considered an integrator with resistive feed-around. That is, it has a low-pass characteristic, but represents a fixed gain of R_2/R_1 to frequencies beyond the passband, which implies that for effective filtering of high frequencies, R_2 should be much less than R_1. A ratio of $R_2/R_1 = 1/10$ was used in Fig. 7.

Figures 8A and 8B illustrate the effect on system performance of $R_2/R_1 = 1/5$ and $R_2/R_1 = 1/1$ respectively. The significant point is that, for the same gain, increasing the magnitude of the resistor ratio not only increases ω_n but also affects the damping ratio. For example, assume that the poles were located at the $K' = 50$ point (ζ slightly greater than 0.707) of the plot in Fig. 7. Increasing the bandwidth to that shown in Fig. 8A for $K = 50$, yields an even larger damping ratio. An additional bandwidth increase to that of Fig. 8B leads to a much smaller damping ratio, which is off the vertical scale in Fig. 8B. Again, these considerations are not necessarily restrictions but the effects should be kept in mind as design parameters are selected.

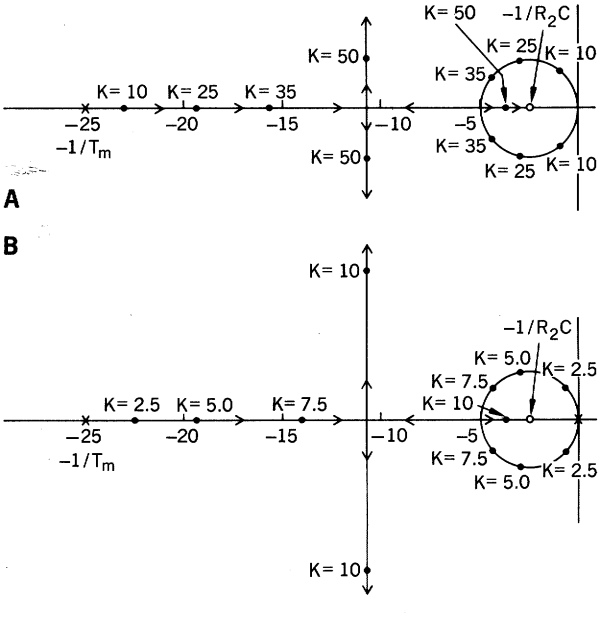
The schematic diagram of a practical design based on these procedures is shown in Fig. 9. The system shown controls a reel-to-reel tape drive. The phase-frequency detector is used to control the speed of a permanent-magnet dc motor. The digital feedback signal is generated by interrupting transmission between two optical devices by means of holes around the perimeter of a plastic disk attached to the motor shaft.

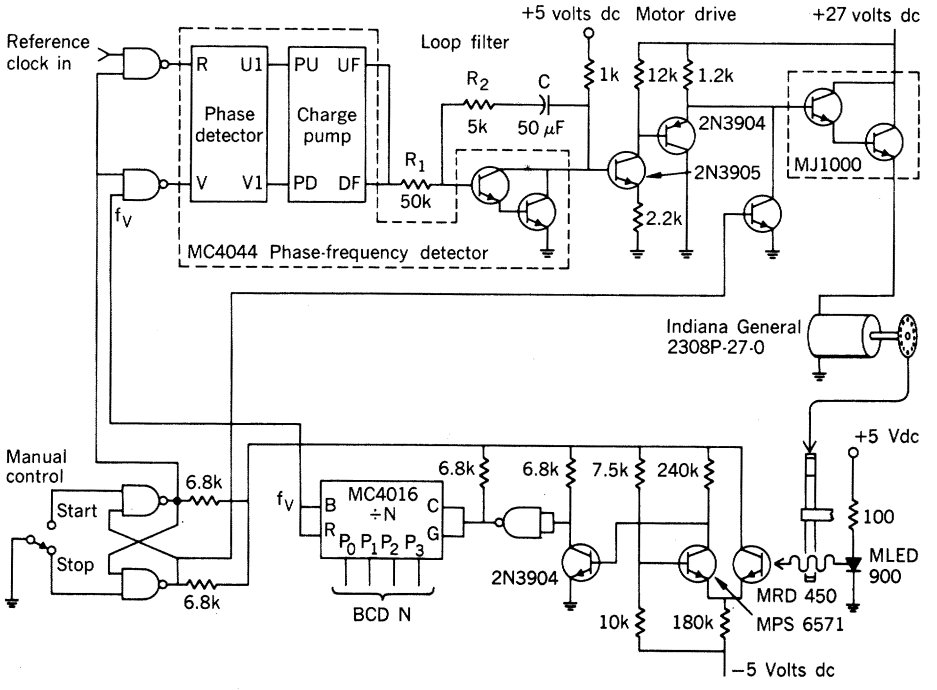
The programmable decade counter in the feedback path provides a simple means of digitally controlling the motor speed. The disk used in this application has 36 holes spaced evenly around its perimeter. Therefore, the optical encoder provides 36 pulses per revolution, or approximately 5.73 pulses per radian. The motor speed v, expressed in radians per second, is then converted to $5.73v$ pulses per second at the encoder output. This is then divided by the counter modulus N, so that the feedback frequency is $f_v = 5.73v/N$ pulses per second or (in rad/s)

[7] Effect of the motor pole in a practical system. The root-locus plot in A represents the characteristics of the design example shown in Fig. 10. Note that with a fixed filter there are two operating points for a given damping ratio. Diagram B shows the effects on the plot of moving the open-loop zero closer to the position of the motor pole (from −2.5 to −4).



[8] The effect on root-locus plot of varying the R_1/R_2 ratio. In diagram A, $R_1/R_2 = 1/5$, whereas in diagram B, R_1 and R_2 are equal. The bandwidth increase in the latter case leads to a much smaller damping ratio, which is not shown because it would be off the vertical scale.





[9] Practical phase-locked-loop design. The digital feed-back signal is generated by interrupting transmission with an optical encoder that provides 36 pulses per revolution. The motor speed *v* is converted to 5.73*v* pulses per second at the encoder output, which is then converted to counter modulus *N*. The feedback frequency f_v is obtained by computing $5.73v/N$.

$$v = \frac{Nf_v}{5.73}$$

In terms of the more commonly used revolutions per minute (r/min), v is given as

$$v = \frac{Nf_v}{5.73} \cdot \frac{60\ \text{s-r}}{2\pi\ \text{min-rad}}$$

$$= 1.67\,Nf_v$$

where f_v is the feedback frequency in pulses per second. Recall now that synchronization will occur when f_v is just equal to the reference input clock f_r. Therefore, the motor speed in r/min is $1.67\,Nf_r$. Counter modulus N can be switched either manually via a BCD thumbwheel switch or electronically. For the circuit shown, the input is 120 pps, allowing the motor to be controlled over the range 200 r/min (N = 1) to 1800 r/min (N = 9). For convenience of illustration, performance of the circuit shown conforms generally to the root locus of Fig. 7 for a gain, K, of 50.

Comparison with servo control

Speed-control applications for motors of the class considered here (i.e., constant velocity with controlled start and stop) can be broadly classified as either open loop or closed loop, depending on the degree of control required. The need for feedback control can usually be determined by a cursory examination of the motor's regulation characteristics. If the open-loop regulation is inadequate, some form of servo control is indicated. If this is the case, there are two basic approaches available—either a conventional analog servo or the digital phase-locked-loop method discussed here.

In the conventional analog servo, a correction signal is generated by sensing velocity variations with a dc tachometer and comparing them with a fixed reference voltage. The phase-locked-loop method forces motor speed to synchronize with a digital pulse train. In computer peripherals where it is desirable to coordinate motor speed with a digital clock or where several motors must run at the same speed as in conveyor systems, the advantages of the phase-locked-loop method are obvious. In applications where synchronization isn't required, the distinction between the two methods is less clear cut. Extremely good precision control can be obtained with either method, and deciding which to use is usually based on economics. It is difficult to define a specific breakpoint, however, the present cost structure of suitable components is such that the digital approach will usually be more economical for high accuracy.

For the reel-to-reel servo previously described, a cost comparison between it and a comparable servo control system shows that the phase-locked-loop IC costs $15, compared with a servoamplifier required for this motor that would cost $40. Both figures are based on catalog prices and do not include encoders or miscellaneous controls. The difference in parts count for building both types of circuits is substantial: The servo system would require approximately 100 parts, against 15 for the phase-locked loop. To this one must also add circuit board fabrication and mounting costs, which magnify the cost differences arising from the number of parts needed in each case.

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