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Analysis, Simulation and Physical Implementation: Modified-SEPIC DC/DC Converter

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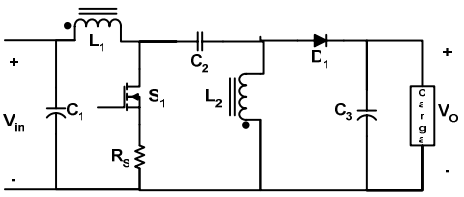
Abstract — **The present paper presents a methodology and electronic analysis in PSPICE for a CD/CD converter with Power Factor Correction (PFC); it is presenting the comparation between the simulated and experimental results. A SEPIC topology is used but with a modification with respects the common configuration in which the second inductor is built as a self transformer with a higher voltage between the external ends an a lower voltage at the middle of the inductor. Beside that the circuit includes an integrated circuit for correcting the power factor, the MC33262. The entire system was simulated and later it was probed in the laboratory where it seems to be working properly.**

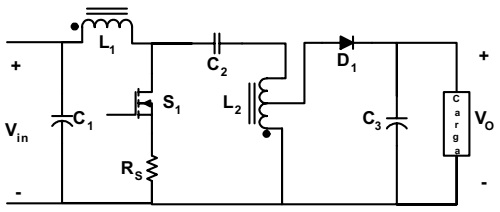
Keywords — **CD/CD converter, MC33262, PFC, SEPIC**

I. Introduction

In the work development [1], [2], it was found that if the output voltage (V_o) is smaller than the input voltage, high transient currents appear on the switch (S_1) and the diode (D_1), for this reason a center tap at the inductor L_2 is proposed, to provide a high output voltage in the primary winding and a small voltage at the secondary winding. The configuration of the SEPIC converter is shown in Fig. 1. Because the voltage in L_1 and L_2 is the same at any moment [3], [4], [5] is allowed winding the inductors in the same core. The characteristic equation for this type of converter is K= Vo/ (Vin + Vo) [4], [5], [6]



a)



b)

Fig. 1. SEPIC converter topology.
a)basic circuit b)modified circuit

II. Specifications

The converter must comply the following characteristics:

Line frequency	60Hz.
Switching frequency (f_{sw})	100 Khz.
Rage input voltage (V_{in})	80 to 140 V a.c
Output voltage (V_o)	14 V d.c
Output power (P_o)	35W

III. Methodology

As it was analyses in [3] with the input and output specifications, it was calculated the RMS minimum and maximum input voltages, as well as the peak current, considering a potential of 100V in the primary winding, to diminish the transitory current in the switch; the voltage between the ends of L_2 is bigger than the output voltage so we have as follows:

Primary voltage	= 100V
Secondary voltage (V_o)	= 14V

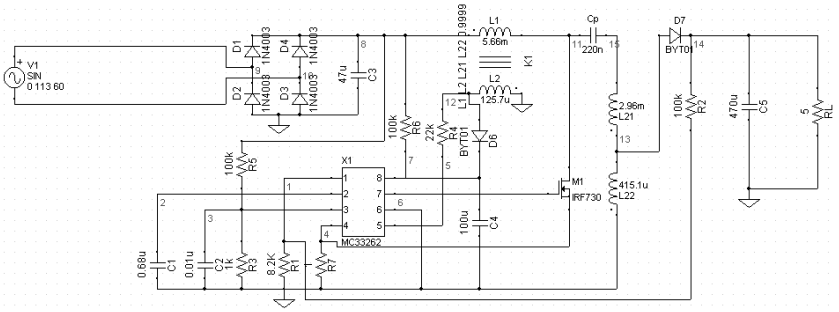


Fig. 2. Modified-SEPIC converter topology as it was simulated.

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$$\frac{N_P}{N_S} = \frac{V_P}{V_S} \quad (1)$$

According (1) we have a turn ratio of 7.14

$$I_P = \frac{N_S}{N_P} I_S \quad (2)$$

Using (2) we rename the current at the secondary (I_P) as I_{PKMOD}=371mA. We calculate de input voltages minimum and maximum in terms of rms values so we have $V_{inMIN} = 113V_{RMS}$; $V_{inMAX} = 198V_{RMS}$. Now we calculate the minimum and maximum duty cycle [6], having D_{max}=0.4691 and D_{min}=0.3355.

$$D_{max} = \frac{V_0}{V_0 + V_{inMIN}} = \frac{100V}{100V + 113V} = 0.46 \quad (3)$$

$$D_{min} = \frac{V_0}{V_0 + V_{inMAX}} = \frac{100V}{100V + 198V} = 0.33 \quad (4)$$

Considering a switching frequency of 100 kHz (T=10μs) in the switch, we calculate the value of the inductor L_1 and L_2 [6]:

$$L_1 = \frac{2T(1 - D_{max})Vin_{max}}{I_{PKMOD}} \quad (5)$$

$$L_2 = \frac{2TD_{max}Vin_{max}}{I_{PKMOD}} \quad (6)$$

As both inductors were wound in the same core, it is calculated according (5) and (6) that $L_1 = L_2 = 5.66$mH.

Considering a coupling factor K=0.9999 between the inductors, as well as an inductors ratio (α) between L_{2a} and L_{2b} of 0.14.

$$L_{2a} = \frac{L_2}{\alpha + 1 + 2K\sqrt{\alpha}} \quad (7)$$

$$L_{2b} = \alpha L_{2a} \quad (8)$$

Using (7) and (8) we have L_{2a}=2.9656mH and L_{2b}=0.4151mH.

Finally we calculate the capacitors C_1, C_2 and C_3 [6]:

$$C_3 = \frac{A_{min} I_S D_{min} T}{\Delta V_{C3}} \quad (9)$$

$$C_1 = \frac{C_3}{10} \quad (10)$$

$$C_2 = \frac{I_{PKMOD} D_{min} T}{\gamma V_{inMIN}} \quad (11)$$

Substituting the values at the (9), (10) and (11) we have C_1=47μF, C_2=220nF and C_3=470μF.

Using the datasheet of the IC MC33262 [7], which it was used as a driver of the switch as well as a power factor corrector, we calculate the values of the elements showed in Fig.2

IV. Simulated Results

The circuit shown in the Fig. 2 was simulating using the corresponding the necessaries models in PSPICE for each elements, that was done to test the theory against the simulation, we can consider the obtained results were as close as it was predicted by formulas. That was because the circuitry that is analyzed is a DC/DC converter, it means that the waveform of the output voltage (V_o) have to be a DC signal; however for obtaining the DC signal of the converter it is necessary the used of a full bridge AC/DC converter, here is where the PFC definition takes place in order to obtained a higher efficiency of the entire prototype.

In the Fig. 3 it is shown the wave form of the voltage at the ends of the inductor L_2, where we can see that voltage is closely 100V.

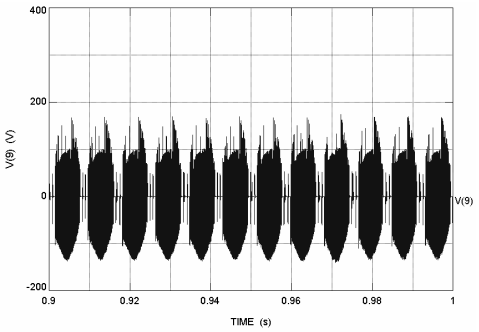

Fig. 3. Voltage at the ends of the inductor L_2.

In the Fig. 4 it is shown the wave form of the voltage at the center tap of the inductor L_2, where we can see that voltage is closely 14V.

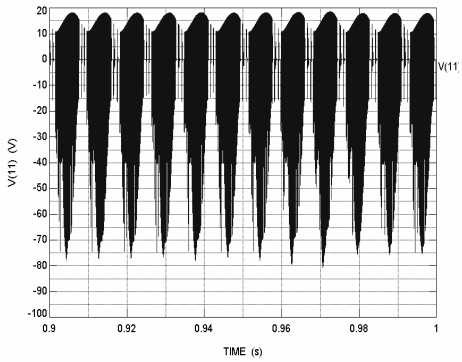

Fig. 4. Voltage at the center tap of the L_2.

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In the Fig. 5 it is shown the wave form of the voltage at output of the converter, where we can see that voltage is closely 14V, even do the obtained curl was bigger tan the predicted value.

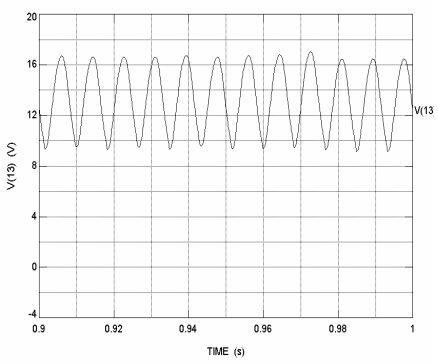

Fig. 5. Output voltage of the converter.

In the next figure we can see how the circuit has done the correction of the power factor; because the wave form of the input current is similar a sinusoidal form that means the entire system is working properly.

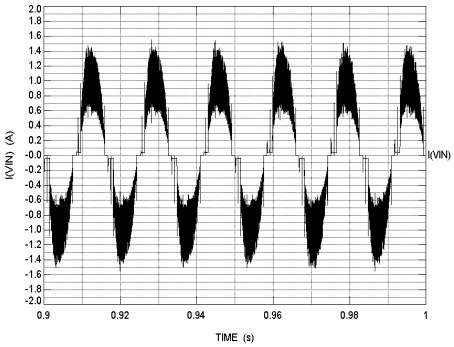

Fig. 6. Input current where we can see the power factor correction.

V. Experimental Results

We built two cards, the first one shown in fig. 7 it was called the power card in which is contained the SEPIC converter, whereas the second card was for the control circuit as shown in fig. 8 where the MC33262 was place.

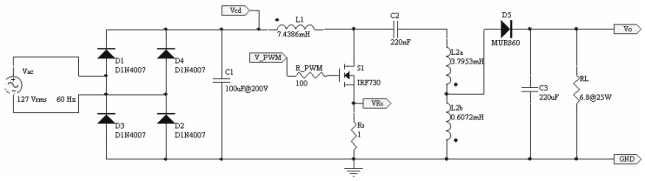

Fig. 7. Power card with the SEPIC converter.

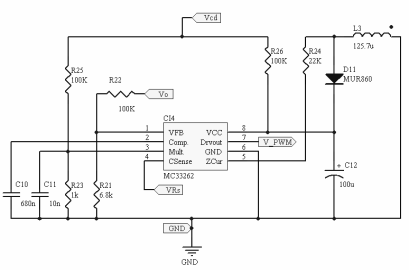

Fig. 8. Control card with the MC33262.

The two cards were interconnected for the test and the obtained results were satisfactory as shown in the next figures.

In the Figure 9 we can see the voltage between the ends of the inductor L_2, however the voltage is lower than the predicted value.

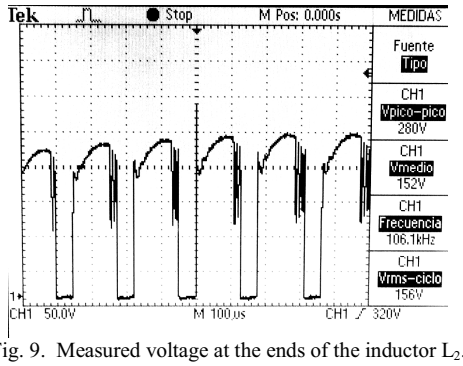

Fig. 9. Measured voltage at the ends of the inductor L_2.

In the Figure 10 we can see the voltage at the center tap of the inductor L_2, where we can see that the voltage was slightly lower that the expected value.

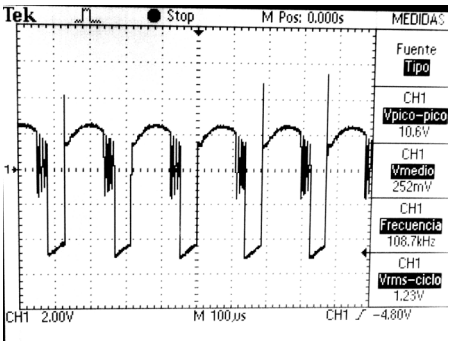

Fig. 10. Measured Voltage at the center tap of the L_2.

In the Figure 11 we can see the output voltage, however the curl is too much bigger than the expected, that was because the value of the used capacitor was lower that the needed value, it means we needed a polyester capacitor with a value of 470µF, the capacitor bough was of 9µF; that was the greater value that was find.

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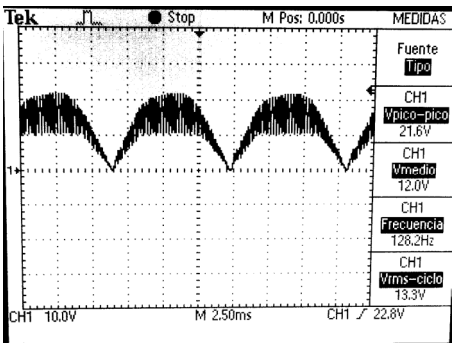

Fig. 11. Output voltage of the converter.

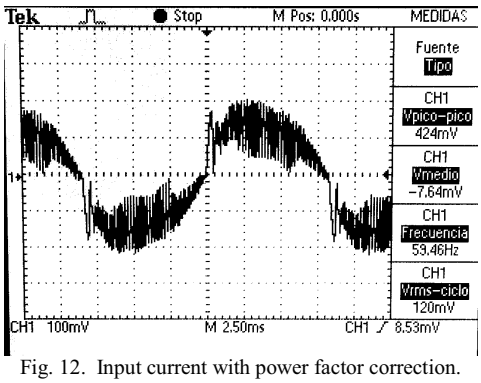

Fig. 12. Input current with power factor correction.

In the Figure 12 we can see the input current, the IC MC33262 did correct the power factor, as we see the wave for at the input of the circuit is almost a sinusoidal wave form. So we can consider that the circuit accomplishes its purpose.

VI. Conclusion

From the obtained results, we can conclude that the main objective of the work was fulfilled; we can see the figures 3 and 9 that the voltage at the inductor L_2 that was closely as it was predicted. It happens with the voltage at the center tap of the inductor shown in figures 4 and 10.

However the curl of the output voltage, figures 5 and 11, is bigger than the expected value because we used a lower value of the capacitor C_3 in terms of the availability for polyester capacitors, because we needed a 470µF polyester capacitor but it was increase the cost of the prototype in terms of the necessity of a bank of lowed value polyesters capacitor.

We can see that the correction of the power factor was accomplished as it is shown in figures 6 and 11, where the wave for was very similar to a sinusoidal wave form.

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