100W Power Factor Correction Of Basing On L6561

Suling Xie, Lifang Liu
School of Electronic & Information, Hangzhou Dianzi University
Hang Zhou， China

Jingbiao Liu
School of Electronic & Information, Hangzhou Dianzi University
Hang Zhou， China

Abstract—**This paper introduced the design of 100W active power correction factor circuit. It gives main calculating parameter of circuit structure ,In a wide range of input voltage, improving the power factor and reducing the pollution of electronic grid.**
Keywords- L6561; APFC ; control circuit

I. INTRODUCTION

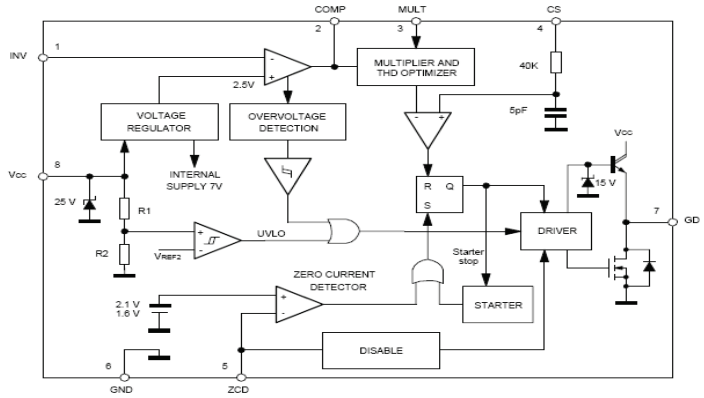
Recent years， because of the development of electronic technology, all kinds of office automation devices， family electrical appliances and computers using increase year by year. These devices inside need a power supply that make AC translate in to DC. During this translation can generate a lot of harmonic current and cause electronic system pollution . As restrict standard, various country have published respective standard. So restrain of harmonic current and power factor correct are important project of research. Common power supply often is afforded by 220V AC. Electric supply 220VAC through rectification and a capacity filter, finally gain a DC voltage . Because rectifier diode and big input filter capacity are not line components. Though input voltage is sinusoidal wave , input current wave cause serve distortion and demonstrate narrow pulse .Due to the input current is not sinusoidal , harmonic current is harmful affect to the power system. Narrow pulse current contains a lot of harmonic wave and make power supply noise. At the same time, the input of rectification circuit use big filter capacity not only cause high cost but also have large volume. Power supply of electronic instrument have serve harmonic current flow into electronic supply and cause harmonic pollution .This make quadratic effect that is current flow into line circuit impedance and produce harmonic voltage .Conversely, it also make electronic voltage distoration. Another aspect may cause circuit accident and let the device hurt . So power factor correction of driver circuit design is an important research .

L6561 chip application circuit is always considered as classical APFC circuit which is convenience test ,less external components and good reliable .Therefore this paper adopt L6561 of ST company as control chip and design a 100W Boost converter which is CRM mode APFC. This project improve power factor and reduce electronic supply pollution .

II. L6561 CHIP INTRODUCTION

A. L6561 Chip Pin Discription

L6561 adopt 8pin DIP package and it integrates voltage error amplifier ,multiplier ,over voltage protect circuit ,start circuit， zero detect , PWM comparator, PWM logic and gate drive circuit. Internal diagram is shown on below picture：



L6561 chip internal diagram

B. L6561 Work Theory

L6561 is CRM mode APFC chip ,its operation theory is in every switch period when inductance current pass zero turn on the switch not until attain twice inductance current turn off MOS. Through inductance of auxiliary wind detect inductance current .Auxiliary wind and Boost inductance phase is reverse. When MOS is turn off and current of boost inductance is rising gradually and at the same time secondary wind react voltage. But zero current sense of PFC control chip is negative. When MOS is turn off ,flow in to the current of boost inductance decrease gradually ,once reduce by zero, The phase polarity of auxiliary wind opposition is positive. Its value is direct ratio to PFC output voltage and rectifier input voltage differentials. While ZCD pin voltage is less 1.6V, zero current detect is trigger and turn on switch. Start a new switch period. Through current of inductance from zero set up and down to zero continual. Its envelope variety trace rectifier output voltage signal envelope.

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III. DRIVER CIRCUIT DESIGN

Basing on L6561 chip，circuit design gain width range input voltage: 85-265V AC , driver circuit power is 100W, output voltage is 385V.

A. Main Circuit Design

- Boost inductance

Boost inductance value is determined by output power and minimum switch frequency. In the designing of circuit to avoid noise coming ,switch frequency must higher than 20KHz,according to the MOS turn on and turn off time and inductance current are line vary ,we can see that

$$t_{on}=L\frac{I_{L(peak)}(t)}{V_{in(peak)}\sin(\omega t)}=L\frac{2\cdot I_{in(peak)}\sin(\omega t)}{V_{in(peak)}\sin(\omega t)}=L\frac{2\cdot I_{in(peak)}}{V_{in(peak)}} \quad (3.1)$$

$$t_{off}=L\frac{I_{L(peak)}(t)}{V_o-V_{in(peak)}\sin(\omega t)}=L\frac{2\cdot I_{in(peak)}\sin(\omega t)}{V_o-V_{in(peak)}\sin(\omega t)} \quad (3.2)$$

From the formula, $I_{L(peak)}$ is inductance current ,

$I_{in(peak)}$ is peak of AC input current , $V_{in(peak)}$ is

AC input voltage , V_o is output DC voltage

I_o is output DC current, η is APFC efficiency.

According to power integral have:

$$I_{in(peak)}=\frac{2\cdot V_o I_o}{\eta\cdot V_{in(peak)}} \quad (3.3)$$

From (3.1) (3.2) can conclude that:

$$T_s=t_{on}+t_{off} \quad (3.4)$$

$$=2\cdot L\cdot I_{in(peak)}\left\{\frac{1}{V_{in(peak)}}+\frac{\sin(\omega t)}{V_o-V_{in(peak)}\sin(\omega t)}\right\}$$

$$=\frac{4\cdot L\cdot V_o\cdot I_o}{\eta\cdot V_{in(peak)}^{\ 2}}\left\{1+\frac{V_{in(peak)}\cdot\sin(\omega t)}{V_o-V_{in(peak)}\cdot\sin(\omega t)}\right\}$$

The maximum of T_s is

$$T_{s(\max)}=\frac{4\cdot L\cdot V_o\cdot I_{o(\max)}}{\eta\cdot V_{in(peak)}^{\ 2}}\left\{1+\frac{V_{in(peak)}}{V_o-V_{in(peak)}}\right\} \quad (3.5)$$

$$L=\frac{\eta\cdot V_{in(peak)}^{\ 2}}{4\cdot f_{sw(\min)}\cdot V_o\cdot I_{o(\max)}}\left(1+\frac{V_{in(peak)}}{V_o-V_{in(peak)}}\right) \quad (3.6)$$

Input voltage V_{in} can achieve width voltage $V_{in(rms)}=$ 85V～265V AC , by (3.6) calculate L is 1500uH～2000Uh, In practical application, MOS switch frequency is $f_{sw(\min)}\geq 20kHz$, L =1942 μH , adopt PQ2620 core , $\varnothing 0.3\times 6$ cotton covered wire 90turn.

- Auxiliary wind

When input voltage V_{in} is the maximum , Auxiliary wind output voltage is the most lowest. Auxiliary wind output voltage must higher than 1.5 V that is threshold voltage of ZCD. Then:

$$N_{aux}>\frac{1.5V\cdot N_p}{V_o-V_{in(peak\_\max)}} \quad (3.7)$$

From the formula, N_p is primary turn, $V_{in(peak\_\max)}$ =385V, calculate PFC inductance Auxiliary wind turn is $N_{aux(\min)}=5$,this design use N_{aux} =7

- Input capacity

When input voltage is the lowest and load is the highest, voltage ripple wave of input capacity is the biggest . because during one switch period ,input current is consider as continuously , according to the practical value ,choose C1=0.1UF, type is high frequency CBB21 capacity.

- Out put capacity

In the APFC converter, output capacity design usually requirement of keep time ,ripple wave and current of main capacity is not queation. Typical capacity value is 1uF to 2uF every wattage. Output filter capacity $C_{out(\min)}$ is

$$C_{out(\min)}=\frac{2\cdot P_o\cdot\Delta t}{V_o^2-V_{o(\min)}^{\ 2}}=\frac{2\times 280\times 30\times 10^{-3}}{385^2-285^2}=251uF \quad (3.8)$$

Because capacity value has error, the capacity should consider derate using . In this design derate 20 percentage,

make sure satisfied requirement of capacity ,then capacity value is $C_{out}=\frac{C_{out(\min)}}{1-\Delta C_{tol}}=\frac{251}{1-0.2}=314uF$

- MOS diode

When MOS turn off ,it will bear opposition voltage 400V, so $V_{DSS}>400V$. flow in to MOSFET maximum average current is I_{Qrms}

$$I_{Qrms}=I_{L(peak\_max)}\sqrt{\frac{1}{6}-\frac{4\sqrt{2}\cdot V_{in(LL)}}{9\pi\cdot V_o}}=\frac{2\sqrt{2}\cdot V_o\cdot I_{o(max)}}{\eta V_{in(LL)}}\sqrt{\frac{1}{6}-\frac{4\sqrt{2}\cdot V_{in(LL)}}{9\pi\cdot V_o}} \quad (3.9)$$

From the formula , $V_{in(LL)}$ is minimum input voltage virtual value. $V_{in(LL)}$ =165V, due to the formular (3.9) calculate $I_{L(peak\_\max)}=5.22A$

$I_{Qrms}=1.484A$, choose IRFBC840 of IR company

On resistance is $R_{DS(on)}=0.85\Omega$, $t_f=29\,ns$

$C_{oss}=96\,pF$, $V_{DSS}=500V$, $I_D=8.0A$

- High frequency rectifier diode D1

When D1 is turn off , it will bear opposition voltage 400V,

Then $V_R>400V$. flow current of rectifier diode is $I_{Davg}=I_{o(max)}$ we choose fast recover diode HFA08TB60 of IR company, V_f =1.4 V,

$V_R=600V$, $I_F=8.0A$, power loss is P_{Diode}

$P_{Diode}=V_f\cdot I_{Davg}=1.4V\times 0.73A=1.02W$

B. Control Circuit Design

- Output voltage sense resistor and feedback cycle design

L6561 reference voltage of chip internal error amplifier $V_{ref}=2.5V$, output voltage sense resistor R_8 and R_9 value is determine by (3.10). Output voltage sense resistor will power loss , R_8 is bigger than 1 MΩ , because pin INV internal capacity C_p , over R_8 value will lead over voltage protect delay, it will increase over voltage protect voltage threshold .

$$\frac{R_{o1}}{R_{o2}}=\frac{V_{o\_high}-2.5}{2.5} \quad (3.10)$$

R_8=1.02M , R_9=6.5K

For APFC circuit , band width of compensation cycle circuit must small 20Hz, otherwise input current will distortion, effect power factor。 Through capacity of COMP and CND pin can make 100 MHZ ripple weaken 40Db, capacity C_{comp} is

$$C_{comp}\geq g_m\cdot\frac{R_{o2}}{0.01\cdot 2\pi\cdot 100Hz\cdot(R_{o1}+R_{o2})} \quad (3.11)$$
$$=115\times\frac{6.5K}{0.01\times 2\times 3.14\times 100\times(1.02M+6.5K)}=116nF$$

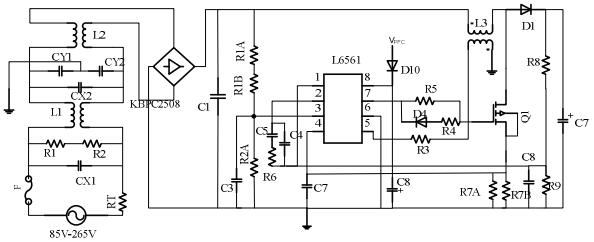
Capacity C_{comp} is 330Nf, in order to improve adjustment of output voltage, C_{comp} is connection R_{comp} in series and increase gain of middle frequency range, adopt R_{comp} =5.1K, At the same time parallel a capacity C_{filter} that is 1/10～1/5 C_{comp}, C_{filter} =47nF.

- Current sense resistor design

When AC input voltage is the lowest and load is the highest ,L6561 voltage of CS pin is maximum. Voltage of over current protect V_{CS} = 0.8V, so

$$R_{sense}<\frac{0.8V}{I_{L(peak\_\max)}}=0.8V\frac{\eta\cdot V_{in(peak\_\min)}}{4\cdot V_o\cdot I_{o(\max)}} \quad (3.12)$$

R_{sense}=0.6Ω.

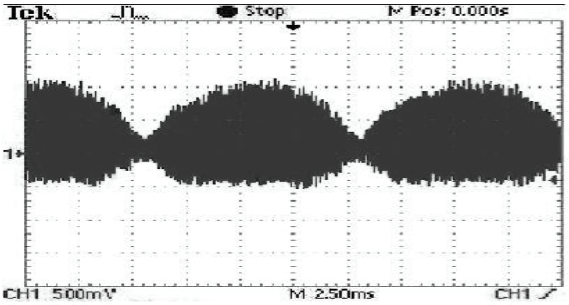


100W APFC scheme picture based on L6561

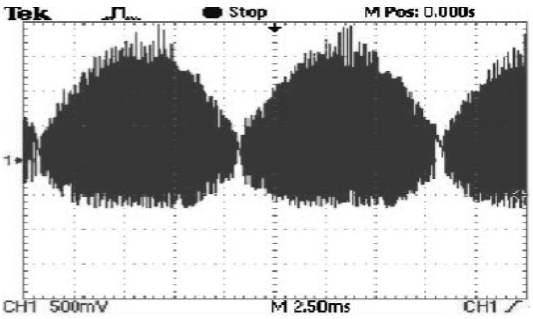
IV. PFC RESULT OF CIRCUIT TEST AND ANALYSIS

A. Authors and Affiliations Inductance Current Waveform And Analysis

When APFC circuit work normally ,inductance current envelope is half sinusoid of 100Hz . Next picture is input voltage is 130V and 260V wave of inductance current . From the picture 1 ,we can see that inductance current peak value is approximation sinusoid wave, period is 100Hz , peak value is relative to input voltage. This can descript APFC circuit of L6561 chip is able to work range is 85-265V . under the work voltage range chip operation current peak control ,zero current CRM mode , function stable .



130v input inductance current waveform

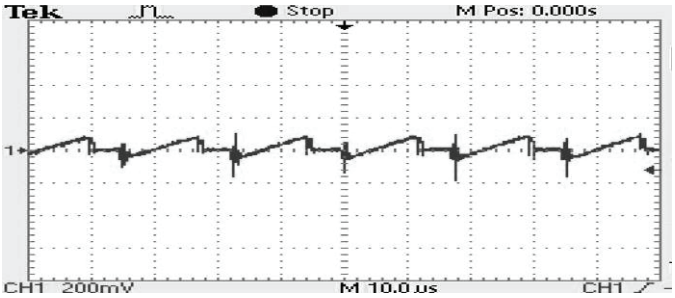


260v input inductance current waveform

picture 1 inductance current waveform

B. Inductance current sample wave and analysis

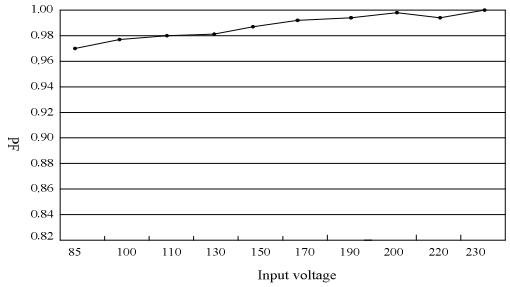
L6561 chip 5 pin is inductance current sense point ,sample inductance current is compared to internal reference signal and achieve inductance current peak control . Working condition of this pin sample signal wave is shown picture 2 ,from the picture we can find out sample voltage is stable , value of amplitude is about 100 mV, circuit is stable ,sample frequency is 50KHz.



picture 2 Inductance current sample wave form

C. PF value table of variety input voltage

Picture 3 is 85Vac~265Vac、50Hz input condition, PF value is followed by input voltage. So, whatever low voltage and high voltage ,PF value is improve .



picture 3 PF value of different input voltage

V. CONCLUTION

This paper designs a 100W APFC circuit and direct detailed main calculate parameter of circuit structure .This circuit is able to operate stably and test conveniencely. From the practical result indicates that in the width range of input voltage ,PF value is improved , harmonic current accord with country standard and electronic pollution problem is perfect .

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