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A New boost power factor pre-regulator

B.P. Divakar & D. Sutanto*
Research associate
*Professor,
Electrical Dept, The Hong Kong Polytechnic university
Hung Hom, Kowloon

Abstract

A novel boost Power Factor corrector using a single switch is discussed. The new circuit is analyzed in steady state and experimental results obtained from the laboratory prototype are also provided. The novel converter has low current and voltage stresses and has a simple control loop to achieve near unity power factor with the aid of the commercially available chip UC3854. Another advantage of the converter is the ability to provide soft switching conditions for the diodes and zero-current switching for the active switch at turn-on using only one switch without increasing the component count.

I. INTRODUCTION

The electronic equipments, used in offices and commercial buildings, are normally fed by a bridge rectifier with a large capacitor at the output terminals of the rectifier. The size of the capacitor depends on the system's requirement such as the holdup time. As this capacitor is charged for a brief period of the input ac voltage, the input current looks like a pulse with a high peak, which is far from the desirable sinusoidal wave shape. The effects of such a current are well known and are as follows: 1) the peak current may exceed the ratings of the series circuit breaker. 2) The harmonics generated by the current cause a large current in the neutral wire of the distribution system. The harmonic components contribute to a low power factor. The importance of curtailing the harmonics generated by the devices has gained importance because it is more economical to design the power supplies with low harmonic emission as an inherent feature than taking measures to reduce the harmonics at the end of the production stage.

II. BACKGROUND OF THE WORK.

Soft switching power factor correctors have been reported [1-4], and have been known to use many components to achieve soft switching with high current/voltage stresses. The other line of research is on the development of single stage power factor corrector, which integrates the function of the power factor pre-regulator and voltage regulator [5-6]. The main limitation is that it is suitable for low power applications as it is operated in discontinuous mode. The converters described in the literatures have one or more of the following limitations:

1. Capacitive turn-on loss is not eliminated
2. Use of many components
3. High voltage/current stress
4. Discontinuous mode of operation
5. Complex control circuits

OBJECTIVES OF THE WORK.

1. To design a boost converter with a single switch operating at a constant switching frequency.
2. To achieve soft-switching for the diodes and zero current switching at turn-on for the switch.
3. To demonstrate that the new boost converter can be implemented as a Power Factor pre-regulator and a dedicated chip can be used to achieve average current mode control.

The paper is organized as follows:
The operation of the novel boost converter as a DC-DC converter will be discussed in Section III. The application of this converter as a power factor corrector will be discussed in Section IV and the experimental results are given in Section V followed by concluding remarks in Section VI.

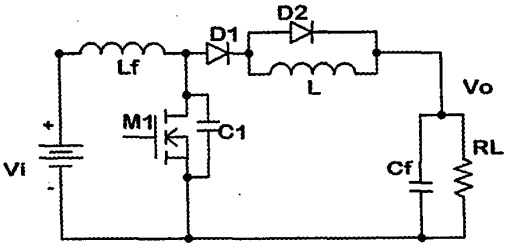

Fig. 1. The new Boost converter

III. OPERATION OF THE BOOST CONVERTER

The proposed boost converter is shown in Fig.1. C1 is the body capacitor of the switch. It is assumed that the input filter L_f is large enough to make the input current continuous, and therefore the input section can be regarded as a constant current source for analysis. As C_f is usually large to minimize the output voltage ripple, the output section comprising C_f and the load can be replaced by a constant voltage sink.

The converter undergoes five topological stages in one switching cycle as shown in Fig.2. The theoretical waveforms of the converter are depicted in the Fig.3.

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A. Analysis of the converter

Stage 1: At t=T_0, the switch M1 is turned on. In the previous stage, the diode D1 and the inductor L were carrying the input current. The current in the inductor is discharged on account of the reverse voltage applied across it. The current in the switch increases linearly until the current through D1 and L is zero. At the end of the stage, the current through the switch is equal to the input current. therefore, the turn-on condition of the switch is ZCS and capacitive turn-on loss is present.

I_S and I_L are the currents through the switch and the inductor respectively.

I_i is the input current.

The expressions for the switch and the inductor current are:

$$I_S(t) = \frac{V_0}{L}t$$
$$I_L(t) = I_i - I_s(t) = I_o - \frac{V_0}{L}t_o \quad (1)$$

The final conditions are:

$$I_S(t_1) = I_i$$
$$I_L(t_1) = 0 \quad (2)$$

The duration of the stage is:

$$t_1 = \frac{I_i L}{V_0} \quad (3)$$

Stage 2: This is the freewheeling stage in which the load is isolated from the input. The stage ends when the feed-back circuit dictates the turn-off of the main switch at ZVS. However, a small turn-off loss is associated during this transition. The duration of this stage is t_2, which can be adjusted to regulate the output voltage.

Stage 3: The parasitic capacitor C_1 is charged by the input current. The voltage across the switch increases linearly until the diodes D_1 and D_2 clamp the capacitor voltage at V_o. The capacitor voltage is given by:

$$V_{C1}(t) = \frac{I_i}{C}t \quad (4)$$

At the end of the stage:

$$V_{C1}(t_3) = V_0$$

The duration of the stage is:

$$t_3 = \frac{CV_0}{I_i} \quad (5)$$

Stage 4: The input current initially flows through D_1 and D_2, the current through the inductor L will then rise exponentially until $I_L=I_i$. The duration of this stage $t_4=3*\tau$.

τ = L/r, where "r" is the combined resistance of D_2 and the external resistor that could be placed in series with D_2 [9].

At the end of the stage;

$$I_L(t_4) = I_i, I_{D2}(t_4) = 0 \quad (6)$$

Stage 5: In this stage, a constant input energy is transferred to the load.

The duration of this stage is obtained as

$$t_5 = T_S - (t_1 + t_2 + t_3 + t_4) \quad (7)$$

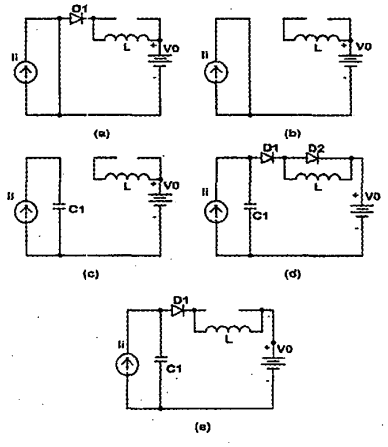

Fig.2 Topological stages of the converter

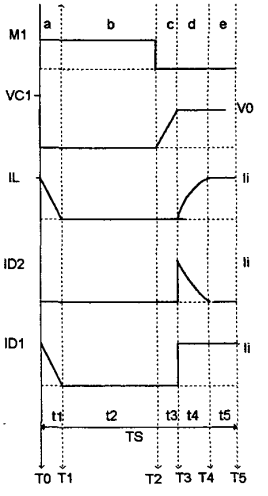

Fig. 3 Theoretical waveforms

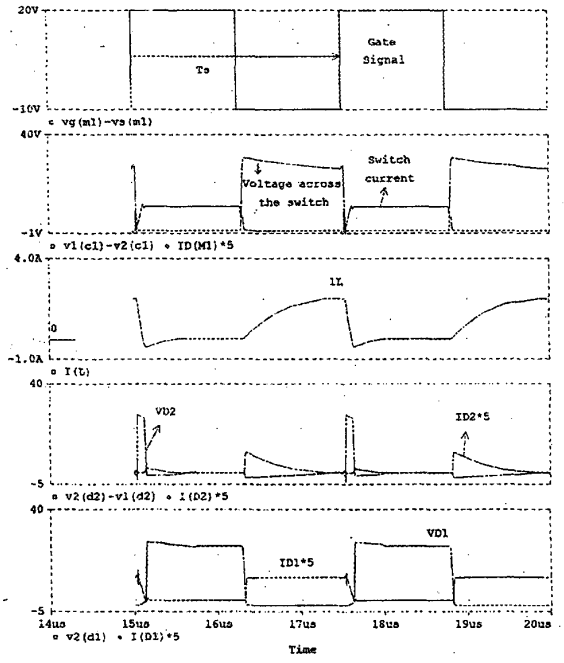

Fig.4 Simulated waveforms

The simulated waveforms in Fig.4 confirms the analysis of the converter under DC steady state condition. The soft switching conditions for the diodes and ZCS turn-on of the main switch are clearly evident from the simulated waveforms.

IV. POWER FACTOR CORRECTION USING THE NEW BOOST CONVERTER.

Fig.5 shows how the new boost converter can be used to provide Power Factor correction when it is inserted between the load and a rectifier. A dedicated chip UC3854A is utilized to provide the control signal. In Section III, the boost converter was analyzed under DC condition, however the same analysis applies when the boost converter is connected to an ac source for Power Factor correction. This is because, the switching frequency of the converter is very large compared to the ac mains frequency, and the input voltage can be regarded as constant during each switching cycle.

. The average control technique is implemented using the commercially available UC3854A chip. The design procedure of [7 & 8] is followed in designing the control circuit. It is not the purpose of this paper to develop a new control strategy for Power Factor correction but to demonstrate that the proposed single switch boost converter can be utilized to provide Power Factor control and harmonic reduction. As it was intended to demonstrate the use of the new boost converter for Power Factor correction, the control circuit is implemented in the open loop. To operate the circuit in the open loop, an external dc source is connected at pin#7 of the chip to regulate the output voltage at the desired level. By varying the voltage at pin#7, desired output voltage can be maintained.

V. EXPERIMENTAL RESULTS

The new boost converter with the following specifications is implemented and used as a power factor corrector.

V_{in}= 25V rms

V_{out}=40V

P_{out}=40W; f_s=100KHz; L =0.5 μH ; C_f= 2.2mF; MOSFET: IRF840; Diodes: MBR10100

$$L_f > \frac{R_{load}}{2f_s}\left[\frac{1}{2\dfrac{V^2_{out}}{V^2_{inpeak}}}\right] \Rightarrow L_f = 220\mu H$$

Fig.6 shows the waveforms of the input voltage and the input current of the bridge rectifier without any Power Factor correction. It can be seen that the input current is highly distorted due to the charging of the output capacitor during the period when the input voltage is less than the capacitor voltage. Fig.7 shows the waveforms after Power Factor is implemented. The input current is made to track the sinusoidal programming signal as closely as possible by the average control technique, and therefore, the input current is sinusoidal and is in phase with the input voltage. The total harmonic distortion from the bridge rectifier was 63% and it was reduced to 6.7% when Power Factor control was implemented.

VI. CONCLUDING REMARKS.

An ideal switching conditions for any switch would be at ZVS-ZCS. The switching losses comprises of (a) capacitive turn-on loss, (b) loss due to overlapping of current and voltage at turn-on and (c)turn-off loss. Part (a) is always present in a switch experiencing zero-current switching, whereas this loss is completely absent in a switch experiencing ZVS. However, to eliminate the capacitive turn-on loss in the main switch, additional switch is used to create ZVS condition for the main switch. The irony is that this switch would experience the same loss which it intended to eliminate in the first place. The additional switch along with the accompanying gate driving circuits do not improve the switching conditions of the converter. The present paper concentrated on eliminating the dominating part (b) of the turn-on loss using minimum number of components without compromising the soft-switching conditions for the diodes as well as the ZCS for the active switch. The paper once again stresses on the fact that two switch topologies will be

meaningful only when the capacitive turn-on loss is completely eliminated.

The advantages of the proposed single switch converter when used as a Power Factor controller are:

1) Low current and voltage stress of the switch. The maximum current stress is equal to the input current while the maximum voltage stress is equal to the output voltage.
2) A dedicated chip can be used to provide the control signals.
3) Simple control circuit on account of constant frequency of operation using only one switch.
4) The turn-on of the switch is characterized by zero-current switching.
5) soft-switching for the diodes.

Limitation:

The switch suffers from turn-off loss, and the topology is non isolated.

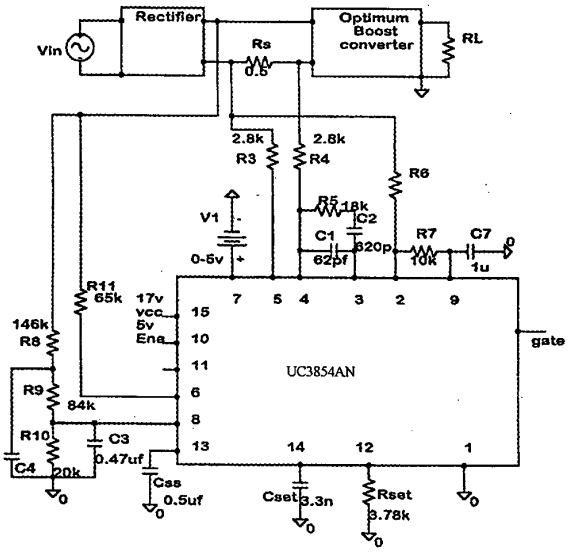

Fig.5 Schematics of Power factor correction using the New converter

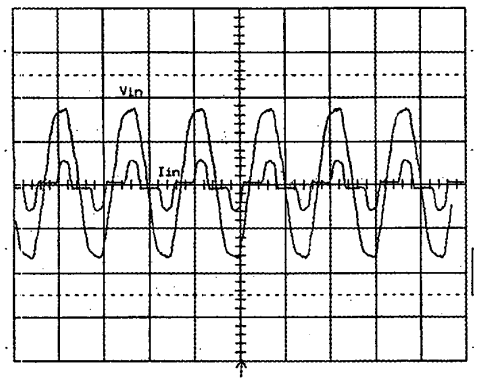

Fig.6 Input current and Input voltage
Without power factor correction

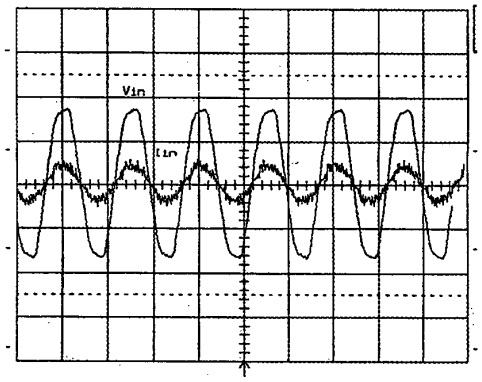

Fig.7 Input current and Input voltage
after power factor correction

Voltage: 20V/div; current: 5A/div

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ACKNOWLEDGEMENT

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APPENDIX.

Functional description of UC3854AN.

The figure below depicts the schematic diagram of the chip UC3854AN used in the average control of Power factor controller in the paper.

Pin#1: Ground:

Pin#2: PKLMT: The function of this pin is to disable the circuit in case the input current exceeds the maximum value. The chip will be disabled when this pin is driven below zero.

Pin#3: CA out: (current amplifier output). This is the output of the wide-bandwidth current error amplifier. The signal at this pin is compared with a ramp signal in a comparator to adjust the duty-cycle.

Pin#4: ISENSE: (current sense negative). This is the inverting input of the current error amplifier. This pin is connected externally to the ground point of the sensing resitor.

Analog multipler: The multiplier has three inputs (#6,#7 and #8) and one output (#5).

Pin#6: IAC: (input ac current) This forms one of the inputs to the analog multiplier. This pin is connected to the positive end of the rectifier through an external resistor and the input to this pin is a half wave sinusoidal current signal. This pin is used to sense the instantaneous input voltage.

Pin#7: VA out. (voltage amplifier output). This is the output of the voltage error amplifier and the function of this pin is to regulate the output voltage. This pin is the second input to the analog multiplier.

Pin#8: Vrms: (feed forward pin). UC3854AN is designed to operate for the universal input voltage range. (85V ac in US and 255V ac in Europe). This is implemented by keeping the input power constant with varying line voltage. A signal proportional to the RMS value of the input voltage is applied at pin#8 and then sqared before applying to the third terminal of the analog multiplier.

Pin#5: MULT out: (multiplier output and current sense positive). The positive terminal of the error amplifier and the output of the analog multiplier are internally connected to this pin. A resistor is connected externally from this pin to the other end of the sensing resistor, therefore, pin#5 is the summing point of the multiplier output current and a current proportional to the inductor current. The output of the multiplier is given by: $(\text{pin}\#6) * (\text{pin}\#7) / (\text{pin}\#8)^2$.

Therefore, the output of the multiplier at pin#5 is a current that increases with the current at pin#6 and the voltage at pin#7, and decreases with the square of the voltage at pin#8. The multiplier output will have the half sine wave shape and forms the programming signal for current shaping.

Pin#9: REF: (voltage reference output). The voltage at this pin internally maintained at 7.5V.

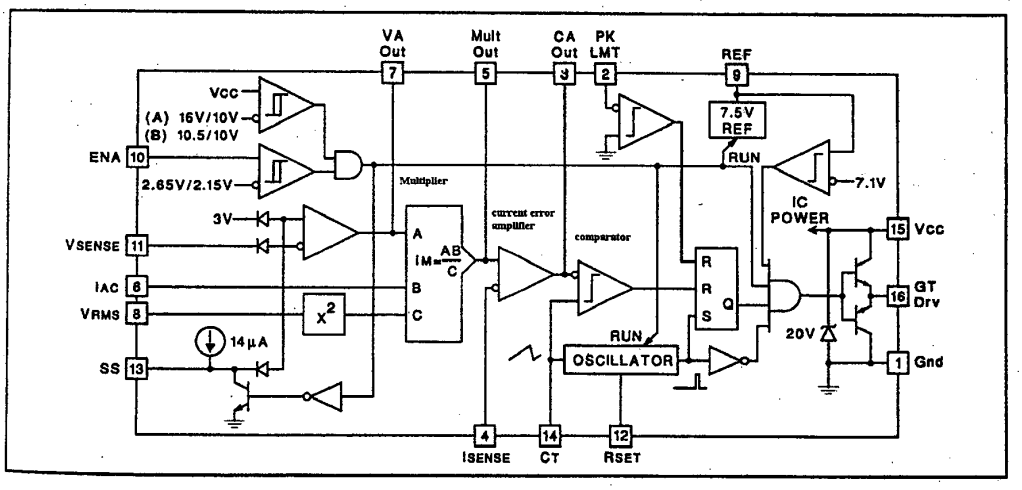
Pin#10: ENA: (enable) The chip will be enabled only when the voltage at this pin reaches 5V.

Pin#11: Vsense: (voltage amplifier inverting input). The output voltage of the boost converter is fed to this pin through a voltage divider to regulate the output voltage.

Pin#12: Rset and Pin# 14: Cset: These are the external components to set the frequency of the PWM oscillator.

Pin#13: SS: (soft-start). A capacitor is connected from this pin to the ground to increase the duty ratio slowly.

Pin#15: Vcc: (positive supply voltage) A supply voltage of above 17V is connected to this pin to power the chip.



UC3854AN. Courtesy: Unitrode product and applications handbook 95-96