A Novel Bridgeless Buck-Boost PFC Converter

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***Abstract*—Conventional cascade buck-boost PFC (CBB-PFC) converter suffers from the high conduction loss in the input rectifier bridge. To resolve the above problem, a novel bridgeless buck-boost PFC topology is proposed in this paper. The proposed PFC converter which removes the input rectifier bridge has three conduction semiconductors at every moment. Comparing with CBB-PFC topology, the proposed topology reduces the conduction semiconductors, reduces conduction losses effectively, improves the efficiency of converter and is suitable for use in the wide input voltage range. In this paper, the average current mode control was implemented with UC3854, the theoretical analysis and design of detection circuits was presented. The experimental prototype with 400V/600W output and line input voltage range from 220VAC to 380VAC was built. Experimental results show that the proposed converter can improve 0.8% efficiency comparing CBB-PFC converter.**

I. INTRODUCTION

Boost PFC converter generates a high voltage stress (>1000V) in the wide input voltage range of adjustable electronic equipments, especially in high voltage input condition. Therefore, it is very difficult to choose the components and energy storage capacitor of later-stage isolated converter [1]. In order to obtain appropriate bus voltage, PFC converters with the capability of providing both step-up and step-down topologies have been proposed. The CBB-PFC converter is shown in Fig. 1. Comparing with the popular boost PFC converter, CBB-PFC converter can even deliver an output voltage lower than the peak of the input voltage. Thus, the maximum device voltage stress in CBB-PFC converter is always lower than that in the Boost PFC converter. In addition, the inrush current problem that occurs in the boost PFC at start-up can be avoided in the CBB-PFC converter [2-5].

However, CBB-PFC converter consists of bridge rectifier and buck-boost converter, and has four conduction semiconductors at every moment. Thus, with the increase of power rating, the conduction loss of converter will increase rapidly. In this paper, a novel bridgeless buck-boost PFC converter is proposed as shown in Fig. 2. Without the input rectifier bridge, bridgeless buck-boost PFC converter has three conduction semiconductors at every moment, and efficiency is improved significantly. Through theoretical analysis, common mode noise of bridgeless buck-boost PFC converter is the same as that of CBB-PFC converter.

Recently, average current mode control is widely applied in PFC circuit [6]. The control method achieves near unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage. Average current mode control maintains stable, low distortion sinusoidal line current without the need for slope compensation, has the fixed switching frequency,

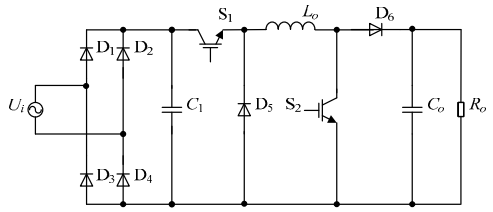


Figure 1. Cascade buck-boost PFC converter

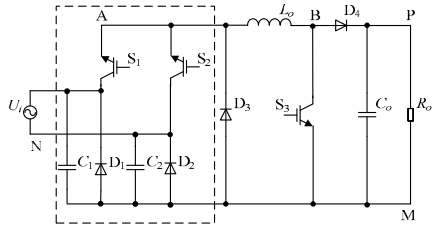


Figure 2. Proposed bridgeless buck-boost PFC converter

and is suited to high power occasions. In this paper, based on bridgeless buck-boost PFC topology, an average current mode control with voltage and current double closed-loop has been adopted, and UC3854 is used as the main control chip.

II. OPERATING PRINCIPLE

The equivalent circuits of bridgeless buck-boost PFC converter during the positive half cycle are shown in Fig.3. Driving signals of switch S_1 and S_2 are same. The operating principle of bridgeless buck-boost PFC converter during the positive half cycle can be described as follows:

When AC input voltage U_i is smaller than output voltage U_o, the converter operates in boost mode.

A. Boost Mode1[Fig. 3(a)]

During this stage, the switches S_1 and S_3 are conducting. Input voltage stores energy to inductor L_o. And the energy is transferred from capacitor C_o to the load.

B. Boost Mode2[Fig. 3(b)]

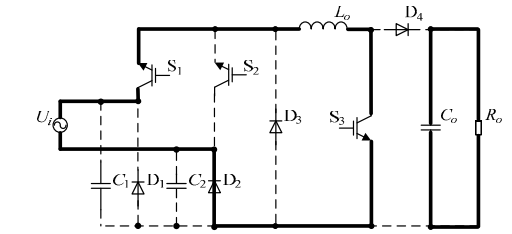
Switch S_3 is turned off. Input voltage and L_o provide power to the load. And energy stored in L_o reduces.

When AC input voltage U_i is larger than output voltage U_o, the converter operates in buck mode.

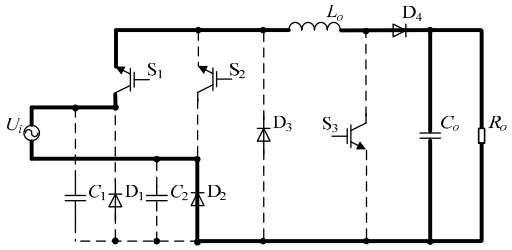
C. Buck Mode3[Fig. 3(c)]

Switch S_1 is turned on. Capacitor C_1 is discharged. Input voltage provides power to the load and inductor.

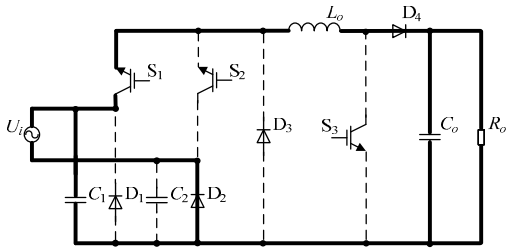
D. Buck Mode4[Fig. 3(d)]



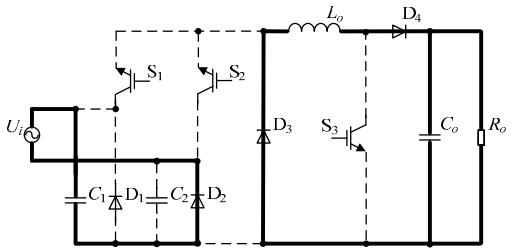
(a) Boost mode 1



(b) Boost mode 2



(c) Buck mode 3



(d) Buck mode 4

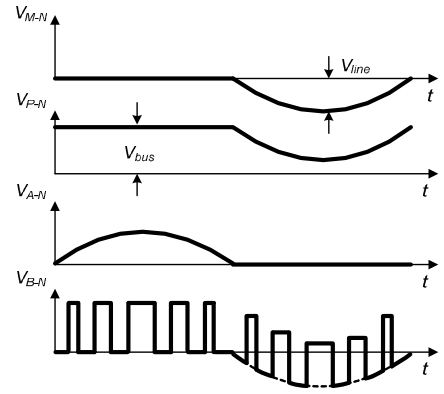
Figure 3. Equivalent circuit for each operation mode

When switch S_1 turns off, diode D_3 conducts. L_o provides power to the load. During this stage, capacitor C_1 is charged.

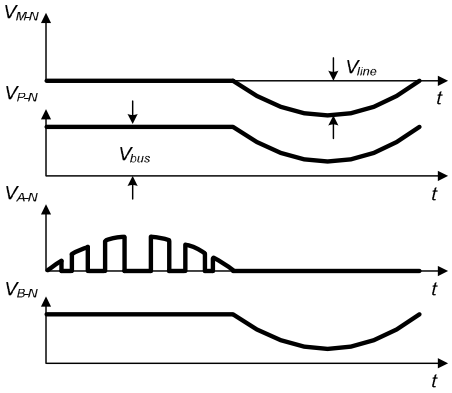
The operations during the negative half cycle are the same as the positive half cycle.

III. Comparison Between Bridge And Bridgeless Buck-Boost PFC Converter

According to the above analysis, Switches S_1 and S_3 should have a symmetrical blocking voltage characteristic. So, the RB-IGBT (Reverse Blocking IGBT) is used. It can block both forward and reverse voltage during its off state. Comparing IGBT with a series connected diode, elimination of the series diode helps to reduce losses by decreasing the on-state voltage across the switching element. The difference between the bridgeless buck-boost PFC and bridge buck-boost PFC is summarized in Table I. Comparing with bridge buck-boost PFC converter, bridgeless buck-boost PFC converter has one more switch



(a) Boost mode



(b) Buck mode

Figure 4. Voltage waveforms regarding neutral for bridgeless buck-boost PFC converter

and capacitor, two less slow diodes. However, comparing the conduction path of these two circuits, at every moment, three semiconductor devices are only conducting for bridgeless buck-boost PFC converter, but four semiconductors are conducting for bridge buck-boost PFC converter. Therefore, conduction loss can be reduced, especially in low line voltage. Theoretically, in one cycle of fundamental frequency, the saving power $P_{c,D}$ of bridgeless buck-boost PFC circuit can be given by

$$P_{c,D} = \frac{1.4\sqrt{2}P_o}{\pi\eta V_{rms}} \quad (1)$$

where P_o is output power, η is circuit efficiency, and V_{rms} is RMS value of the input voltage.

As to the EMI noise, Fig. 4 shows the voltage waveforms of M, P, A & B regarding input neutral for bridgeless buck-boost PFC converter. The M trace of DC bus is connected to neutral of AC input via bridge diodes D_1 and D_2. Therefore, there is no high frequency voltage transition at P and M, as shown in Fig. 2. CM noise of bridgeless buck-boost PFC is same as that of CBB- PFC.

IV. Control Strategy

In the application of PFC, average current mode control is widely applied. And it is also fit for bridgeless buck-boost PFC converter. In order to enable the circuit to operate properly in two modes, the cascade control method is adopted. It includes three steps. Step 1 is to control output voltage, and produce sinusoidal reference

TABLE I.
SUMMARY OF DIFFERENCES BETWEEN BRIDGE PFC AND BRIDGELESS PFC CONVERTERS

		Slow diode	Fast diode	Switch	Conduction semiconductor devices at every moment
Bridge buck-boost PFC converter	Boost mode 1	2	0	2	4
	Boost mode 2	2	1	1	4
	Buck mode 3	2	1	1	4
	Buck mode 4	2	2	0	4
Bridgeless buck-boost PFC converter	Boost mode 1	1	0	2	3
	Boost mode 2	1	1	1	3
	Buck mode 3	1	1	1	3
	Buck mode 4	1	2	0	3

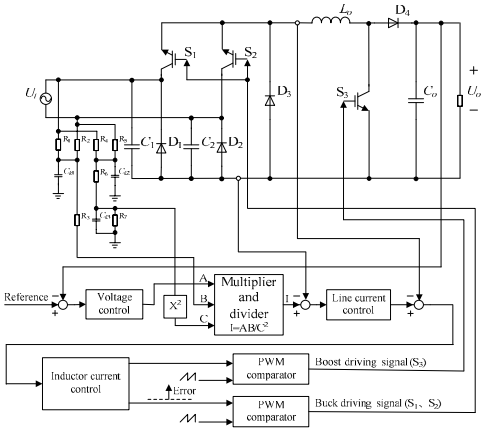


Figure 5. Control structure of bridgeless buck-boost PFC converter

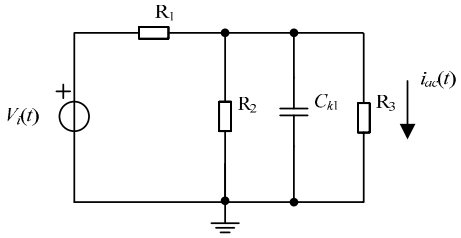


Figure 6. Input voltage sensing equivalent circuit

current signal through multiplier and divider; Step 2 is to control line current; Step 3 is to control inductor current. The control block diagram is shown in Fig. 5. To adapt to the current changes during operation modes conversion, two current-loops are used. Synchronously, input current waveform distortion can be reduced and power factor can be improved.

Because there is no input rectifier for bridgeless buck-boost PFC converter with average current control, it is difficult to sense the input voltage. A line frequency transformer is a simple solution for the voltage sensing. Due to the larger size of low frequency transformer and the cost issue, it is generally unacceptable for an efficient design. The optical coupler is also a good candidate for the voltage sensing, because it can easily achieve isolation. To achieve lower distortion of the voltage sensing, higher linearity optical coupler with wide operating range needs to be used, which is not practical and much more complex [7]. In this paper, a special resistor network for voltage sensing is applied.

UC3854 is used as control chip. The rectified input voltage is sensed by using a resistor network, and the mirrored signal is delivered to one of the multiplier's inputs (I_{AC}-pin6). The voltage sensing equivalent circuit is shown in Fig. 6.

The relation between input voltage V_i and the current that flows into I_{AC} pin is:

$$Y_{(S)} = \frac{1}{R_{eq}} \cdot \frac{1}{1+s\tau} \tag{2}$$

where

$$R_{eq} = R_1 + 2 \cdot R_3,\ \tau = \left(\frac{R_1}{2} // R_3\right) \cdot C_{k1},\ R_1 = R_2.$$

The net introduces one pole at: $f_p = \frac{1}{2 \cdot \pi \cdot \tau}$.

The pole must be located at a frequency high enough not to distort the input waveform and at the same time, low enough to switching frequency. In the application, the equivalent resistance R_{eq} is chosen, which fits well with the current amplifier design. Accordingly, R_1, R_2 and R_3 can be obtained.

The pole has been placed a decade before the switching frequency. Then C_{k1} can be obtained as determined by

$$C_{k1} = \frac{1}{2 \cdot \pi \cdot f_p \cdot \left(\frac{R_1}{2} // R_3\right)} \tag{3}$$

Voltage feed-forward, a useful function in wide range application, requires a DC voltage proportional to the RMS value of the input voltage. For the UC3854, this value must be from 1.4V to 4.5V so that it can mirror over a wide range. Voltage feed-forward equivalent circuit is shown in Fig. 7.

Defining H_{LP}(s) as transfer functions between the input voltage V_i and the voltage at the output of the filter V_{LP} (V_{RMS}-pin8). The following relation can be given by

$$H_{LP} = K_{LP} \frac{1}{(1+s\tau_1) \cdot (1+s\tau_2)} \tag{4}$$

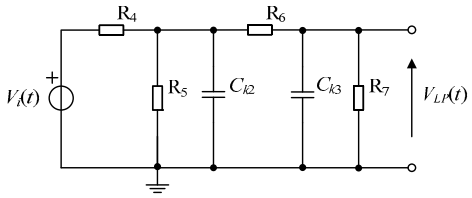


Figure 7. Voltage feed-forward equivalent circuit

where $K_{LP}=\dfrac{R_7}{R_4+2R_6+2R_7}$, $R_4=R_5$.

The time constants cannot be expressed in simple way so that the position of poles can be numerically calculated. The constant is defined taking into account the wide-range that is, RMS value of input voltage is between 200V and 415V:

$$V_{LP}=V_{RMS}\frac{2\sqrt{2}}{\pi}\cdot K_{LP} \tag{5}$$

This value can be chosen to calculate at the midpoint of the allowed values:

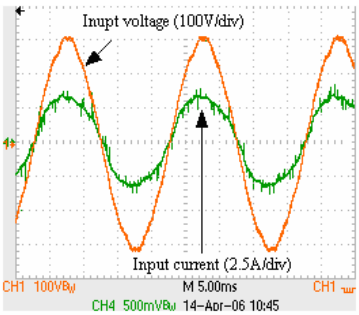
$$\frac{2\sqrt{2}}{\pi}\cdot\frac{200+415}{2}\cdot K_{LP}=\frac{1.4+4.5}{2} \tag{6}$$

Therefore, R_4, R_5, R_6 and R_7 can be obtained. Through choosing two poles frequency, capacitor C_{k2} and C_{k3} can also be obtained.

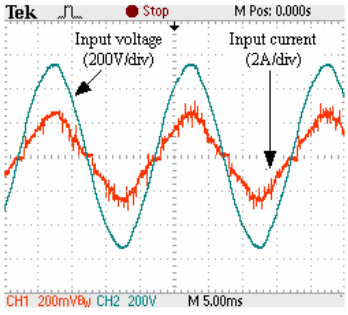
V. Experimental Results

To illustrate the feasibility, a 600W bridgeless buck-boost PFC converter prototype was built. The specifications of the experimental prototype are as follows:

Input voltage from 200V to 415V, output voltage V_o=400VDC, rated power P_o=600W, switching frequency f_s=50KHz.



(a) 220VAC input



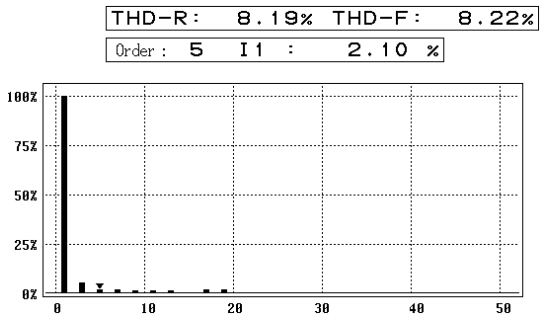
(b) 380VAC input

Figure 8. Input voltage and current waveforms

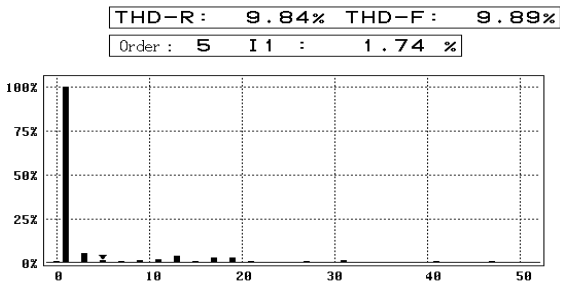
The input voltage and current waveforms at 220VAC and 380VAC are shown in Fig. 8. A high power can be achieved. With the increase of input voltage, input current decreases correspondingly, and input power maintains constant, which does not change while the input voltage changes.

THD and odd harmonic histogram at 220VAC and 380VAC input is shown in Fig. 9. High order harmonic is well restricted.

The relationship of input line voltage and power factor is shown in Fig. 10.



(a) 220VAC input



(b) 380VAC input

Figure 9. THD and odd harmonic histogram

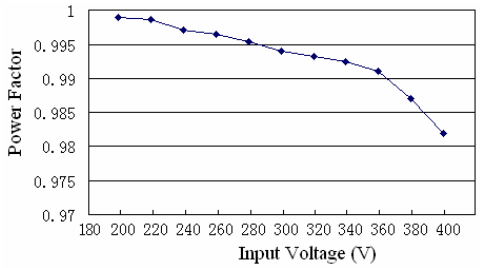


Figure 10. Relationship of input line voltage and power factor

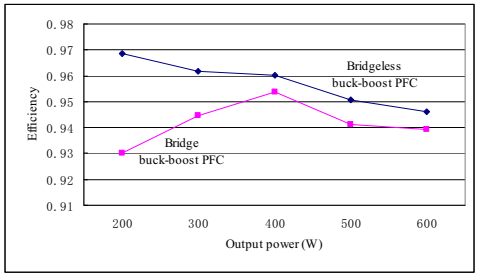


Figure 11. Efficiency of bridge and bridgeless buck-boost PFC converters

Efficiency of bridge and bridgeless buck-boost PFC converters is shown in Fig. 11. From this figure, it can be seen that the efficiency of bridgeless buck-boost PFC converter is higher than that of bridge buck-boost PFC converter. The results match well with the theoretical analysis.

VI. CONCLUSION

In this paper, a novel bridgeless buck-boost PFC topology is proposed. Without the input rectifier bridge, bridgeless buck-boost PFC converter has only three conduction semiconductors at every moment. Comparing with the CBB-PFC converter, the efficiency is increased. Power factor is more than 0.98, and THD is less than 10%.

ACKNOWLEDGMENT

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