Research and Design of High Power Factor Induction Motor Drive Based on *V/f* Control

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***Abstract*--This paper presented the design and implementation of an induction motor drive. In order to improve energy efficiency of this drive, system configuration comprised a single to three-phase converter with additional circuitry for PFC. In this design, using TI's UC3854 as the PFC controller chip, and the related parameters were designed. The control scheme was based on *V/f* control using two low-cost resistance current sensors. Only stator current measurements were needed to compensate for stator resistance drop. Regardless of changes in frequency or load, the magnitude of the stator flux can be constant by vectorially modifying the stator voltage. Furthermore, the hardware and software design were presented in detail. Experiments results showed that the proposed control system had high power factor and excellent performance.**

***Index Terms*--induction motor, PFC, *V/f* control**

I. INTRODUCTION

Owing to the nonlinear characteristics of rectifier diode and the influence of the capacitance of the filter, the current of AC supply has enormous harmonic components. It makes low power factor of conventional motor drive, seriously reduces energy conversion efficiency [1]. In order to reduce harmonic components, a boost circuit controlled by TI UC3854 was added between uncontrolled rectifier and three-phase bridge inverter in this paper. The related parameters of boost circuit and control circuit will be introduced in section Ⅱ. *V/f* control is preferred because of lower control costs for many applications, such as fans, pumps and compressors [2]. However, its practical application below a speed of 3 Hz is still challenging [3]. In order to resolve it, this paper presents a new *V/f* control with stator resistance compensation. The only measured quantity is the stator current. The stator resistance voltage drop is fully compensated for by vectorially adding it to the command voltage. The algorithm and software were carried on in section Ⅲ. And then this paper introduced simulation and experimental results in section Ⅳ to validate effectiveness of the proposed control system.

II. HARDWARE SYSTEM DESIGN

A. Hardware Block Diagram

The system hardware mainly includes power circuit, control circuit, switch power supply circuit and detection circuit. Power circuit mainly includes uncontrolled rectifier, boost PFC circuit and three-phase bridge inverter. Control circuit mainly includes PFC control chip peripheral circuit and microcontroller minimum system. Analog control chip UC3854 produced by TI was used as PFC controller. Infineon 32-bit microcontroller XMC1300 was used as the core controller to implements full-digital *V/f* control with stator resistance compensation. And almost of the protection function was achieved by software instead of hardware to reduce cost. The hardware block diagram was showed in figure1.

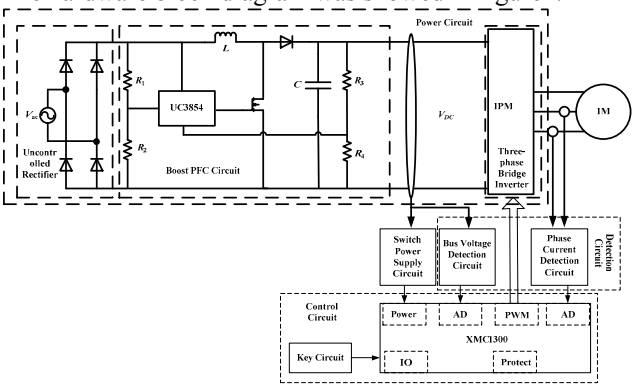

Fig.1 Hardware block diagram

B. PFC Circuit Design

In this paper, circuit design parameters were shown in table Ⅰ.

TABLE I
CIRCUIT DESIGN PARAMETERS

Output Power(KW)	4
DC Bus Voltage(V)	360
Switch Frequency(KHz)	30
Power Factor	≥0.85
DC Bus Voltage Ripple(V)	≤30

1) Inductor Selection

The inductor determines the amount of high frequency ripple current in the input and its value is chosen to give some specific value of ripple current. In this paper, ripple current is limited in 20% of the input peak current. So the inductor is given below:

$$L = \frac{V_{in} D_{\max}}{f_s \Delta I} \tag{1}$$

Where L is PFC inductor, V_{in} is peak voltage of input AC voltage, D_{max} is max duty factor of switch transistor, f_s is switch frequency, ΔI is ripple current.

The max duty factor is:

$$D_{\max} = \frac{V_o - V_{in}}{V_o} \tag{2}$$

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Where V_o is output DC bus voltage.

The input peak current is:

$$I_{peak} = \frac{\sqrt{2}P_{in}}{V_{in(\min)}} \tag{3}$$

Where I_{peak} is input peak current, P_{in} is input power, $V_{in(\min)}$ is minimum voltage of input AC voltage.

According to the above equation, induction value in this design selected 400μH.

2) Output Capacitor

The factors involved in the selection of the output capacitor are the switching frequency ripple current, the second harmonic ripple current, the DC output voltage, the output ripple voltage and the hold-up time. The output capacitance value can be represented as:

$$C_o = \frac{2 \times P_{out} \times \Delta t}{V_o^2 - V_{o(\min)}^2} \tag{4}$$

Where C_o is the output capacitor, P_{out} is output power, Δt is the hold-up time, in this design, hold-up time is selected as 1/2 period of the input AC voltage, is 10ms, $V_{o(\min)}$ is minimum output DC voltage.

According to the above equation, output capacitance value in this design is 1562μF, in practice, use three 680μF capacitors in parallel. The typical selection is 1 and 2μF per watt of output.

3) Voltage Loop Design

The voltage loop selected Ⅱ compensation circuit, was shown in figure 2.

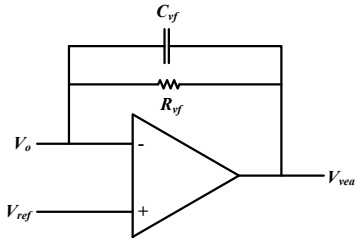

Fig.2 Voltage compensation circuit

The peak value of the second harmonic voltage is given by:

$$V_{o(pk)} = \frac{P_{in}}{2\pi f_r C_o V_o} \tag{5}$$

Where $V_{o(pk)}$ is the peak value of the output ripple voltage, f_r is the ripple frequency which is the second harmonic of the input voltage.

The ripple voltage at the output of the voltage loop must be limited in the specification for the converter, this need the gain of the voltage loop in second harmonic frequency is:

$$G_{va} = \frac{\Delta V_{vea} \times V_{ripple}}{V_{o(pk)}} \tag{6}$$

Where G_{va} is the gain of the voltage loop, ΔV_{vea} is the range of the voltage loop output voltage (4V on the UC3854), V_{ripple} is the design DC bus voltage ripple, in this paper, is 30V.

After get G_{va}, the feedback capacitor can be given as:

$$C_{vf} = \frac{1}{2\pi f_r R_{vi} G_{va}} \tag{7}$$

Where C_{vf} is the feedback capacitor of voltage loop, R_{vi} is the input resistance, it must be large enough so that the power dissipation is small, in this paper, choose 510K.

The pole frequency of the voltage loop can be represented as:

$$f_{vi}^{\ 2} = \frac{P_{in}}{\Delta V_{vao} V_o R_{vi} C_o C_{vf} (2\pi)^2} \tag{8}$$

So the feedback resistance can be given as:

$$R_{vf} = \frac{1}{2\pi f_{vi} C_{vf}} \tag{9}$$

The feedback resistance R_{vf} can be obtained as 51.8K, in practice, choose 51K. In real design, C_{vf} could influence dynamic response of PFC circuit. So we can choose a smaller C_{vf}, but make f_{vi} constant to get faster output voltage dynamic response. It can resolve output voltage surge in design.

4) Current Loop Design

The current loop must be compensated for stable operation. Current compensation circuit was shown in figure3.

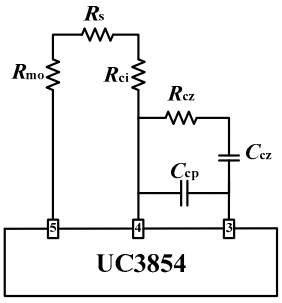

Fig.3 Current compensation circuit

The gain of the current loop near the switching frequency is determined by matching the down slope of the inductor current when the switch is off with the slope of the ramp generated by the oscillator. The voltage ripple in current sense resistor R_s is:

$$\Delta V_{rs} = \frac{V_o R_s}{L\omega_s} \tag{10}$$

Where ΔV_{rs} is voltage ripple in current sense resistor R_s, R_s is current sense resistor, ω_s is angular switching frequency.

The gain of the current loop is:

$$G_{ca} = \frac{V_s}{\Delta V_{rs}} \tag{11}$$

Where G_{ca} is gain of the current loop, V_s is the peak to peak amplitude of the oscillator ramp, is 5.2V in UC3854.

The feedback resistor is:

$$R_{cz} = G_{ca} R_{ci} \tag{12}$$

Where R_{cz} is feedback resistor of current loop.

The crossover frequency of current loop is:

$$f_{ci} = \frac{V_o R_s R_{cz}}{V_s 2\pi L R_{ci}} \tag{13}$$

Where f_{ci} is crossover frequency of current loop, the placement of the zero in the current error amplifier response must be at or below the crossover frequency. If the zero is lower in frequency the phase margin will be greater. This design selected f_{ci} is 15.9KHz, so G_{ca} is 31.25, select R_{ci} = 240Ω, then R_{cz} is 7.5KΩ.

The capacitor C_{cz} can be represented as:

$$C_{cz} = \frac{1}{2\pi f_{ci} R_{cz}} \tag{14}$$

Substituting relating parameters obtained, C_{cz} can be obtained as 6.2nF. In there, the design of PFC circuit parameters was finished.

III. V/F CONTROL WITH RESISTANCE COMPENSATION

A. Control System Structure

The whole control structure of this system is shown in figure 4. The control system is mainly composed of two parts: conventional *V/f* control and resistance compensation loop. Conventional *V/f* control is the base of the control system. The computation efforts of the control system and the dependence on the parameters of induction motor could be greatly reduced with varying the voltage as the frequency proportionally. Resistance compensation loop could make the magnitude of stator flux constant by adding stator resistance voltage drop to the command voltage. The only measurement needed is the stator current.

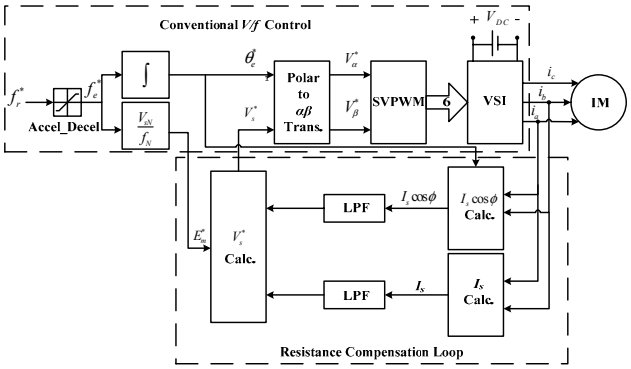

Fig.4 *V/f* control with resistance compensation structure

B. Voltage Control Method

The steady-state vector diagram of the asynchronous motor was shown in figure 5.

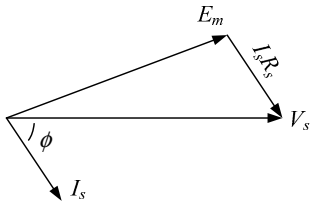

Fig.5 Steady-state vector diagram of the asynchronous motor

According to the law of cosines, V_s can be obtained as:

$$V_s = I_s R_s \cos\phi + \sqrt{E_m^2 - \left(I_s R_s \sin\phi\right)^2} \tag{15}$$

Where V_s is stator voltage vector, I_s is stator current vector, R_s is stator resistor per phase, E_m is voltage vector induced by stator flux, ϕ is power factor angle.

In this paper, it is necessary to make stator flux stable, then E_m can be represented as:

$$E_m = \frac{f^*}{f_N} E_N \tag{16}$$

Where f^* is target frequency, f_N is rated frequency, E_N is rated voltage. f_N and E_N can be obtained from nameplate of motor.

Substituting formula (16) into (15), another expression of V_s is:

$$V_s = I_s R_s \cos\phi + \sqrt{\left(\frac{f^*}{f_N} \times E_N\right)^2 + \left(I_s R_s \cos\phi\right)^2 - \left(I_s R_s\right)^2} \tag{17}$$

Stator current vector I_s can be obtained by stator phase current as:

$$I_s = \sqrt{i_\alpha^2 + i_\beta^2} = \sqrt{i_{as}^2 + \frac{1}{3} \times \left(i_{as} + 2 \times i_{bs}\right)^2} \tag{18}$$

Where i_α i_β are stator current components in stationary α β reference frame, i_{as} i_{bs} are stator phase current measured by two low-cost resistance current sensors. In this way, the instantaneous stator current I_s can be used for over current protection after a filter. An average filter and a low pass filter can be selected to eliminate sample noise in case of the over current protection misoperation.

The term $I_s cos\phi$ in (17) is the stator current vector component along with the stator voltage vector. By transforming the measured phase currents to the stator voltage fixed reference frame this term can instantaneously be calculated as:

$$I_s \cos\phi = \frac{2}{3}\left[i_{as}\cos\theta_e + i_{bs}\cos\left(\theta_e - \frac{2}{3}\pi\right) - \left(i_{as} + i_{bs}\right)\cos\left(\theta_e + \frac{2}{3}\pi\right)\right] = \frac{2}{\sqrt{3}}\left[i_{as}\cos\left(\theta_e - \frac{\pi}{6}\right) + i_{bs}\sin\theta_e \right] \tag{19}$$

Where θ_e is the position of the voltage vector in the stationary reference frame. In software, it was obtained by target frequency integration. The term "sinθ_e" and "cosθ_e" were obtained by looking up table. The control structure was shown in resistance compensation structure of figure 4. Two low pass filters (LPF) were used to eliminate the high frequency ripples in the calculated currents I_s and $I_s cos\phi$. In practice, the cut-off frequency of these filters was selected 100 Hz.

C. Control Program Design

According to the control strategy mentioned above, the control program consisted of main program, period interrupt program, fault interrupt program. The main program included initialization of variable, detection of start/stop and protection program. The period interrupt program was the realization of control strategy. It mainly included current sampling values obtaining, stator voltage calculation, target frequency integration and SVPWM module calculation. The moment of current sampling is PWM one match, because the low mosfets of three-phase bridge inverter were all open in this time. Two phase current sensor resistors were connected to the low mosfets of three-phase bridge inverter, only when low mosfets were open, the current sensor resistors flowed current. In this moment, motor phase current can be sampled by this hardware. The moment of current sampling shown in figure 6.

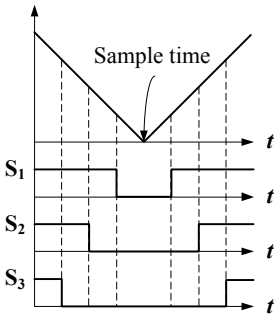

Fig.6 Current sampling time

During motor starting, the target frequency increased linearly, the starting time can be set in the program, but this term cannot be set too small, if not the inverter will occur over current protection. In the same, if motor stopping used this way, the stopping time cannot be set too small, because too small stopping time will make output capacitor charging, then output capacitor will breakdown because of over voltage. The fault interrupt program is a hardware protection, if the "FO" pin in hardware become low level from high level, it was necessary to set both PWM pin passive state and show "over current" to user.

IV. Simulation and Experimental Results

A. Power Factor Analysis

The Saber simulation results of PFC Circuit under 4KW load was shown in figure 7. The load resistor value selected 32.4Ω. In this figure, input current had same phase with input voltage. Input current sinusoidal distortion was high. The output DC voltage ripple was under 15V.

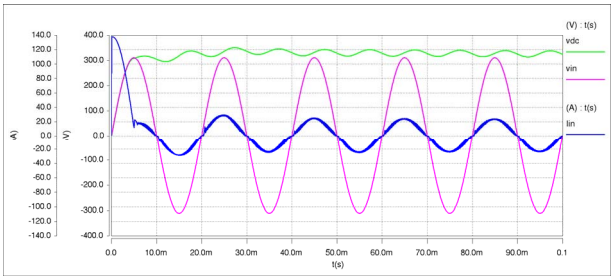

Fig.7 Simulation result of PFC under 4 KW

In order to get power factor, the harmonic analysis of input current shown in figure 8. 1-20 harmonic spectrum of input current shown this figure. The total harmonic distortion of input current is 6.47%, input current lagged 6.42° of input voltage. So the power factor can be calculated as 0.992.

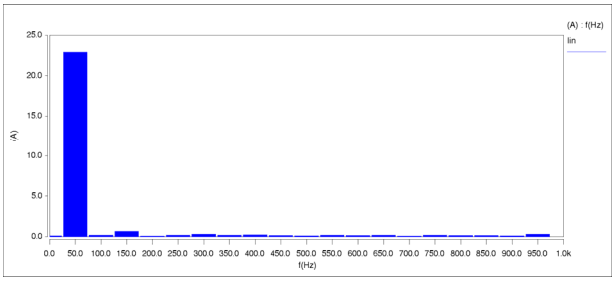

Fig.8 Harmonic spectrum of input current

In practice, a single phase inverter was designed to drive asynchronous motor. The rated power is 4KW. Conventional inverter used uncontrolled rectifier was tested to drive this asynchronous motor. The input current shown in figure 9. In this figure, input current distortion is serious, harmonic component is big. Import this oscilloscope sample data into Matlab to make FFT analysis. The total harmonic distortion of this input current is 138.66%, assuming that input current has same phase with input voltage. So the power factor is 0.58.

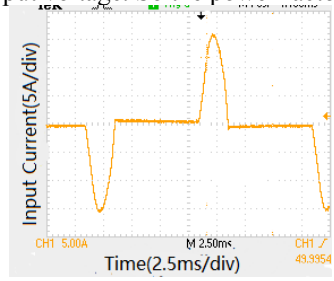

Fig.9 Input current in conventional inverter

Input voltage and input current shown in figure 10 when inverter with PFC drive this asynchronous motor at 3KW. In this figure, input current sinusoidal distortion was high and had the same phase with input voltage. Import this oscilloscope sample data into Matlab to make FFT analysis. The total harmonic distortion of this input current is 32.87%, power factor of this inverter is 0.95. Obviously, power factor greatly improved compared with conventional inverter.

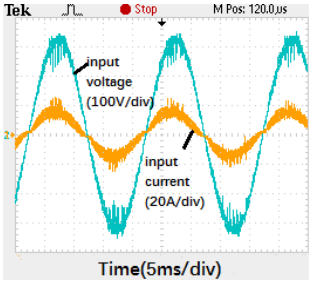

Fig.10 Input current in inverter with PFC

B. Motor Control Analysis

Asynchronous motor parameters used in this paper were presented in table Ⅱ.

TABLE Ⅱ
ASYNCHRONOUS MOTOR PARAMETERS

Rated speed n_N(r/min)	26444
Rated torque T_N (N • m)	0.5
Rated voltage V_N(V)	220
Rated current I_N (A)	30
Pole pairs p	1
Winding connection (Δ/Y)	Δ
Motor inertia J (kg • m^2)	3.39×10^{-3}

To validate the effectiveness of the voltage amplitude correction, the simulation is respectively conducted with or without the stator resistance compensation in low frequency. In there, selected 10Hz. In the simulation the frequency reference of motor starts from 0 to 10Hz in step. At t=1s a step rated torque T_L = 6N • m is applied. The figure11 and figure 12 demonstrate the simulation results of motor speed under two different control structure.

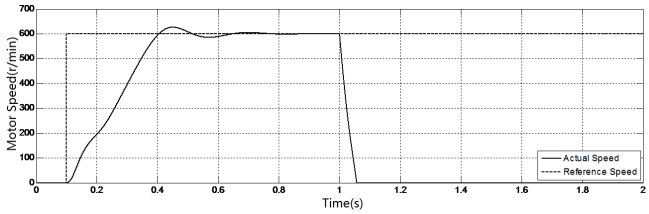

Fig.11 Motor speed of conventional *V/f* control in 10Hz

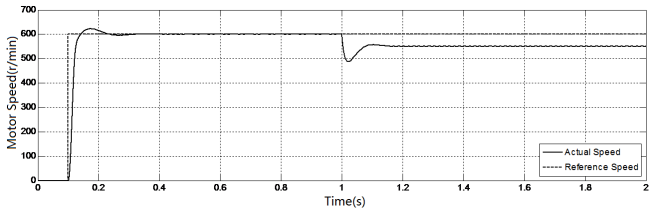

Fig.12 Motor speed of *V/f* control with stator resistance compensation in 10Hz

Compared with these two figures, *V/f* control with stator resistance compensation has better steady and dynamic performance than conventional *V/f* control. In specific, the starting time of first control scheme is 0.6s, the last one is 0.2s. The motor speed overshoot of these two control structures are almost equal, is 20 r/min (3.3% of target speed). So the last control structure has a better dynamic response. Conventional *V/f* control cannot drag the rated load in 10Hz, after a rated torque was applied in this motor, it was stopped in 0.05s. *V/f* control with stator resistance compensation can drag the rated load shown in figure 12, after a rated torque was applied in this motor, it stably operated in 550 r/min. The speed drop is almost 8.3%, stable time is 0.1s. So *V/f* control with stator resistance compensation a better steady response. The cut off frequencies of these two low pass filters were important for this proposed control algorithm. The cut off frequencies are too large will conduct motor speed ripples. And too small cut off frequencies will conduct long adjusting time. In this simulation, selected 100 Hz.

The related experiments also have been conducted to test the proposed structure. The microcontroller uses Infineon XMC1300 with 32MHz. Switching frequency and sampling frequency are same, selected 5KHz. Low pass filter cut off frequency selected 100 Hz. The experiment platform was shown in figure 13. From left to right, this four parts are respectively motor, power board, PFC circuit and control board.

Fig.13 The experiment platform

In order to test the speed control performance in the whole speed range. The stator phase currents at low speed, medium speed and high speed were shown in figure 14. Low speed, medium speed and high speed were respectively selected 50Hz, 200Hz and 450Hz. Figure 14 illustrates that peak and burr of stator currents in whole speed range are small and the degree of waveform sine are high. It demonstrates small torque ripple and excellent steady performance of the proposed control strategy.

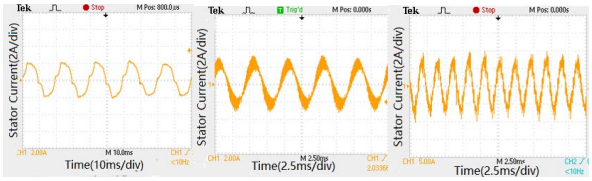

Fig.14 Stator phase current in whole speed range

V. Conclusion

This paper designed a high power factor induction motor drive, a PFC circuit controlled by TI's UC3854 was added to a single to three-phase converter. A *V/f* control including stator resistance drop compensation was also developed in this paper. Only two low-cost resistance current sensors were added in the hardware. So this design is suitable for low-cost and low dynamic response required applications, such as fans, pumps and electric tools. From the experiment and simulation analysis, this induction motor drive had a high power factor over 0.9 and an excellent speed control performance in the whole speed range.

Acknowledgment

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