Soft-Switching Single-Stage Current-Fed Full-Bridge Isolated Converter for High Power AC/DC Applications

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***Abstract*-- In this paper, a novel single-stage soft-switching current-fed full-bridge AC/DC converter is proposed. By adding an additional commutation path, soft-switching can be realized for all power devices. The power density is also enhanced by eliminating the DC capacitor. Meanwhile, the conduction loss is also lowered through the use of the additional commutation path. Furthermore, the control strategy for the proposed converter is compatible with that for traditional PFC converter. This facilitates the use of well-developed analog control IC such as UC3854. In this paper, the topology derivation and circuit operational analysis are given. The control strategy is introduced. A simulation is carried out to verify the circuit functionality.**

***Index Terms*-- AC-DC, PFC, Single stage, Soft-switching**

I. INTRODUCTION

For industry application where a large number of DC loads are installed such as telecommunication center or electrical vehicle charging station, AC/DC converters, also known as rectifiers, are the crucial parts which build the connection between the grid and the DC load networks. For the system where the power rating is over tens of watt, the power factor correction (PFC) function is required to save the electric energy and minimize the interference of power electronics converters to the grid [1-2]. In most of the utility interfaced applications, galvanic isolation is also required [3].

In practice, for power ratings above 1 kW, the multi-phase (or multi-pulse) rectifiers are cost-effective solution for this application. They shape the multi-phase ac voltages with the employing zigzag transformers [4]. The lower order input current harmonics are cancelled out by the superposition of the input currents in each phase. However, the transformers are working at the source line frequency. Therefore, they inevitably suffer from large volume. Moreover, the input currents are uncontrollable and the dynamic response is slow.

Instead of that, a two-stage system configuration based on power electronic converters, which consists of a front-end circuit stage with PFC function followed by an isolated DC-DC stage, is commonly employed [5-6]. Usually, the frond-end stage is composed by a diode rectifier bridge followed by a boost switch cell. Large DC link capacitors are also required between the two stages. There are several drawbacks of this two-stage solution. First, two-stage circuits are hard to achieve high efficiency since PFC stage is not easy to realize soft-switching. Meanwhile, the bulk decoupling capacitors in the dc link significantly increase the volume and cost [7].

Single stage AC-DC converters with isolation are advanced solutions which have higher power density and potentially can have higher efficiency. Several types of single stage solutions are developed for PFC applications. Non-bridge solutions such as flyback or sepic based topologies are popular in low power range [8-9]. However, the efficiency of these solutions is pretty low as the energy in leakage inductance is difficult to handle.

In higher power range, bridge type solutions are preferred. Depending on different types of DC link sources, these solutions can attribute to voltage source type and current source type. Usually, voltage source type converters eliminate the use of the boost cell in the PFC stage by simply combining the diode rectifier bridge and full-bridge DC-DC converter [10-12]. But the problem of these solutions is that a large volume of DC electrolytic capacitor is still required to form the DC link between the rectifier and the full bridge circuit, which limits the circuit performance. If the capacitance is decreased to be a very small volume [7], the DC link voltage will keep fluctuating with the input AC voltage. The soft-switching process of DC-DC stage will then become complex.

Current source type converter such as single-stage isolated current-fed full bridge converter should be more suitable for high power application because continuous input current [13-16]. But during the operation, when the input inductor and the leakage inductor of the transformer are connected together during the switching transient, high voltage spike will take place on switches. In order to clamp the over-voltage, complex active clamping circuit or passive snubbers have to be implemented. These also decrease the circuit efficiency.

In this paper, a novel single-stage soft-switching AC/DC topology is proposed. It is derived from current-fed full-bridge isolated converter. By adding an additional commutation path, soft-switching can be realized for all power devices. As there is no DC link capacitor, the power density is also enhanced. Meanwhile, the conduction loss is also lowered through the additional commutation path. Furthermore, the control strategy for the proposed converter is compatible with that for the traditional PFC converter. This facilitates the use of well-developed analog control IC such as UC3854. In this paper, the topology derivation and circuit operational analysis are given. The control strategy is introduced. A simulation is carried out to verify the circuit functionality.

II. PROPOSED CIRCUIT ANALYSIS

A. Topology derivation

The proposed topology is derived from current-fed full bridge DC-DC converter where the input source is replace by AC source with diode bridge rectifier, which is shown in Fig. 1(a). In order to clamp the voltage spike taken place when the input inductor L_{in} and high frequency transformer T_1 leakage inductor L_k are connected together, a capacitor C_r with tens of nF is added between the mid-points of two bridges. The derived circuit is shown in Fig. 1(b). But this circuit is hard to realize soft-switching since there is no additional commutation path. To solve this problem, an additional commutation path is added, which is formed by a Mosfet S_1 with a series-connected diode D_1. Two commutation inductors L_{r1} and L_{r2} are added to limit the *di/dt* during the commutation. The final version of the proposed topology is shown in Fig. 1(c). The new circuit is somehow similar with the traditional two-stage solution where the intermediate DC link capacitor is eliminated. $S_1(D_1)$ is the boost main switch, which conducts during the boost "on" time. All the other devices $S_2(D_2)$-$S_5(D_5)$, D_{o1}-D_{o4} composes the full-bridge circuit which operates during the boost "off" time. Half of the switches conduct during the "off" time to deliver the energy to the output and achieve high frequency isolation. The function of L_{r1} and L_{r2} are to realize ZCS turn-on and turn-off for all the switches. In the following section, the circuit operational principle and analysis are given to shown the operating principle of soft switching.

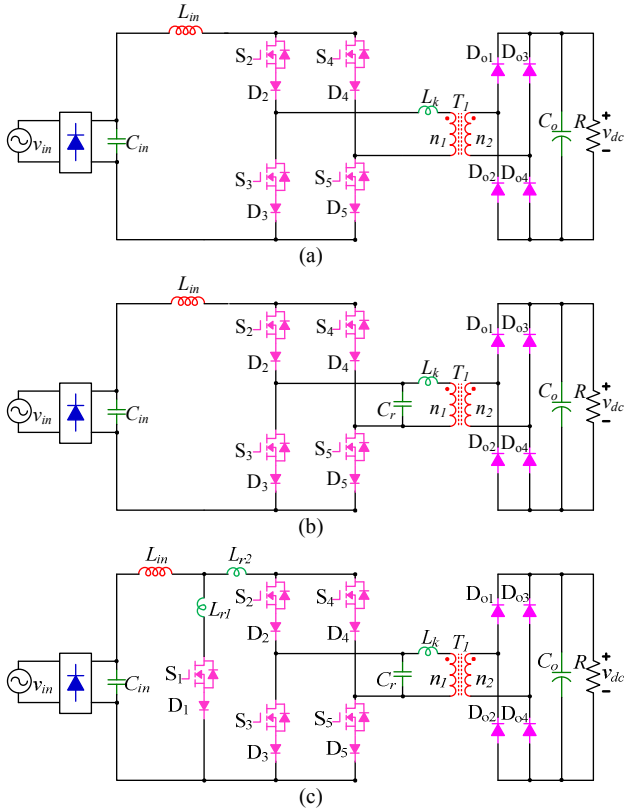


Fig. 1 Derivation of proposed converter (a) original current-fed full bridge AC-DC converter (b) improved form (c) final proposed converter

B. Circuit Operational Analysis

Firstly, one switching period can be divided into two symmetric sub-periods corresponding to positive and negative cycle of T_1. One sub-period is further divided into five stages. The positive cycle is taken as example to demonstrate the operation. The corresponding equivalent circuits are given in Fig. 2(a)-(f), the key waveforms are shown in Fig. 3. During the positive sub-period, it is assumed that the output DC voltage v_{dc} remains almost constant during one switching period.

Stage 0 [t_0-t_1]: The equivalent circuit of this stage is shown in Fig. 2(a). Before stage 1, S_2 and S_5 are in ON state, S_1, S_4 and S_3 are in OFF state. L_{in}, L_{r2} and L_k are connected together and discharged to the output. The main current thus decreases gradually. The capacitor voltage v_{Cr} is in steady state, which can be given by:

$$v_{Cr} = \frac{n_1}{n_2} v_{dc} \tag{1}$$

The voltages on S_1, S_3 and S_4 are equal to v_{Cr}.

Stage 1 [t_1-t_2]: The equivalent circuit of this stage is displayed in Fig. 2(b). At the time t_1, S_1 is turned on. C_r begins to resonant with both L_{r1}+L_{r2} and L_k. The current rising rate of S_1 is limited by L_{r1}, which shows that it is under ZCS turned on. Also, the current decreasing rate of D_2, D_5, S_2 and S_5 is limited by L_{r2}. This implies that they are all in ZCS condition. It is assumed that the energy in C_r is large enough compared to L_{r1}, L_{r2} and L_k, so v_{Cr} will keep almost constant during this stage. The commutation time which allows current changing from L_{r2} to L_{r1} can be calculated as:

$$t_{c1} \approx \frac{(L_{r1} + L_{r2}) i_{Lin}}{v_{Cr}} \tag{2}$$

Usually, the inductance of L_{r1}+L_{r2} are set to be rather small, thus t_{c1} is kept to be short as well. After current in L_{r2} decreases to zero and is reverse blocked by D_2 and D_5, S_2 and S_5 can be turned off at any time. The voltages on S_3, S_4, S_2 and S_5 change to half of v_{Cr}.

At the same time, C_r continues to resonant with L_k. The current in L_k decreases to zero at the time t_2. As the changing rate is limited by L_k, D_{o1} and D_{o4} are turned off in ZCS. The duration of stage 1 can approximately calculated by:

$$t_2 - t_1 \approx \frac{\pi}{2} \sqrt{L_k C_r} \tag{3}$$

Stage 3 [t_2-t_3]: In this stage, as shown in Fig. 2(c), only S_1 and D_1 are in ON state. L_{in} and L_{r1} are charged by v_{in}. This stage is equal to the "on" state of the boost PFC circuit.

Stage 4 [t_3-t_4]: At the time t_3, S_3 and S_4 are turned on simultaneously. C_r begins to resonant with L_{r1}+L_{r2} again. The current in L_{r1} begins to fall gradually to zero and reverse blocked by D_1. Thus S_1 and D_1 are turned off with ZCS. Also, the current increasing rate of S_3 and S_4 is limited by L_{r2}. It implies that they are in ZCS condition. Similar with stage 1, the duration of this stage, also is the commutation time, can be calculated as:

$$t_{c2} = t_4 - t_3 \approx \frac{(L_{r1} + L_{r2}) i_{Lin}}{v_{Cr}} \tag{4}$$

As the instant value of i_{Lin} changed between stage 1 and stage 3, t_{c1} and t_{c2} will not be equal. The equivalent circuit of this stage is displayed in Fig. 2(d).

Stage 4 [t_4-t_5]: In this stage, current in L_{r1} decreases to zero. S_1 can be turned off in this stage. C_r continues to be discharged by v_{in} through L_{in} and L_{r2}. v_{Cr} goes to negative finally. The equivalent circuit is shown in Fig. 2(f). It can be found that, during this interval, voltages on all the off-state switches are clamped by C_r. v_{Cr} and i_{Lin} follow the bellowing resonance equations:

$$i_{Lin} = I_{Lin0}\cos\left[\omega_r(t-t_3)\right] + \frac{v_{in}+v_{Cr}}{Z_r}\sin\left[\omega_r(t-t_3)\right] \quad (5)$$

$$v_{Cr} = -v_{in} + (v_{in}+V_{Cr0})\cos\left[\omega_r(t-t_3)\right] - Z_r I_{Lin0}\sin\left[\omega_r(t-t_3)\right] \quad (6)$$

Where ω_r and Z_r are given by:

$$\omega_r = \frac{1}{\sqrt{(L_{r2}+L_{in})C_r}}, \qquad Z_r = \sqrt{\frac{L_{r2}+L_{in}}{C_r}} \quad (7)$$

I_{Lin0} is the initial values of i_{Lin}, V_{Cr0} is almost equal to $v_{dc}\,n_1/n_2$. The duration of stage 3 and 4 can be calculated by using (6) where v_{Cr} is equal to $-v_{dc}\,n_1/n_2$.

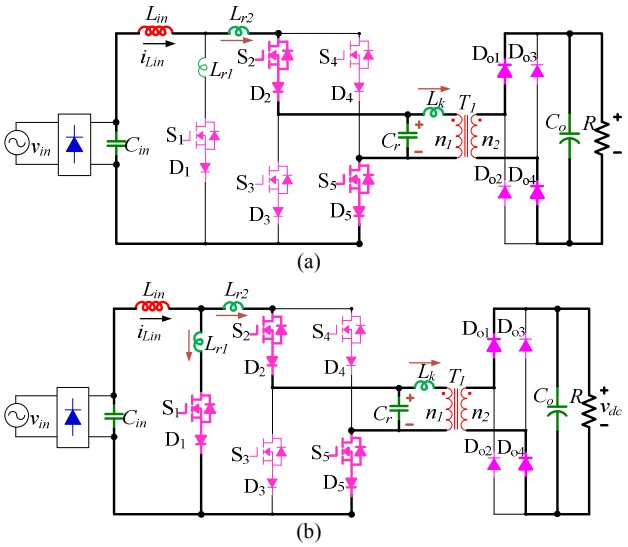
Stage 5 [t_5-t_6]: The equivalent circuit of this stage is shown in Fig. 2(g). After v_{Cr} falls below $-v_{dc}\,n_1/n_2$, D_{o2} and D_{o3} are turned on. C_r Begins to resonant with L_k. The maximum voltage overshoot will be:

$$\Delta v = I_{\text{Lin max}}\sqrt{\frac{L_k}{C_r}} \quad (8)$$

The maximum switch voltage on the primary side will be:

$$V_{switch} = \frac{n_1}{n_2}v_{dc} + I_{\text{Lin max}}\sqrt{\frac{L_k}{C_r}} \quad (9)$$

According to the analysis, all the switches are clamped to C_r during the operation. It can be inferred from (9) that keeping the inductance of L_k as small as possible can limit the over-voltage of v_{Cr} and limit the voltages on all the switches. This will also make the volume of C_r smaller.



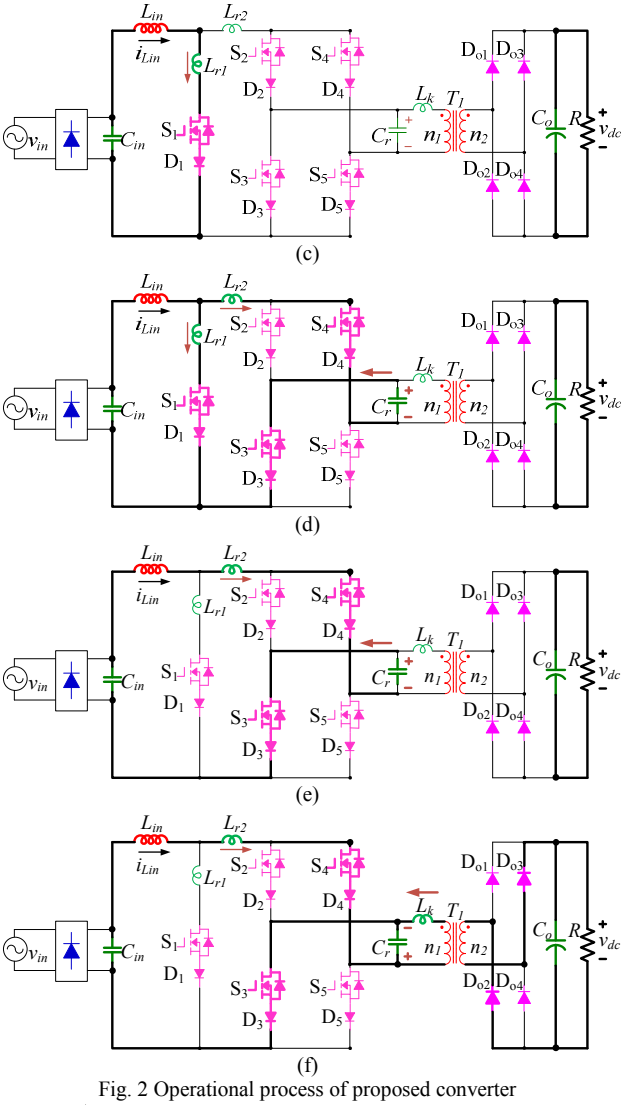


Fig. 2 Operational process of proposed converter

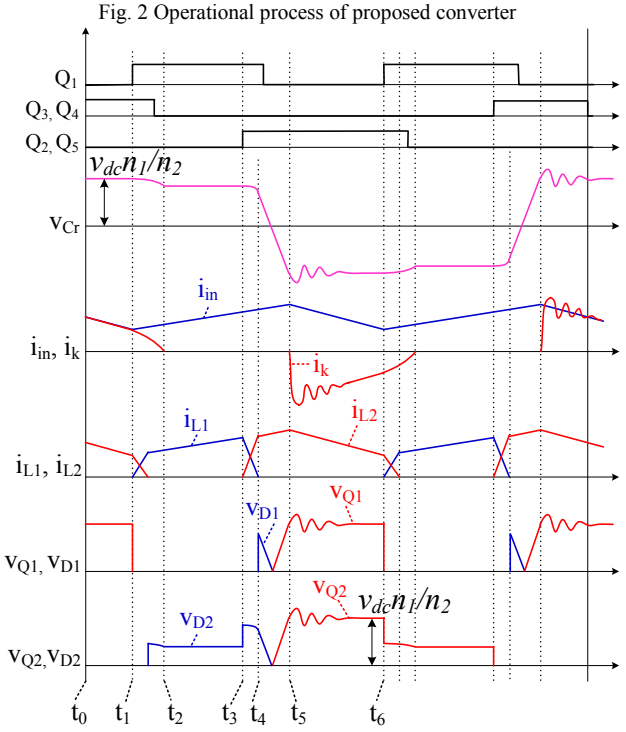


Fig. 3 operational waveforms for proposed converter

One positive sub-period is from stage 0 to stage 4., The negative sub-period begins with the stage 5 where S_1, S_2 and S_5 become active. The commutation process will be similar with the positive sub-period.

C. Soft-switching design criterion

According to the former analysis, there are three commutation stages in one sub-period, which are stage 1, stage 3 and stage 4. Minimum commutation time should be guaranteed.

For the stage 1 and 3, according to (2) and (4), the worst case takes place when input current i_{Lin} reach its maximum value. The inductance of L_{r1} and L_{r2} is set to be 100nH, thus these two intervals are very short compared to one switching period. During the gate signal generation, the realization method for these commutation time is to insert a common "ON" deadtime between the switching action of S_1 and S_x(x=2-5). The duration of this deadtime is given by:

$$t_{d1} = \frac{n_2(L_{r1} + L_{r2})i_{Lin\max}}{n_1 v_{dc}} \tag{10}$$

For the stage 4, minimum commutation time is set to ensure that v_{Cr} will become negative before S_1 is turned on again. According to (6), the worse case takes place during the AC voltage and current crossing zero. The maximum duration of the time is given by:

$$t_{d2} = \frac{\pi}{2}\sqrt{(L_{r2} + L_{in})C_r} \tag{11}$$

In order to realize this minimum commutation time, a maximum duty cycle limit which is no less than (11) is applied to S_1.

D. Decreasing of conduction loss

In addition to the minimization of switching loss due to soft-switching, the conduction loss of the proposed circuit is also decreased a lot. If traditional current-fed full bridge circuit shown in Fig. 1(a) is applied, six switches including two rectifier diodes always exist in the current path. As a result, the conduction loss should be larger than traditional two-stage solution. By adding the additional commutation path, only four switches exist in the current path during the boost "on" time. This decreases the conduction loss, which makes the proposed circuit have comparable conduction loss performance with the two-stage solution.

III. Control Strategy Explanation

The control strategy of the proposed PFC converter is fully compatible with traditional CCM PFC control. This control function is implemented to analog PFC control IC such as UC3854 [17]. Only an additional gate signal distribution block is required to generate the gating signals for all the switches. It only needs digital logic gates and flip-flop gates.

The additional gate signal distribution block is shown in Fig. 4. In this block, the generation of the gate signal is based on the original gating signal from PFC controller, which is represented by G_{pfc}. It is also the gate signal for S_1 after an off-delay is added. G_{pfc} is also sent to a J-K flip-flop gate to generate two complimentary square signals. These two square waves are "AND" with the complimentary wave of G_{pfc}. The two result signals are for S_2, S_5 and S_3, S_4 respectively after off-delays are added. The resultant gating pattern is demonstrated in Fig. 5. The frequency of G_{s1} is the same as the converter switching frequency. Frequencies of other switches are all divided by two as the using of J-K flip-flop gate. φ represents the common "ON" deadtime.

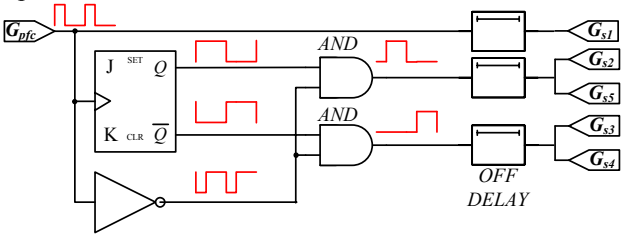


Fig. 4 Additional gating block implemented to proposed circuit

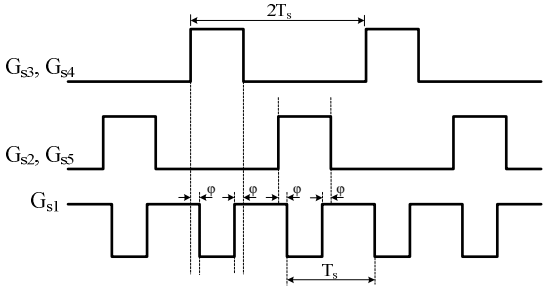


Fig. 5 gating pattern demonstration

IV. Simulation and Experiment

A simulation is carried out to verify the proposed circuit. An inductor L_{source} is added to the AC input voltage source to emulate the grid impedance. And a capacitor C_{filter} is added to represent the input filter. The value of all the components is given in TABLE I.

The design of main circuit components such as input inductor L_{in} and output capacitor C_o follows the common design process for traditional PFC front end stage. Commutation inductors L_{r1} and L_{r2} are set to 100nH. The leakage inductor L_k is defined by the manufacturer's performance. 0.005 p.u., or 0.68μH is selected for the simulation. According to these value, Clamping capacitor C_r is set to be 22nF to limit the voltage overshoot less than 100V under full load condition.

TABLE I Specification of Simulation for Proposed Circuit

Converter	Output power P_{out}	3kW
	Input AC voltage V_{in}	208V_{ac}
	Output DC voltage V_{dc}	540V_{dc}
	Switching frequency f_{sw}	100kHz
	Input inductor L_{in}	150μH
	Commutation inductor L_{r1}, L_{r2}	100nH
	Clamping capacitor C_r	22nF
	Leakage inductor L_k	0.68μH
	Turn ratio n_1:n_2	35:54
	Output capacitor C_o	2.2mF
	Switch voltage rating V_{switch}	650V
Grid	Source impedance L_{source}	100μH
	Grid filter capacitor C_{filter}	6.8μF

The simulation results are given in Fig. 6-Fig. 8. The key waveforms of the components in one complete switching period are shown in Fig. 6 and Fig. 7. It can be found that the waveforms in Fig. 6 when AC input

voltage is on the peak are similar with Fig. 3 shows. The soft switching performance of S_1 and S_2 do not display very clear due to the limitation of simulation step. But it can be inferred from the voltage waveforms of the two switches that they are all in soft-switching since no voltage spike take places during the switching transient. On the other hand, the spike of voltage ringing on C_r is also control to be lower than 500V, which is safe for all 650V switches.

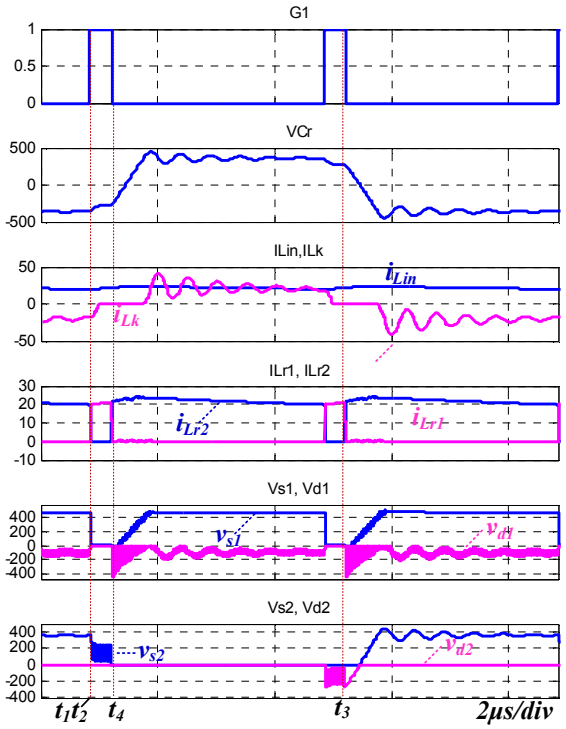


Fig. 6 Key waveforms in one switching period when AC input voltage is on the peak

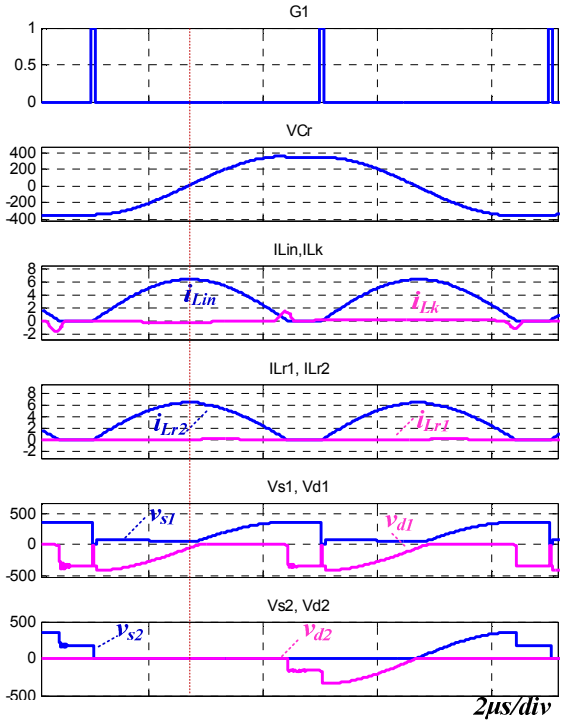


Fig. 7 Key waveforms in one switching period when AC input voltage is crossing zero

Fig. 7 shows the waveforms when AC input voltage is crossing zero. It can be found that the soft-switching is still realized even if the transformer current L_k and the input current I_{Lin} are all nearly zero. This is because that the V_{Cr} can be self reversed by resonance with L_{in}.

Fig. 8 shows the input and output waveforms of the AC-DC converter. The voltage waveform of v_{in} is scaled down to be the same level with input current i_{in}. It shows that the PFC function is almost realized. There are two problems with the input current. The first one is the zero-crossing distortion, which slightly increase the THD to 6.9%. This can be solved by further optimization. The second one is a tiny phase shift between the input voltage and the input current. This is because the AC voltage is sampled from the output of the diode bridge rectifier. The existing of the input capacitor filter causes this phase shift.

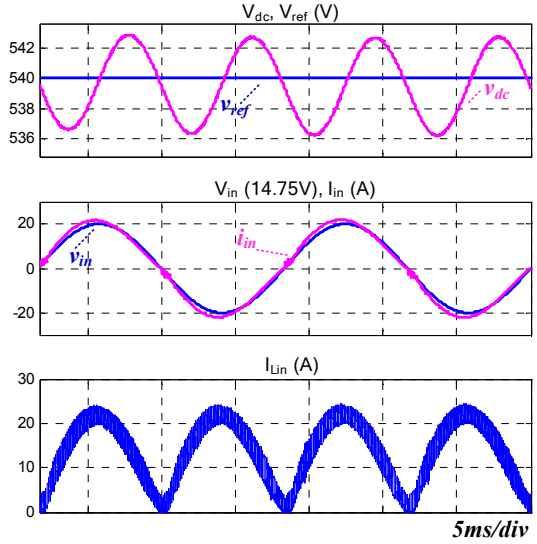


Fig. 8 Simulation waveforms for Input and output waveforms

V. Conclusions

Traditional isolated AC/DC converters always suffer from low power efficiency and low power density. In this paper, a novel single-stage soft-switching current-fed full-bridge AC/DC converter is proposed. By adding an additional commutation path, soft-switching can be realized for all power devices. The power density is also enhanced as there is no DC link capacitor. Meanwhile, the conduction loss is also lowered through the additional commutation path. Furthermore, the control strategy for the proposed converter is compatible with that for the traditional PFC converter. This facilitates the use of well-developed analog control IC such as UC3854. In this paper, the topology derivation and circuit operational analysis are given. The control strategy is introduced. A simulation is carried out to verify the circuit functionality. The results show that the converter can realize soft-switching for all switches, and the THD is lower than 6.9%.

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