Bridge PFC converter with split boost choke

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Abstract– **The paper presents a single-phase PFC converter built in the bridge configuration with split boost inductor placed on the AC side. The proposed topology enables decreasing of switching losses and limits the possible short circuit current through the transistor leg when its control signals temporary overlap. Both features make a construction of high power converters possible. In spite of an increased number of controllable power switches and the use of split choke, the converter's operation relies on a commercially available PFC controller (L4981). Due to the shifted pulses for the upper and the lower switches in the bridge the input current ripple and consequently the output voltage ripple are reduced.**
Based on a described principle an experimental model with nominal output power 1 kW has been built. Its functionality has been verified by measurements and harmonic analysis.

1 Introduction

Conventional AC/DC power supplies usually employ a full wave rectifier bridge with a smoothing capacitor, which introduce harmonic currents in the utility and decrease power factor. That is known as a harmonic pollution and reflects in a voltage distortion, heating and reduced transmission capability of the line. Distortion problem becomes more serious when the loads connected to the power supply become highly non-linear. This facts and the need to comply with the standards and recommendations [1] have forced the use of power factor correction circuits in power supplies.

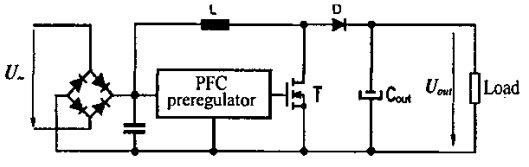


Figure 1. Basic topology of the PFC converter

Power factor can be significantly improved if power factor switching preregulator is placed between the input rectifier and smoothing capacitor (Fig.1). Regarding to the power stage of the preregulator, the boost converter is the most common used topology because of its advantageous: grounded transistor, small input inductor, simplicity and high efficiency. [2, 3] Switching at a frequency that is much higher than the line's one, the preregulator draws a sinusoidal input current that is in phase with the input line voltage. Regardless of the switching state, the current flows always through three silicon devices causing power dissipation and leading to the low efficiency of the PFC converter. As a result the topology seen in Fig.1 is convenient only for low power applications and for a middle output voltage range up to 450 V where the use of MOSFET switches are still feasible. At higher voltage and power levels IGBT transistors dominate despite of limited switching frequency that result in lower operating frequency of switches, bigger power stress on switches and higher current ripple.

All these disadvantages can be solved by a simple solution proposed by [4]. The author omitted the use of input bridge rectifier (Fig.2) by putting the choke into the AC side and doubling the boost stage.

As it is seen, the number of semiconductor devices that conduct current in the individual time instant, is reduced from three to two, resulting also in lower conduction losses. Besides, additional reduction of switching losses of individual switch is achieved, since each transistor is active only in one half-period of the line voltage.

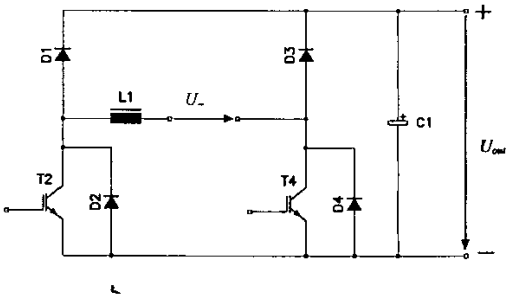


Figure 2. PFC converter with boost inductor on AC side

Further, since the choke inductor is placed into an AC side, its inductance can be reduced when it is preceded with an EMI filter. Comparing both solutions (Fig. 1, 2) there is no advantage considering the current ripple flowing in line conductor.

The current ripple and consequently the ripple of the output voltage can be essentially reduced, if the diode D1 and D3 from Fig. 2 are substituted by transistors. In this case, during the particular half-period of the input voltage, the sinusoidal shape of the input current is maintained by alternative switching of corresponding diagonal

transistors. As a consequence, the frequency of the current ripple is doubled compared to the switching frequency of the individual transistor. On the other hand, if we consider constant current ripple, the substitution of the D1 and D2 with the switches attains drastic reduction of the switching losses. The control logic is more complicated because it has to deliver pulses between the switches of the bridge and it has to prevent simultaneous conduction of the switches in the bridge leg.

2 Proposed topology

Considering all aforementioned facts, we propose a PFC converter with a modified bridge topology and split boost choke as it is seen in Fig. 3. Our goal was to reduce the current ripple and to avoid the use of sophisticated control logic at the same time. For that reason two additional half-bridge legs with the upper transistor are added into the bridge instead of substituting the diodes D_1 and D_3 (Fig. 2) with switches. The boost inductor is split into four windings. Each winding is connected to the particular bridge leg with one end and to the AC main with the other. The core of the windings can be either common in order to reduce the number of the components or the windings can be placed on separate cores. Since the achieved output voltage ripple is the most favourable, we decided for two separate inductors connected as it is shown in Fig. 3. Combination of windings L_1 and L_4 on one core and L_3, L_2 on the other offers an efficient protection of the bridge switches in case of pulse overlapping (T_1 and T_2 or T_3 and T_4 are switched on at the same time). Even though, the number of semiconductor devices of the proposed topology increased, only two semiconductor devices conduct and therefore two voltage drops exist at the individual time instant.

2.1 Basic operation concept

Diagonal switches T_2 and T_3 maintain the input current in one half period of the line voltage while in the other half period the T_1 and T_4 play an active role. Further, switches are triggered with pulses generated by the control logic, which are alternately delivered to one of the diagonal switch. This approach enables reducing thermal stress of the switches and doubles the switching frequency of the converter, which is twice as high as the switching frequency of the individual switch.

In subsequent lines a detailed analysis of operation is given. It is valid for a positive half-period when transistor T_2 and T_3 are alternately switched on and off. Their switching cycle can be divided into four intervals, which coincide with the particular operation mode (Fig. 5).

Mode 1: $t_0 < t < t_1$

In time interval $t_0 < t < t_1$ the switch T_2 is turned on. Current flows from the utility network through the inductor L_1-L_4, switch T_2 and diode D_4. As it is seen in Fig 4a, there flows no current through the other elements of the circuit. When converter operates in this operation mode, energy accumulates in the inductor L_1-L_4.

Mode 2: $t_1 < t < t_2$

Second operation mode starts at the instant t_1 when the switch T_2 is turned off. Due to the energy accumulated in the inductor L_1-L_4, the magnitude and the direction of inductor current remain unchanged. Since the T_2 is off and the voltage on the boost inductor L_1-L_4 raises the potential in A (Fig. 4b) above the U_{DC}, inductor current commutates from the T_2 into the circuit consisted of diode D_1, capacitor C and diode D_4.

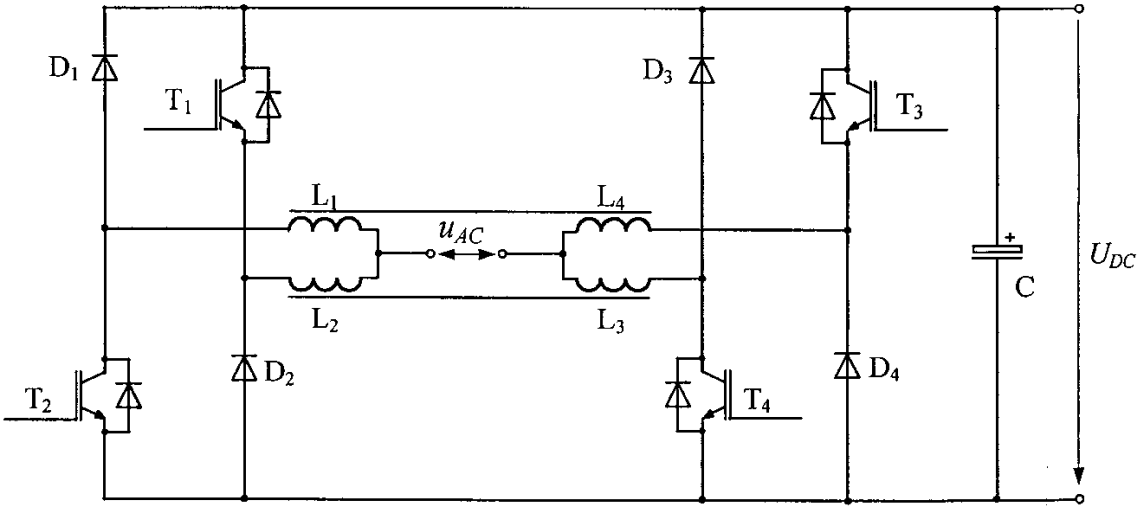
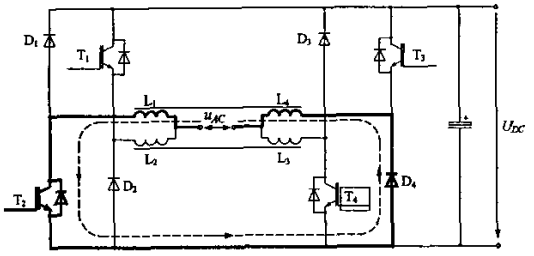
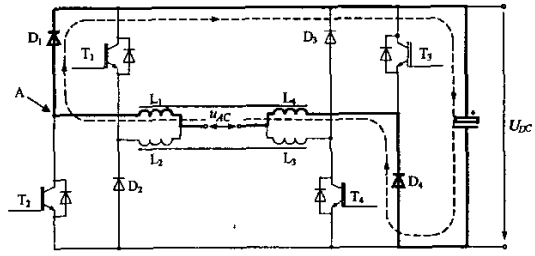


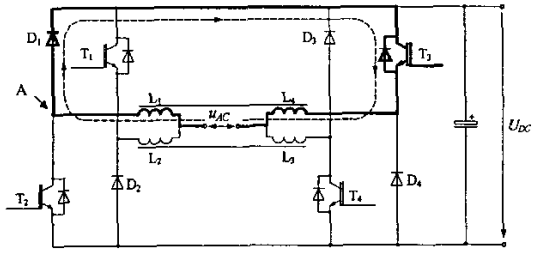
Figure 3. PFC converter with modified bridge topology and split boost choke



a) Mode 1



b) Mode 2, Mode 4



c) Mode 3

Figure 4. Modes of operation

The path of the current flow is shown in Fig. 4b. Energy, which was in previous interval stored in the boost inductor, is during this operation mode released into the output capacitor and load.

Mode 3: $t_2 < t < t_3$

In the instant t_2, triggering pulse u_{kr} is delivered to the T_3. Inductor current starts rising through the inductor L_1 - L_4, diode D_1, switch T_3 and diode D_4. As long as the switch T_3 is turned on, energy accumulates in the inductor. This state is similar to the second operation mode, with the exception that D_1 and T_3 play an active role, instead of T_2 and D_4. The circumstances in the circuit are shown in Fig. 4c.

Mode 4: $t_3 < t < t_4$

This operation mode starts at the instant t_3, when the T_3 is switched off and the accumulated energy releases into the load circuit. Current flows through the same components as in mode 2 (Fig. 4b) with the exception that the commutation process carries out between switch T_3 and diode D_4.

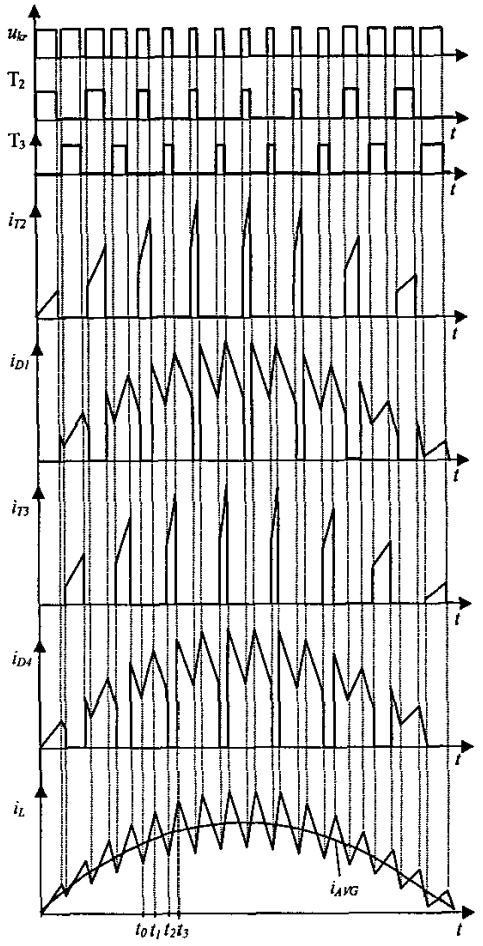


Figure 5. Main current waveforms

In negative half-period converter functions in the same way except that the role of active elements take over the inductor L_2-L_3, switch T_1, T_4 and diode D_2, D_3. If the trigger pulses drop out, the converter behaves as a well known diode rectifier.

As it has been mentioned before, one of the qualities of the proposed topology is also the short circuit protection in case of pulse overlapping. That state can occur at zero crossing of the line voltage (the upper and lower switches exchange the active role) when the duty cycle is nearly 1.

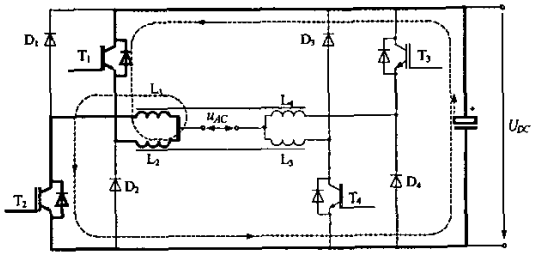


Figure 6. Short circuit protection in case of pulse overlapping

Since the switches have a finite turn off and turn on time, it is possible that the lower switch (T_2) turns on before the turning off of the corresponding upper switch (T_1). If that happens, the current, which is forced by the U_{DC} flowing through the upper and lower switch, is limited by the partial inductance of the L_1-L_4 and L_2-L_3 (Fig. 6).

2.2 Control circuit

To control the input current, a well-known average [5] current control method is used, which offers good input current waveforms especially near the zero crossing of the line voltage and operating with constant switching frequency. From a wide palette of commercially available control IC's for PFC applications, the L4981 from the SGS-Thompson [6] was selected and used in the experimental model. Since the controller is intended to drive single switch converters, in our case an additional logic circuit, which alternately delivers control pulses to the switches in the bridge, is necessary. The logic circuit has to be reliable with minimal time delay between its input and output. From the operation analyses of the proposed converter topology is obviously that the switches T_1 and T_3 as well as the T_2 and T_4 can be triggered synchronously. Moreover, due to the split inductor and its short circuit protection function, there is no need to interpose the dead time between the upper and lower triggering pulses. Regarding to the above-mentioned facts, the control logic and the logic for the distribution of the triggering pulses can be accomplished on a very simple way. Fig. 6 shows the pulse delivery circuit, which consists of JK-flip flop and an analogue dual switch. Due to the connection, the JK-flip flop behaves like a T-flip flop.

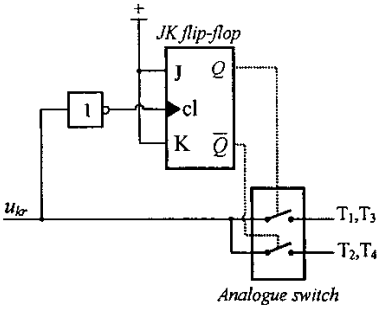


Figure 6. Pulse delivery logic circuit

The output signal u_{kr} from the control IC is connected to the input of the pulse delivery circuit. As the u_{kr} logic state changes from 1 to 0, the JK flip flop changes its output state and alternately triggers analogue switches. In this way, pulses from the control IC are alternately delivered to the upper and lower switches of the power stage. Since the particular analogue switch is turned on before the corresponding triggering pulse u_{kr}, the delay time of the analogue switch and flip-flop is avoided. Fig. 7 shows characteristic time waveforms of the pulse delivery circuit.

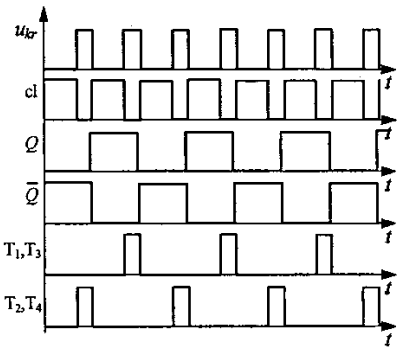


Figure7. Characteristic time waveforms of the pulse delivery logic circuit

3 Experimental results

A prototype PFC rectifier of nominal power 1 kW has been built to experimentally verify the analysis. The prototype operates in a continuous conduction mode (CCM) with average current control. Other rectifier specifications are:

Line voltage:	U_{AC} =150 V - 230 V
Output voltage:	U_{DC} = 400 V
Switching frequency:	f_{sw} = 80 kHz
Boost inductor:	L_1-L_4 = 450 μH L_2-L_3 = 450 μH

Fig. 8 and 9 show line voltage and current drown from the utility grid.

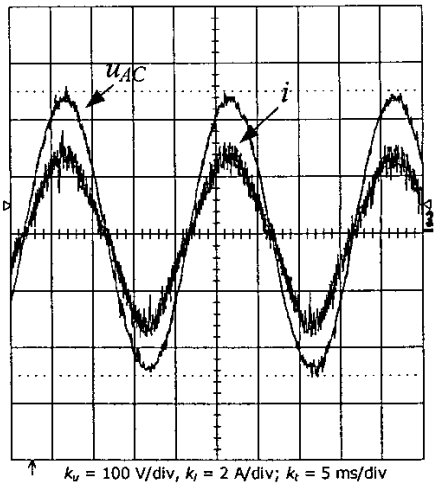


Figure 8. Line voltage and input current of the prototype rectifier

As it is seen, the current waveform authentically follows the line voltage, except in the range of voltage zero crossing, where despite of maximal duty cycle, the

energy stored in the boost inductor isn't sufficient. The current and voltage waveforms are almost in phase and the power factor is 0,98.

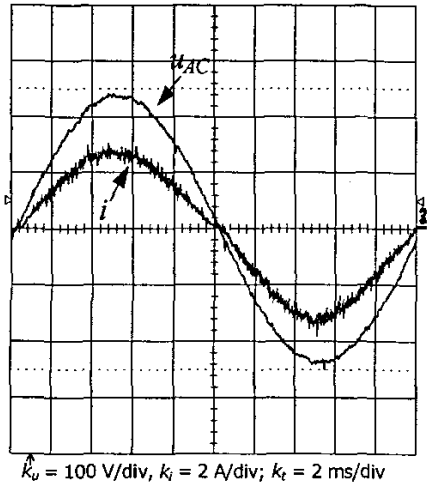


Figure 9. Line voltage and input current of the experimental model

Fig.10 shows the harmonic spectrum of the input current. Reasons for such amount of *THD* are the deformation of the current waveform around the zero crossing and the switching operating mode (the experimental model contains no EMI filter at its input).

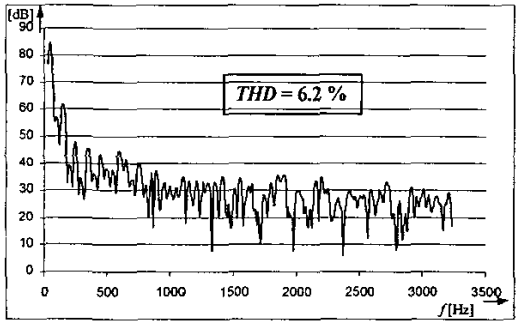


Figure 10. Harmonic spectrum of the input current

4 Conclusion

The paper presents a PFC converter based on a modified bridge topology, which is designed in order to reduce input current ripple and losses on the individual power switch without decreasing the simplicity of the control logic. To meet these goals, two additional transistors are added into the converter power stage that results in doubling the ripple frequency. In spite of an increased number of the controllable devices, we kept the control logic simple due to the applied split boost inductor. The latest dictates disposition of the additional transistors into an extra bridge legs with the intention to limit short circuit current in case of overlapping the triggering pulses. Since the upper transistor couple as the lower one can be triggered simultaneously and dead time interposing between the upper and lower triggering pulses is unnecessary, a very simple control circuit is feasible. Due to the described advantages of the proposed topology, a construction of high power converters (up to several kW) is possible. The results exceed the standard requirements and show the near unity power factor.

References

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