# Development of AC-DC Converter for Laboratory Power Amplifier

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***Abstract*—The purpose of the paper focuses on developing the power supply to feed the laboratory power amplifier. Such a power supply contains one boost converter with power factor correction (PFC), one multi-output two-transistor flyback converter with two other output voltages feeding the power amplifier and with two other output voltages feeding the peripheral circuit of this power supply. Regarding the control methods used herein, the boost converter is controlled by L6561, whereas the two-transistor flyback converter is controlled by UC3845. In this paper, the mathematical derivation is firstly introduced, and secondly some simulated and experimental results are provided to verify the effectiveness of the proposed topology.**

***Index Terms*—Isolated two-stage AC-DC converter, laboratory power amplifier.**

## I. INTRODUCTION

As generally known, the laboratory power amplifier is widely used in industrial applications, such as piezo drive. In general, the power supply to feed the power amplifier is the linear power supply [1]. And hence, there are many demerits existing in the linear power supply, such as large size, low efficiency, heavy weight, low PFC, high THD, etc. Therefore, in this paper, two converter are cascaded [2-5] as shown in Fig. 1, so as to reduce the voltage stress on the switch [6][7]. The first-stage converter, a boost converter, is used to perform power factor correction [8][9], whereas the second-stage converter, a two-transistor flyback converter, is used to execute isolation and multiple outputs [6] [7].

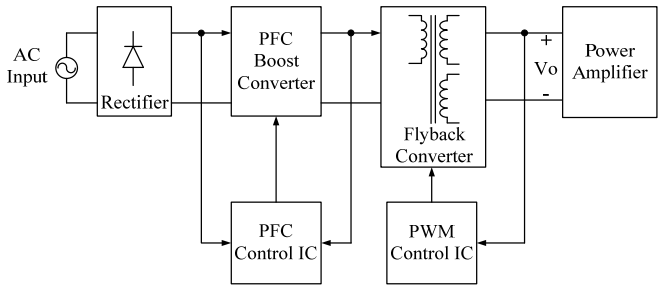


Fig. 1. Block diagram for two-stage-cascaded converter with PFC.

## II. TWO-STAGE CONVERTER CONFIGURATION

Fig. 2 shows the two-stage converter configuration. The first stage is the boost converter which is controlled by one control IC named L6561 made by ST Company and used to perform PFC. This control IC makes the boost converter operated in the critical mode (CRM) with variable switching frequencies. The voltage $V_{o1}$ sensed via the voltage divider built up by the resistors $R_1$ and $R_2$, the voltage $V_{in}$ sensed via the voltage divider established by the resistors $R_3$ and $R_4$, and the current sensed from the resistor $R_{s1}$ are sent to L6561 to generate proper pulse-width modulated (PWM) control signal to drive the switch $S_1$, so as to make the power factor as close to one as possible.

As for the second stage is the two-transistor flyback converter which is controlled by one control IC named UC3845 and used to obtain the positive and negative high voltages $V_{o2}$ and $V_{o3}$ to feed the power amplifier, and the positive and negative low voltage $V_{o4}$ and $V_{o5}$ to power the peripheral circuit. The control IC renders the two-transistor flyback converter operated in the discontinuous current mode (DCM). The voltage $V_{o2}$ sensed via the voltage divider constructed by the resistors $R_5$ and $R_6$, and the current sensed from the resistor $R_{s2}$ are both sent to UC3845 to create suitable PWM gate driving signals to drive $S_2$ and $S_3$, so as to stabilize $V_{o2}$ at the prescribed value.

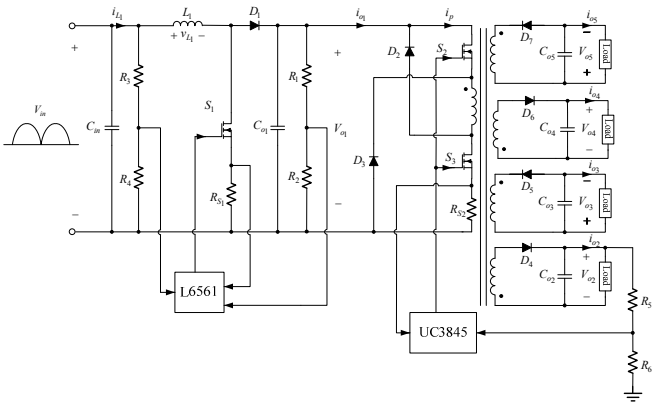


Fig. 2. Circuit for two-stage-cascaded converter with PFC.

## III. SYSTEM SPECIFICATIONS

Since the proposed converter is a two-stage-cascaded converter, the first stage is the boost converter and the second stage is the two-transistor flyback converter. The following tables are used to describe the specifications for individual converters. Table I is for the boost converter whereas Table II is for the two-transistor flyback converter.

TABLE I BOOST CONVERTER SPECIFICATIONS

| | |
|---|---|
| Input voltage | 85~265$V_{AC}$ |
| Output voltage | 400$V_{DC}$ |
| Rated output power ($P_{o1}$) | 90W |
| Switching frequency | 40kHz~100kHz |
| Operating mode | CRM |
| Input capacitance | 0.3μF |
| Input inductance | 702μH |
| Output capacitance | 20μF |

TABLE II FLYBACK CONVERTER SPECIFICATIONS

| | |
|---|---|
| Input voltage | 400$V_{DC}$ |
| Output voltage | ±300$V_{DC}$ , ±12$V_{DC}$ |
| Output power | 80W |
| Switching frequency | 100kHz |
| Operating mode | DCM |
| Input capacitance | 75μF |
| Primary inductance | 1.6mH |
| Output capacitance for $C_{o2}$, $C_{o3}$, $C_{o4}$, $C_{o5}$ | 75μF , 20μF , 20μF , 20μF |

## IV. DESIGN OF CONTROLLERS

In this paper, the state-space average technique is used to obtain the small-signal models required. Besides, by means of MATLAB/SISOTOOL, the suitable controllers can be found.

### *A. First-Stage Converter*

The first-stage converter is the boost converter, which is controlled by one PWM control IC named L6561. The corresponding small-signal block diagram is shown in Fig. 3. In order to obtain a high-power-factor value, the crossover frequency of the loop gain is set to 20Hz or less. Since the boost converter operates in CRM, the transfer function $G_3(s)$ for the variations in the output voltage $V_{o1}$ to variations in the peak value of the input inductance current $I_{L1\text{-}pk}$ can be expressed as

$$G_3(s)=\frac{dI_{L1\text{-}pk}}{dV_{o1}}=\frac{\sqrt{2}}{4}\cdot\frac{V_{in-rms}}{V_{o1}}\cdot\frac{R_{o1}}{1+s\cdot R_{o1}\cdot C_{o1}} \tag{1}$$

where $R_{o1}$ is the output resistance relevant to the rated output power $P_{o1}$ and $V_{in\text{-}rms}$ is the rms value of the input voltage $V_{in}$.

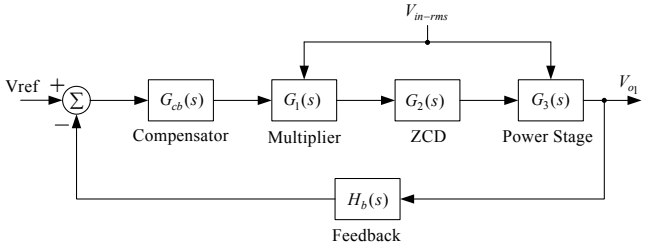


Fig. 3. Block diagram of closed-loop small-signal model for the first stage.

Also, the transfer function $G_1(s)$ for variations in the output voltage $V_{COMP}$ obtained from the compensator to variations in the peak value $V_{cs\text{-}pk}$ of the multiplier can be represented by

$$G_1(s)=\frac{dV_{cs-pk}}{dV_{COMP}}=K_M\cdot K_P\cdot\sqrt{2}\cdot V_{in-rms} \tag{2}$$

where $K_P$ is the resistance ratio of the input voltage divider and $K_M$ is the gain of the multiplier and can be expressed to be

$$K_M=0.651\cdot(1-85.29\cdot e^{-1.776\cdot V_{COMP}}) \tag{3}$$

where the quiet operating point for $V_{COMP}$ can be obtained to be

$$0=2.5+\frac{2\cdot P_{o1}\cdot R_s}{\eta\cdot K_M\cdot K_P\cdot V^2{}_{in-rms}}-V_{COMP} \tag{4}$$

where $\eta$ is the efficiency at the rated output power $P_{o1}$.

Besides, the transfer function $G_2(s)$ for variations in the peak value $V_{cs\text{-}pk}$ of the multiplier to variations in the peak value of the input inductance current $I_{L1\text{-}pk}$ can be represented by

$$G_2(s)=\frac{dI_{L_1-pk}}{dV_{cs-pk}}=\frac{1}{R_s} \tag{5}$$

Also, the feedback transfer function $H_b(s)$ is set to 1/160. Before the compensator $G_{cb}(s)$ is added, i.e., $G_{cb}(s)$ is equal to one, the uncompensated loop gain $T_{ub}(s)$ can be expressed as

$$T_{ub}(s)=\frac{1}{320}\cdot\frac{1}{R_s}\cdot\frac{K_M\cdot K_P\cdot V^2_{in-rms}}{V_{o1}}\cdot\frac{R_{o1}}{1+s\cdot C_{o1}\cdot R_{o1}} \tag{6}$$

Based on (6) and MATLAB/SISOTOOL, the suitable parameters for the compensator can be obtained, as shown in Fig. 4 with (7):

$$\begin{aligned}G_c(s)&=\frac{R_6}{R_1}\cdot\frac{1+s\cdot C_1\cdot R_5}{1+s\cdot C_1\cdot(R_5+R_6)}\\&=7.2177\cdot\frac{(1+0.04\cdot s)}{(1+34\cdot s)}\end{aligned} \tag{7}$$

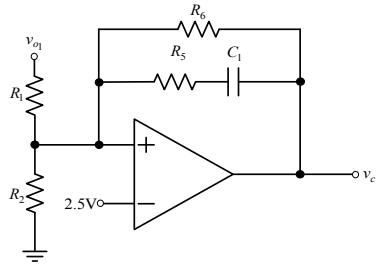


Fig. 4. Implementation of PI controller for $G_{cb}(s)$.

Therefore, the Bode plot shown in Fig. 5 is with the compensator added. It is obvious that the resulting corner frequency and phase margin with the compensator added are 18.8Hz and 80.8° respectively, which corresponds to the requirements of the system stabilization. Finally, based on MATLAB/SIMULINK, (6) and (7), the closed-loop system can be constructed, as shown in Fig. 6. Hence, Fig. 7 shows the resulting output voltage, about 395V close to 400V.

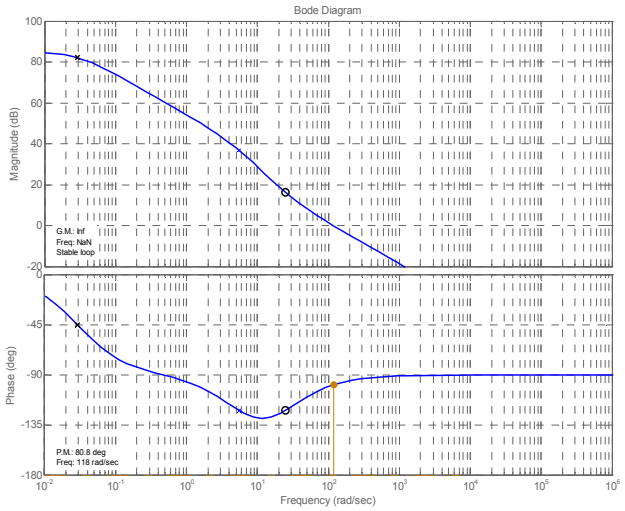


Fig. 5. Bode plot with the compensator added.

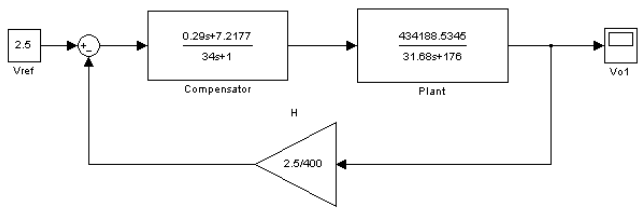


Fig. 6. Closed loop for the first stage constructed by MATLAB/SIMULINK.

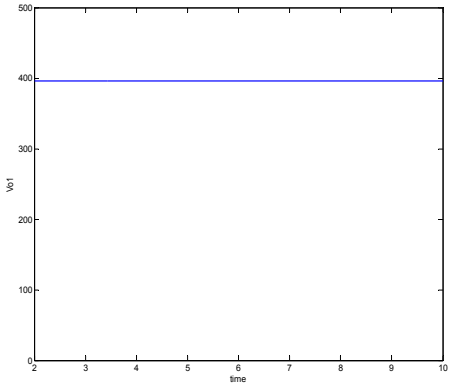


Fig. 7. Simulated closed-loop output voltage for the first stage.

*B. Second-Stage Converter*

Since the second-stage converter is the two-transistor flyback converter which is controlled by one PWM control IC named UC3842 and operates in DCM, there are three operating states. The corresponding small-signal block diagram is shown in Fig. 8. The average voltage across the primary of the transformer, $\langle v_{LP}(t)\rangle$, can be obtained via the second-voltage balance and can be expressed as

$$\langle v_{LP}(t)\rangle = d_a(t)\cdot\langle v_{o1}(t)\rangle_{Ts} - d_b(t)\cdot n\cdot\langle v_{o2}(t)\rangle_{Ts} + d_c(t)\cdot 0 = 0 \quad (8)$$

where $d_a(t)$ is the duration for state 1; $d_b(t)$ is the duration for state 2; $d_c(t)$ is the duration for state 3; $\langle v_{o1}(t)\rangle_{Ts}$ is the average output voltage per switching period for state 1; $\langle v_{o2}(t)\rangle_{Ts}$ is the average output voltage per switching period for state 2; $n$ is the turns ratio of $N_p$ to $N_s$, where $N_p$ is the number of turns at the primary and $N_s$ is the number of turns at the secondary. Hence, the duration for state 2, $d_b(t)$ can be expressed to be

$$d_b(t) = d_a(t)\cdot\frac{\langle v_{o1}(t)\rangle_{Ts}}{n\cdot\langle v_{o2}(t)\rangle_{Ts}} \quad (9)$$

where $d_c(t) = 1 - d_a(t) - d_b(t)$.

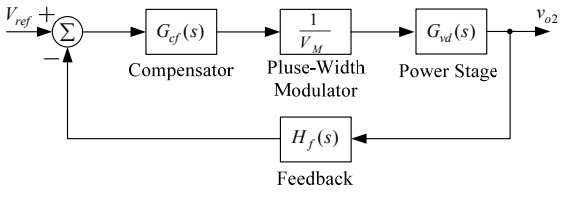


Fig. 8. Block diagram of closed-loop small-signal model for the first stage.

Via the voltage and current equations for the active and passive switch components, the large-signal model for the two-transistor flyback converter operating in DCM can be shown in Fig. 9. After perturbation and linearization of the input and output variables shown in Fig. 8, the small-signal model can be

obtained as shown in Fig. 10, with the following nodal equations:

$$\tilde{i}_{ds2} = \frac{v_{ds2}}{r_1} + j_1\tilde{d} + g_1 v_{d4} \tag{10}$$

$$\tilde{i}_{d4} = -\frac{\tilde{v}_{d4}}{r_2} + j_2\tilde{d} + g_2 v_{ds2} \tag{11}$$

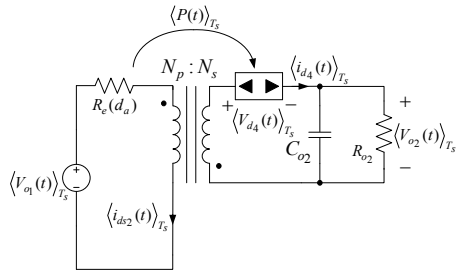


Fig. 9. Large-signal model for the second stage.

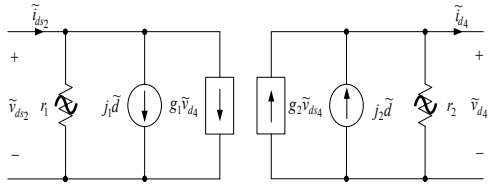


Fig. 10. Small-signal model for the second stage.

By means of Taylor's expansion, the parameters $r_1$, $j_1$, $r_2$, $j_2$ and $g_2$ can be obtained, and hence the control-to-output transfer function in Fig. 10 can be expressed to be

$$G_{vd}(s) = \left.\frac{\tilde{v}_{o2}}{\tilde{d}}\right|_{v_{o1}=0} = \frac{G_{d0}}{1+\dfrac{s}{\omega_p}} \tag{12}$$

where

$$G_{d0} = j_2 \cdot (R_{o2} \,//\, r_2) \tag{13}$$

$$\omega_p = \frac{1}{(R_{o2} \,//\, r_2)\cdot C_{o2}} \tag{14}$$

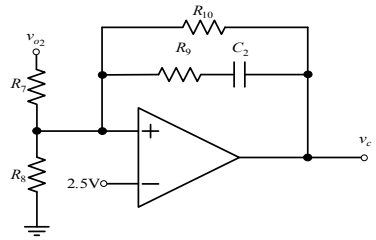


Fig. 11. Implementation of PI controller for $G_{cf}(s)$.

Also, the feedback transfer function $H_f(s)$ is set to 1/120. Before the compensator $G_{cf}(s)$ is added, i.e., $G_{cf}(s)$ is equal to one, the uncompensated loop gain $T_{uf}(s)$ can be expressed as

$$T_{uf}(s) = \frac{1}{120}\cdot\frac{1}{V_M}\cdot\frac{G_{do}}{1+\dfrac{s}{\omega_p}} \tag{15}$$

Based on (15) and MATLAB/SISOTOOL, the suitable parameters for the compensator can be obtained, as shown in Fig. 11 with (16):

$$\begin{aligned} G_c(s) &= \frac{sR_{10}}{R_7}\cdot\frac{1+s\cdot C_2\cdot R_9}{1+s\cdot C_2\cdot(R_9+R_{10})} \\ &= 26.694\cdot\frac{(1+0.0056\cdot s)}{(1+0.35\cdot s)} \end{aligned} \tag{16}$$

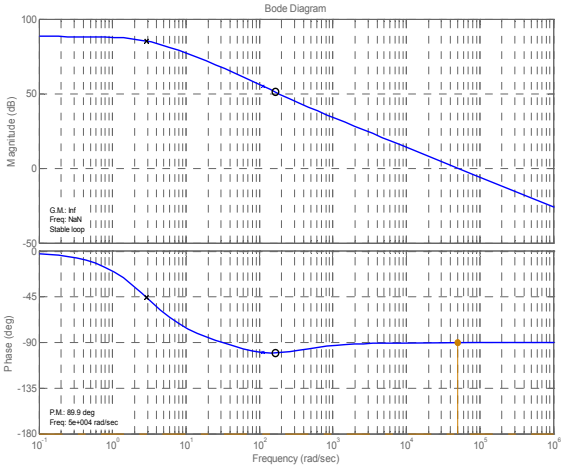


Fig. 12. Closed loop for the second stage constructed by MATLAB/SIMULINK.

Therefore, the Bode plot shown in Fig. 12 is with the compensator added. It is obvious that the resulting corner frequency and phase margin with the compensator added are 8kHz and 89.9° respectively, which corresponds to the requirements of the system stabilization. Finally, based on MATLAB/SIMULINK, and (15) and (16), the closed-loop system can be constructed, as shown in Fig. 13. Hence, Fig. 14 shows the resulting output voltage, about 300V.

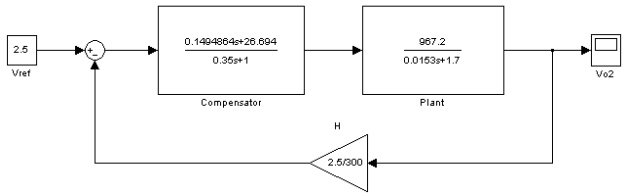


Fig. 13. Block diagram of closed-loop small-signal model for the second stage.

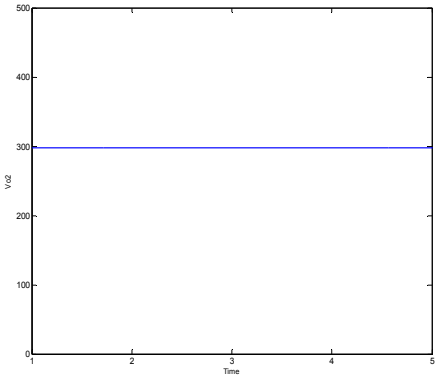


Fig. 14. Simulated closed-loop output voltage for the second stage.

## V. EXPERIMENTAL RESULTS

The following experimental results are used to verify the proposed two-stage converter to feed the laboratory power amplifier. First, the key waveforms are measured under the AC input voltage of $85V_{AC}$ and $265V_{AC}$ at the half and rated powers. After this, the proposed two-stage converter is applied to the laboratory power amplifier. Figs. 15 to 17 show the waveforms for the boost converter under the input voltage of $85V_{AC}$ at the half power. Fig. 15 shows the input voltage $v_{in}$ and the input current $i_{in}$; Fig. 16 shows the gate driving signal for $S_1$, $v_{gs1}$, the voltage across $S_1$, $v_{ds1}$, and the current flowing through $L_1$, $i_{L1}$; Fig. 17 displays the DC output voltage $V_{o1}$. Figs. 18 to 20 show the waveforms for the boost converter under the AC input voltage of $85V_{AC}$ at the rated power, and the items of waveforms for Figs. 18 to 20 are the same as those for Figs. 15 to 17.

On the other hand, Figs. 21 to 23 and Figs. 24 to 26 show the waveforms for the boost converter under the AC input voltage of $265V_{AC}$ at the half and rated powers, respectively. And, the items of waveforms for Figs. 21 to 23 and Figs. 24 to 26 are the same as those for Figs. 15 to 17. From the waveforms shown above, it is obvious that the first-stage converter can operate stably.

Sequentially, Figs. 27 to 29 show the waveforms for the two-transistor flyback converter at the half power. Fig. 27 shows the gate driving signal for $S_3$, $v_{ds3}$, and the current flowing through the primary winding, $i_p$; Fig. 28 shows the DC output voltage $V_{o2}$, the voltage across $D_4$, $v_{d4}$, and the current flowing through the secondary winding, $i_s$. Fig. 29 shows the DC output voltages, $V_{o2}$, $V_{o3}$, $V_{o4}$ and $V_{o5}$. On the other hand, Figs. 30 to 32 show the waveforms for the two-transistor flyback converter at the rated power, and the items of waveforms for Figs. 30 to 32 are the same as those for Figs. 27 to 29. From the waveforms shown above, it is obvious that the second-stage converter can operate stably. Besides, the resulting efficiencies and power factors are tabulated in Table III. From Table III, it can be seen that the higher the AC input voltage, the higher the efficiency and the less the power factor, whereas the more the output power, the lower the efficiency and the higher the power factor.

Eventually, the proposed two-stage converter is used to feed a laboratory power amplifier constructed by two-stage-cascaded amplifiers with individual scalings. One is controlled by OPA LT1358, and the other is controlled by OPA PA94. Figs. 33 and 34 are under the same input voltage signal of 5V with the amplification gain 1×10 and 2×10 respectively. From these results, it can be seen that the laboratory power amplifier fed by the proposed converter can operate stablly.

TABLE III MEASURED PF AND EFFICIENCY

| $V_{in}$ | $P_{in}$ | $P_{o2}$ | Eff. | PF |
|---|---|---|---|---|
| $85V_{AC}$ | 44W | 40W | 90% | 0.93 |
| $265V_{AC}$ | 43W | 40W | 93% | 0.88 |
| $85V_{AC}$ | 94W | 80W | 85% | 0.96 |
| $265V_{AC}$ | 90W | 80W | 89% | 0.94 |

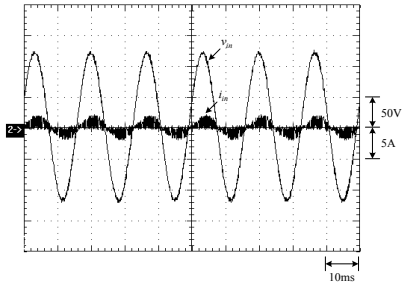


Fig. 15. Measured waveforms under input voltage of $85V_{AC}$ at half load for the first stage: (1) $v_{in}$; (2) $i_{in}$.

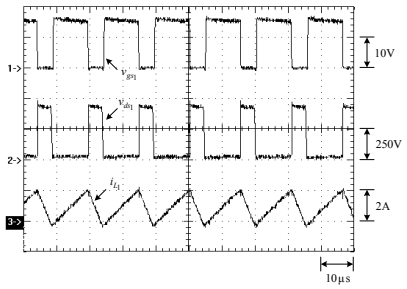


Fig. 16. Measured waveforms under input voltage of $85V_{AC}$ at half load for the first stage: (1) $v_{gs1}$; (2) $v_{ds1}$; (3) $i_{L1}$.

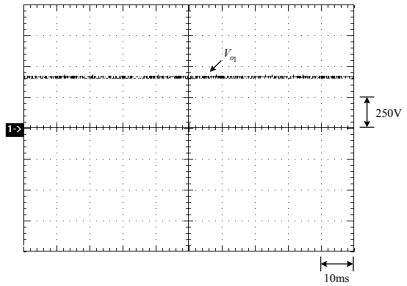


Fig. 17. Measured DC output voltage under input voltage of $85V_{AC}$ at half load for the first stage.

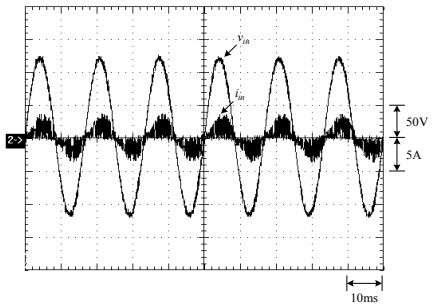


Fig. 18. Measured waveforms under input voltage of $85V_{AC}$ at rated load for the first stage: (1) $v_{in}$; (2) $i_{in}$.

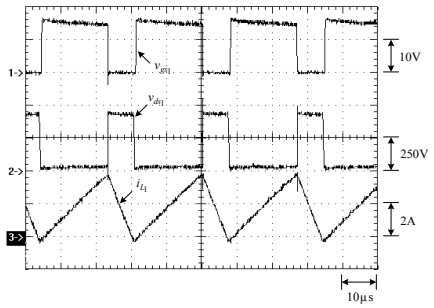


Fig. 19. Measured waveforms under input voltage of $85V_{AC}$ at rated load for the first stage: (1) $v_{gs1}$; (2) $v_{ds1}$; (3) $i_{L1}$.

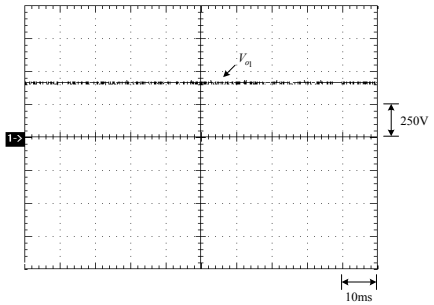


Fig. 20. Measured DC output voltage under input voltage of $85V_{AC}$ at rated load for the first stage.

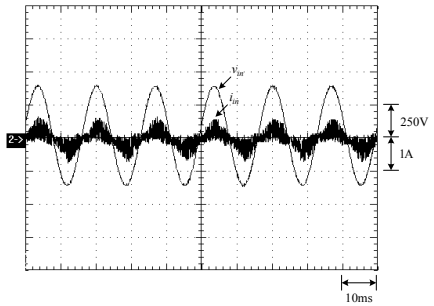


Fig. 21. Measured waveforms under input voltage of $265V_{AC}$ at half load for the first stage: (1) $v_{in}$; (2) $i_{in}$.

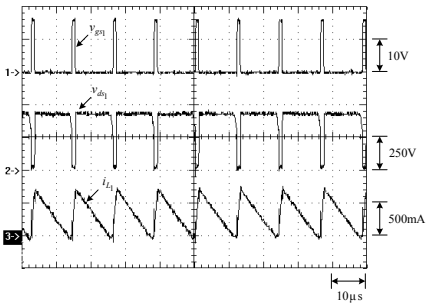


Fig. 22. Measured waveforms under input voltage of $265V_{AC}$ at half load for the first stage: (1) $v_{gs1}$; (2) $v_{ds1}$; (3) $i_{L1}$.

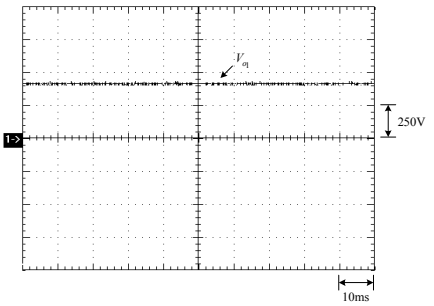


Fig. 23. Measured DC output voltage under input voltage of $265V_{AC}$ at half load for the first stage.

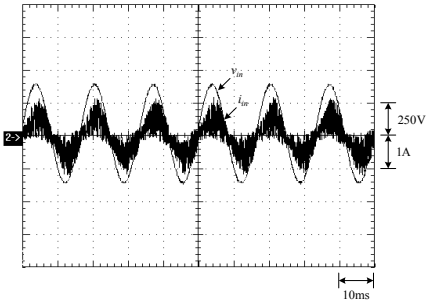


Fig. 24. Measured waveforms under input voltage of $265V_{AC}$ at rated load for the first stage: (1) $v_{in}$; (2) $i_{in}$.

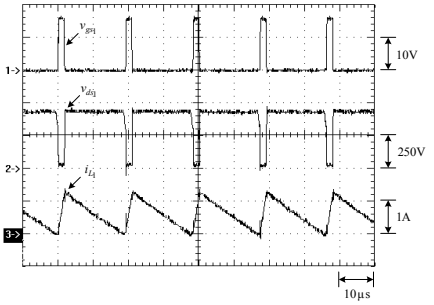


Fig. 25. Measured waveforms under input voltage of $265V_{AC}$ at rated load for the first stage: (1) $v_{gs1}$; (2) $v_{ds1}$; (3) $i_{L1}$.

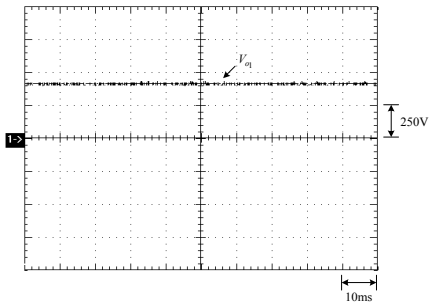


Fig. 26. Measured DC output voltage under input voltage of $265V_{AC}$ at rated load for the first stage.

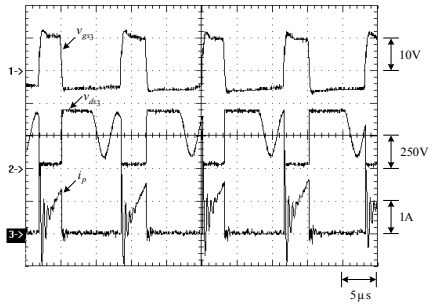


Fig. 27. Measured waveforms at half load for the second stage: (1) $v_{gs3}$; (2) $v_{ds3}$; (3) $i_p$.

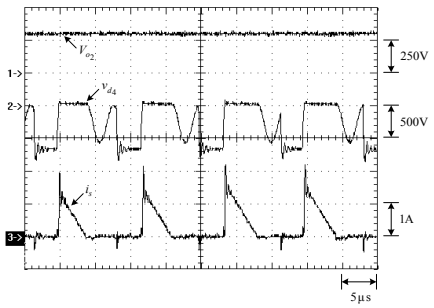


Fig. 28. Measured waveforms at half load for the second stage: (1) $V_{o2}$; (2)$v_{d4}$; (3) $i_s$.

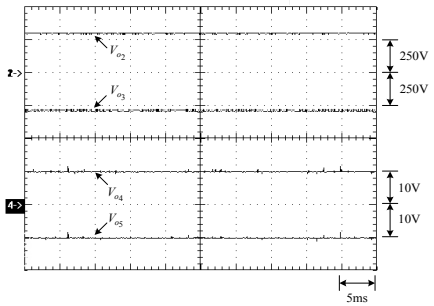


Fig. 29. Measured waveforms at half load for the second stage: (1) $V_{o2}$; (2) $V_{o3}$; (3) $V_{o4}$; (4) $V_{o5}$.

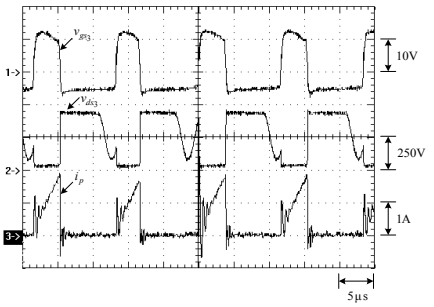


Fig. 30. Measured waveforms at rated load for the second stage: (1) $v_{gs3}$; (2) $v_{ds3}$; (3) $i_p$.

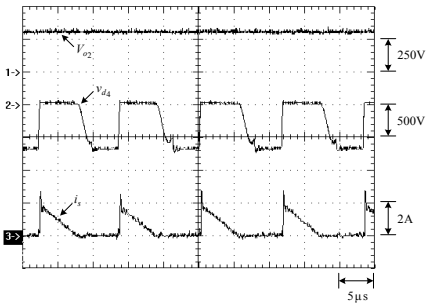


Fig. 31. Measured waveforms at rated load for the second stage: (1) $V_{o2}$; (2)$v_{d4}$; (3) $i_s$.

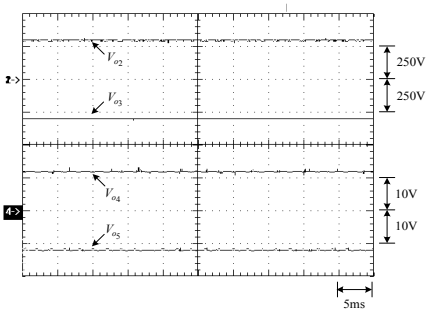


Fig. 32. Measured waveforms at rated load for the second stage: (1) $V_{o2}$; (2) $V_{o3}$; (3) $V_{o4}$; (4) $V_{o5}$.

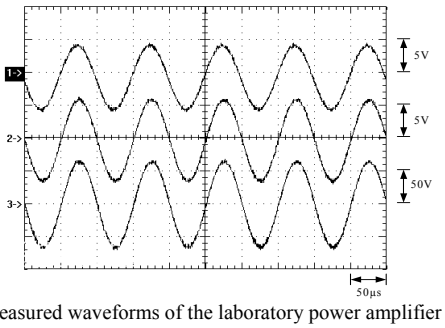


Fig. 33. Measured waveforms of the laboratory power amplifier with the proposed two-stage converter fed under the condition of the amplification gain 1×10 : (1) input voltage signal; (2) output of the first amplifier; (3) output of the second amplifier.

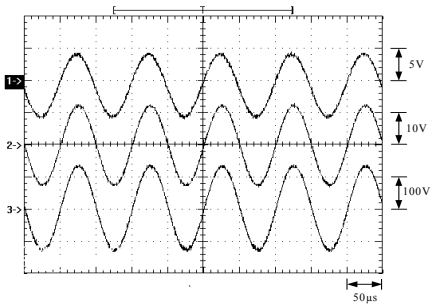


Fig. 34. Measured waveforms of the laboratory power amplifier with the proposed two-stage converter fed under the condition of the amplification gain $2\times10$ : (1) input voltage signal; (2) output of the first amplifier; (3) output of the second amplifier.

## VI. CONCLUSION

In this paper, two converters are cascaded to realize PFC and multiple outputs, and applied to feed the laboratory power amplifier. The first-stage converter is controlled in CRM, whereas the second-stage converter is controlled in DCM, and hence the controller for each converter is easy to design based on MATLAB/SISOTOOL. By doing so, this topology is suitable for high-voltage low-power applications. Aside from this, the two-transistor flyback converter is used as the second-stage converter, and hence the voltage stress across the corresponding main switches can be reduced, if high-voltage applications are required.

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