![Texas Instruments]

Using the I2S Audio Interface of DS90Ux92x FPD-Link III Devices

Mahendra Patel, Ryan Bailey

ABSTRACT

I2S is a standard protocol for transmitting two channels (stereo) Pulse Code Modulated digital data over a 3-wire serial bus.

Advanced automotive systems require transport of multiple audio data sources, such as mobile devices, Navigation systems, Infotainment, security, or gaming consoles, to speakers located throughout the vehicle. Also, surround sound systems requiring multiple audio data channels may be utilized to enhance the quality and richness sound reproduction. This document describes how to use the Inter-IC Sound (I2S) features of the DS90Ux92x family of FPD-Link III Serializers and Deserializers.

Contents

List of Figures

1 Introduction

The DS90Ux92x family of devices supports the I2S specification by simple setup of the serial control registers or hardware configuration. These Ser/Des devices allows transportation of I2S digital signals along with the video data over a single serial link. This makes it a cost effective solution for the automotive infotainment systems, as it enables transportation of Audio-Visual information simultaneously. Refer Figure 1.
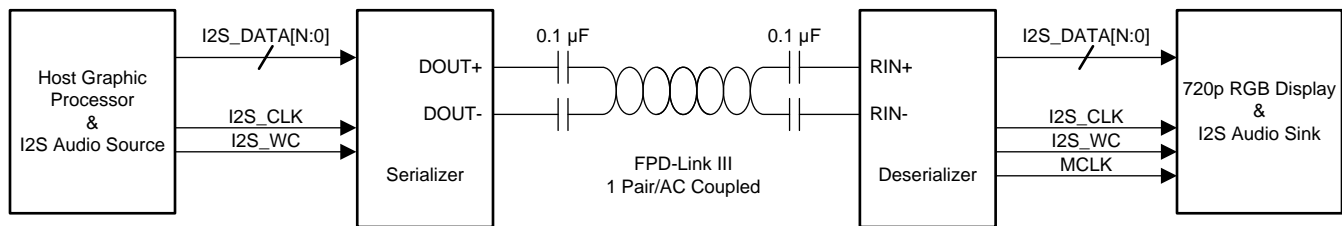

Figure 1. Generic I2S Operation on SER/DES link

This application note focuses on the I2S interface of following:

- Serializers: DS90UB925, DS90UB927, DS90UH925, DS90UH927
- Deserializers: DS90UB926, DS90UB928, DS90UH926, DS90UH928

Table 1 lists the I2S pins on each of the SER/DES devices referenced in this report. For the purposes of this document, register names are referred to using hexadecimal notation (0xYZ[i]), where YZ is the 8-bit register address offset and [i] refers to a specific bit or range of bits.

Table 1. I2S Bus pin details

Device	I2S Bus line (Name, pin #)						
	MCLK	CLK	WC	SD		SD	
DS90Ux925	N/A	I2S_CLK, 13	I2S_WC, 12	I2S_DA, 11		I2S_DB, 44	
DS90Ux926	MCLK, 60	I2S_CLK, 1	I2S_WC, 30	I2S_DA, 45		I2S_DB, 18	
DS90Ux927	N/A	I2S_CLK, 2	I2S_WC, 1	I2S_DA, 3	I2S_DB, 4	I2S_DC, 5	I2S_DD, 6
DS90Ux928	MCLK, 11	I2S_CLK, 8	I2S_WC, 10	I2S_DA, 7	I2S_DB, 3	I2S_DC, 37	I2S_DD, 36

2 I2S

The Inter-IC Sound (I2S) serial interconnect format is a popular standard for the exchange of stereo digital samples between two devices on a printed circuit board. It uses Pulse-code modulation (PCM) to digitally represent sampled analog signals. The magnitude of the analog signal is sampled regularly at uniform intervals, with each sample being quantized to the nearest value within a range of digital steps.

2.1 Interface

The I2S bus is a three-wire (or more) connection that exclusively handles two time-multiplexed data channels. Other information such as sub-coding and control are transferred separately. The three lines are the bit clock (CLK), the word clock (WC), and the serial data line (SD).

The device which generates appropriate bit clock (CLK) and word clock (WC) signals on the bus is called master, whereas other devices which accept CLK and WC as inputs are all slaves. The serialized audio signal transmitting device (which may or may not be the master device) places the data on the bus in synchronization with the CLK and WC signal from the master. Serializers are capable of receiving the clocking signals to act as I2S slave and the Deserializer device regenerates all of the necessary clocking signals to act as I2S master.

Table 2 below covers the range of I2S sample rates, most common word sizes and bit rate combinations.

Table 2. Audio Interface Frequencies

Sample Rate (kHz)	I2S Data Word Size (bits)	I2S_CLK (MHz)
192	16	6.144
32	24	1.536
44.1	24	2.117
48	24	2.304
96	24	4.608
192	24	9.216
32	32	2.048
44.1	32	2.822
48	32	3.072
96	32	6.144
192	32	12.288

NOTE:
- I2S_CLK frequency for DS90Ux92x devices must be maintained below PCLK/2 or 12.288MHz, whichever is lower.
- Devices listed in Table 1 supports the I2S electrical and timing specifications. For more details on timings of the signal refer to the device datasheet and I2S bus Specification by Philips Semiconductor.

2.2 Bit Rate Calculation

I2S data lines (PCM streams) have two basic properties that determine their fidelity to the original analog signal i.e., sampling rate (f_S) and number of bits per sample (M). Hence, I2S_CLK is decided by the bit rate (B_R) required to transport a digital audio signal, which can be calculated as follows:

$$B_R = MNf_s$$

M = Bit depth per sample (example: M=16 for 16-bits per channel)

N = number of channels (example: N=2 for standard I2S stereo format)

f_s = sampling rate (example: f_s=48kHz)   (1)

3 Operation

This section will discuss various modes of operation and controlling parameters of I2S bus for DS90Ux92x devices in detail.

3.1 Timing Supported

Standard I2S bus specification from Philips Semiconductor is meant to support two channels of audio (Stereo) over a single I2S data-line. However, the same electrical interface is capable of transmitting and receiving more than 2 channels of audio data using proper TDM scheme as explained in Section 3.1.2 and Section 4.5.

3.1.1 Stereo I2S

In this format, data is transmitted in order starting with MSB first for each word. Alternating left and right channel data words are transmitted over serial data line:
- Left Channel: WC = LOW
- Right Channel: WC = HIGH
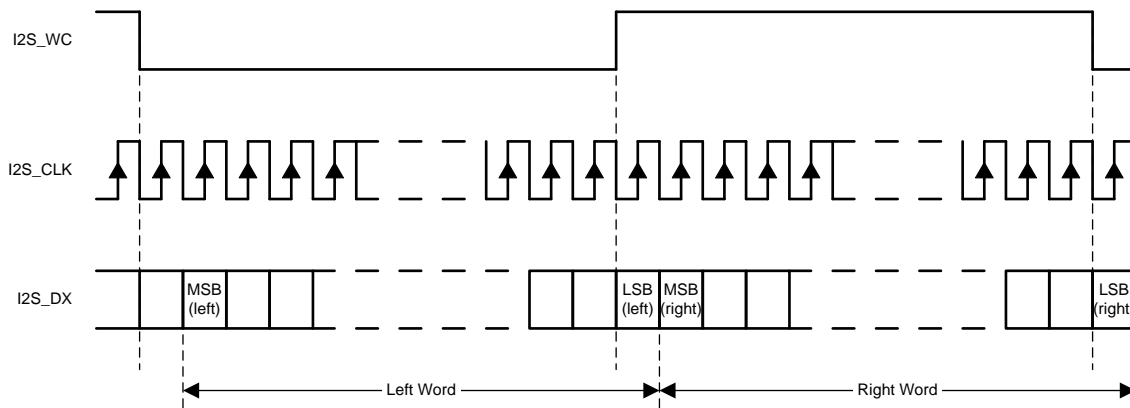
Figure 2 shows a timing diagram of the bus data.

Figure 2. I2S Frame timing diagram

The I2S specification is flexible enough that receivers and transmitters need not agree on a word size. Since data is transmitted MSB first and each new word is indicated by a transition in WC, the slave device can determine the appropriate word size based on the master's signals.

3.1.2 Time Division Multiplexing

The TDM interface is similar to the 2-Channel Serial Audio Interface, as discussed in Section 3.1.1, with the exception that more than 2 channels, typically 4 or 8, are transmitted within a frame (defined by a period of the I2S_WC), as shown in Figure 3 . As with the 2-Channel Serial Audio Interface, the TDM interface is comprised of the serial audio data line (I2S_DA), two control clocks, a frame synchronization pulse (FSYNC or I2S_WC, also called sampling frequency, f_S), and the serial clock (BCK or I2S_CLK).
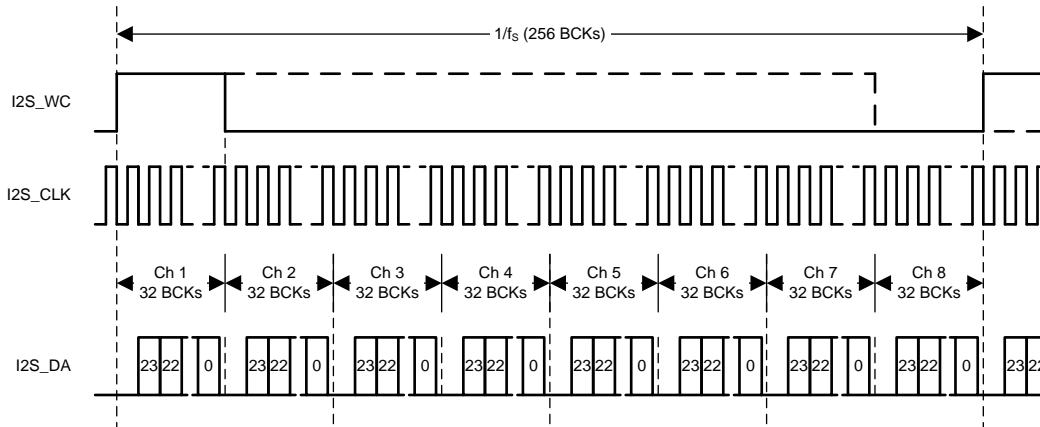

Figure 3. TDM Example: 8 Audio Channels Multiplexed

I2S_WC line identifies the beginning of a frame and the serial clock, I2S_CLK provides reference to shift the audio data into or out of the serial audio ports bit by bit. Width of the I2S_WC pulse can be used to define width of a slot assigned to each channel or a word duration within a frame as shown in Figure 3. Other sync schemes are possible and are specific to the audio master and slave devices used in the system.

3.2 Transport Methods

For DS90Ux92x family of devices, audio information can be transmitted in two different modes. The required transport mode can be selected by properly setting the Data Path Control 1 register. Refer to Table 5 for more details.

3.2.1 Packetized I2S Audio Transport

The FPD-Link III forward channel is organized into 28 [1] or 35-bit frames, the majority of which is occupied by video and control data. To support multi-channel audio, digital audio data is sent as a special frame during vertical video blanking periods, referred to as **Packetized Audio**.
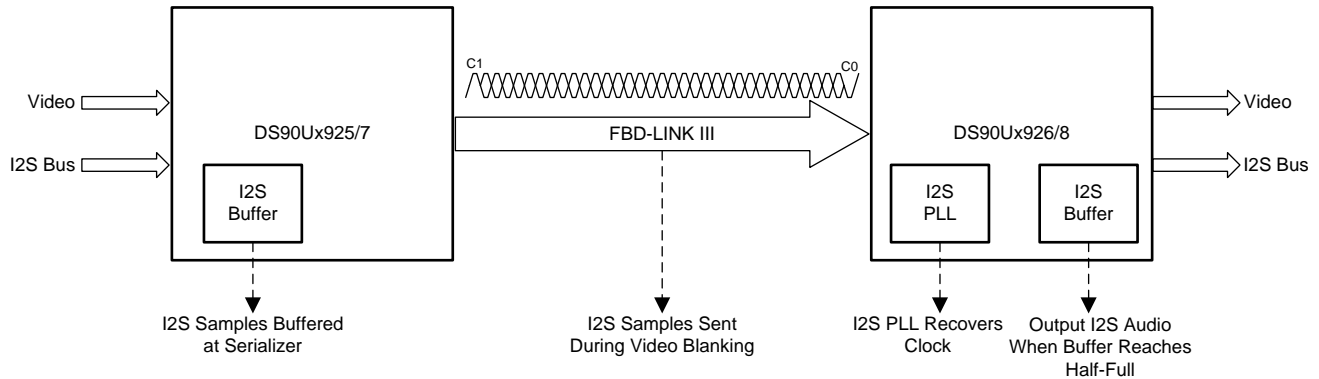

Figure 4. Packetized Audio Transmission

Input audio samples received at the serializer I2S pins are buffered internally. These buffered samples are transmitted to the deserializer during video blanking period over FPD-Link III in FIFO manner. The deserializer buffer receives audio samples and the deserializer I2S PLL recovers the I2S clock. The deserializer starts putting audio data on its I2S output pins once its buffer is half full.

3.2.2 Forward Frame I2S Audio Transport

In this mode, audio data is embedded with the video stream itself, allowing transmission of a few I2S data bits in each forward channel frame during active video.

> **NOTE:** Except for the surround sound mode in DS90Ux927/8, all of the remaining modes provides an option to select between two methods of audio transport mentioned in Section 3.2.1 and Section 3.2.2.

3.2.3 I2S Latency Across the Serial Link [2]

As I2S signals require additional processing at each device on the SER/DES link, there is a latency (delay) between input and output I2S signals. Typical latency period lies between 100µs and 200µs, which is much less than 2ms, required for most AV applications. Factors affecting latency include:

*   I2S PLL lock time on deserializer
*   Video blanking period and timing
*   I2S_CLK frequency (higher the frequency, lower is the latency)
*   Using multiple I2S data lines (more channels fill buffer faster, hence reduced latency)

3.3 Multi-Channel Operation

Each I2S data line can support one stereo channel data (i.e. two audio outputs, left and right). The DS90Ux92x family of devices supports multi-channel operation, utilizing multiple I2S data lines synchronized to the same I2S_WC and I2S_CLK lines. Specifically:

*   DS90UB925/6 devices have two I2S data lines (I2S_DA, DB) and can support 4 audio channels or 2 Stereo channels.
*   DS90UB927/8 devices has four data lines (I2S_DA, DB, DC, DD) and can support maximum of 8 audio outputs or 4 Stereo channels or 7.1 surround sound system.
*   In addition, TDM allows more than two channels of digital audio to be transported on a single I2S data

[1] The 28 bit frame format corresponds to backward compatible mode and I²S audio transport is not supported in this mode.
[2] This section talks about absolute latency of the I2S signal and not the latency with respect to video signals.

line.

3.4 Deserializer MCLK

In addition to I2S_CLK, I2S_WC, and I2S data lines, the Deserializer generates a Master I2S Clock (MCLK) using its internal I2S PLL. When the I2S PLL is disabled, the MCLK output is off.

The I2S PLL also cleans jitter of the reference clock, which reduces I2S_CLK output jitter to +/- 2ns. If I2S CLK frequency is less than 1MHz, this feature has to be disabled through the I2S Control register (0x2B), as given in Table 3.

By default MCLK is 2xI2S_CLK. However, it can be made 1×, 2×, 4× I2S_CLK through register settings described below:

Configuration of Deserializer MCLK frequency:

The following formula determines the MCLK frequency on deserializer:

$$MCLK = \frac{32 \times I2S\_CLK}{MDIV \times MSEL}$$

MDIV configures the MCLK multiplier, and is determined by 0x3A[6:4], as listed in Table 3

MSEL is chosen by internal logic to minimize the output jitter of MCLK, and is read from 0x7B[5:4]   (2)

To set the MCLK:

1. Set 0x3A[7]= 1, to override divider select for MCLK.
2. Read MSEL (0x7B[5:4])
3. Use MSEL and the above equation to set MDIV (0x3A[6:4]) for the required I2S MCLK frequency.

Table 3. Deserializer DS90Ux926/8: I2S PLL and MCLK control

ADDR (dec)	ADDR (hex)	Register name	Bit(s)	Register Type	Default (hex)	Function	Description
43	0x2B (DS90Ux926 only)	I2S Control	7	R/W	0x00	I2S PLL	I2S PLL Control 0: I2S PLL is on for I2S data jitter cleaning 1: I2S PLL is off. No jitter cleaning
			6:1			Reserved	-
			0			I2S Clock Edge	I2S clock edge select 0: I2S Data is strobed on the rising clock edge 1: I2S data is strobed on the falling clock edge
43	0x2B (DS90Ux928 only)	I2S Control	7	RW	0x00	I2S PLL Override	I2S PLL Control Override 0: PLL override disabled (default) 1: PLL override enabled
			6			I2S PLL Enable	I2S PLL Control Enable 0: I2S PLL is on for I2S data jitter cleaning (default) 1: I2S PLL is off. No jitter cleaning
			5:1			Reserved	-
			0			I2S Clock Edge	I2S Clock Edge Select 0: I2S Data is strobed on the Falling Clock Edge(default) 1: I2S Data is strobed on the Rising Clock Edge
58	0x3A	I2S MCLK Output	7	R/W	0x00	MCLK Override	0: No override for MCLK divider 1: Override divider select for MCLK
			6:4			MCLK Frequency Select	Divide ratio select for MCLK output, 000: MDIV=32, 001: MDIV=16, 010: MDIV=8, 011: MDIV=4, 100 or 101: MDIV=2, 110 or 111: MDIV=1.
			3:0			Reserved	-

Table 3. Deserializer DS90Ux926/8: I2S PLL and MCLK control (continued)

ADDR (dec)	ADDR (hex)	Register name	Bit(s)	Register Type	Default (hex)	Function	Description
123	0x7B	I2S Test Monitor	5:4	R	-	MSEL value	Internally selected divide ratio for MCLK output, 00: MSEL=1, 01: MSEL=2, 10: MSEL=4, 11: MSEL=8.

3.5   Backward Compatibility

I2S functionality is not supported when the DS90Ux92x devices are configured in Backwards Compatibility Mode (BKWD=1). Refer to the device datasheets for more information.

3.6   Repeater Configuration

Setting these devices into repeater mode provides a mechanism for transmission over multiple links to multiple display devices in the system. In the repeater application, serializers are referred to as the Transmitter (TX) and deserializers are referred to as the Receiver (RX).

At each repeater node, the parallel LVCMOS or LVDS interface provides video data, HS/VS/DE control signals and optionally, packetized audio data. All audio and video data can be fanned out to maximum of three transmitter per receiver.
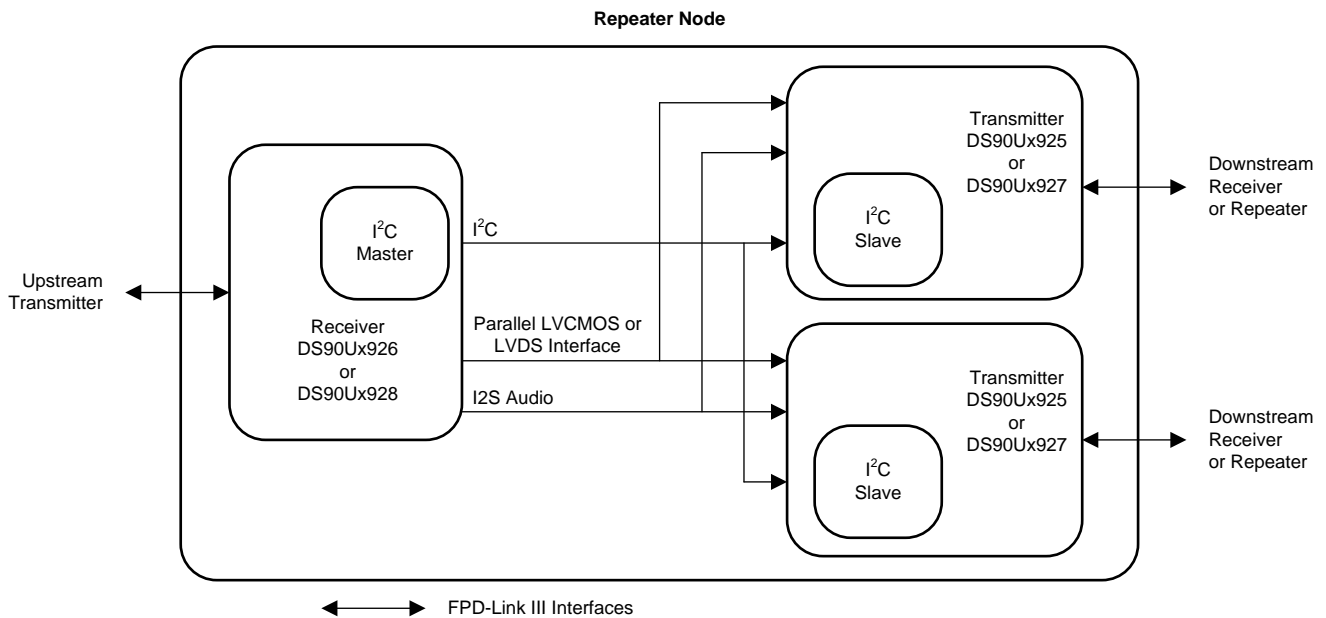
Figure 5. 1:2 Repeater Configuration

By default, audio is transmitted over the video interface during video blanking periods. This method is referred to as Data Island Audio transport, and avoids the need to regenerate the I2S interface at each repeater node.

Alternatively, audio can be set to transmit using the I2S pins on each device. To select between the two modes:

* On serializer, setting 0x12[4] = 1 allows regeneration of audio signals on I2S bus at each repeater node. This format is supported on deserializer, by auto loading of 0x22[4] (set to 1) from SER over forward channel.
* On serializer, setting 0x12[4] = 0 allows packetized audio to be transmitted on the parallel video interface pins. This format is supported on deserializer, by auto loading of 0x22[4] (set to 0) from SER over forward channel.

> **NOTE:**
> 1. For this mode of operation, all Transmitter and Receiver located at each repeater nodes must be set into the Repeater Mode. Refer device datasheet for more details on how to set the device in repeater mode.
> 2. To disable the auto loading of 0x22[4] bit in deserializer, set 0x22[7]=1. This will allow to set the mode on deserializer locally.

3.7 Control Registers

This section gives descriptions of control registers associated with the I2S interface of the DS90Ux92x devices.

3.7.1 Data Path Control 1

This register is present on all DS90Ux92x devices and Table 4 gives the address details. This content is automatically loaded into the deserializer from SER over forward channel, unless overridden in the deserializer control registers. To disable auto-loading and instead configure locally, set the deserializer register 0x22[7]=1.

Table 4. Data Path Control 1: Address details

	Device	Address (Dec)	Address (Hex)
1	DS90Ux925, DS90Ux927	18	0x12
2	DS90Ux926, DS90Ux928	34	0x22

Table 5. Data Path Control 1 Register

Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
Data Path Control	4	RW	0x00	I2S Repeater Regen	I2S Repeater Regeneration 1: Repeater regenerate I2S from I2S pins 0: Repeater pass through I2S from video pins (packetized audio)
	3			I2S Channel B Enable Override	I2S Channel B Enable 1: Set I2S Channel B Enable from reg_12[0] 0: Set I2S Channel B Enable from MODE_SEL pin
	2			18-bit Video Select	18–bit video select 1: Select 18-bit video mode Note: use of GPIO(s) on unused inputs must be enabled by register. 0: Select 24-bit video mode
	1			I2S Transport Select	I2S Transport Mode Select 1: Enable I2S Data Forward Channel Frame Transport 0: Enable I2S Data Island Transport
	0			I2S Channel B Enable	I2S Channel B Enable 1: Enable I2S Channel B 0: I2S Channel B disabled

3.7.2 Data Path Control 2

This register is present on both DS90Ux927 and DS90Ux928 devices. The serializer settings are automatically loaded into the deserializer, unless overridden in the deserializer control registers. To disable auto-loading and instead configure locally, set the deserializer register 0x28[7]=1.

Table 6. Data Path Control 2 Register: DS90Ux927

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
26	0x1A	Data Path Control 2	7	RW	0x00	Block I2S Auto Config	Block automatic I2S mode configuration (repeater only) 0: I2S mode (2-channel, 4-channel, or surround) is detected from the in-band audio signaling 1: Disable automatic detection of I2S mode
			6:1				*Reserved*
			0	RW		I2S Surround	Enable 5.1- or 7.1-channel I2S audio transport 0: 2-channel or 4-channel I2S audio is enabled as configured in register 0x12 bits 3 and 0 (default) 1: 5.1- or 7.1-channel audio is enabled Note that I2S Data Island Transport is the only option for surround audio. Also note that in a repeater, this bit may be overridden by the in-band I2S mode detection.

Table 7. Data Path Control 2 Register: DS90Ux928

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Description
40	0x28	Data Path Control 2	7	RW	0x00	Block I2S Auto Config	Override Forward Channel Configuration 0: Enable forward-channel loading of this register(default) 1: Disable loading of this register from the forward channel, keeping local values intact
			6:4				*Reserved*
			3	RW		Aux I2S Enable	Auxiliary I2S Channel Enable 0: Normal GPIO[1:0] operation (default) 1: Enable Aux I2S channel on GPIO1 (Aux Word Select) and GPIO0 (Aux Data)
			2	RW		I2S Disable	Disable All I2S Outputs 0: I2S Outputs enabled (default) 1: I2S Outputs disabled
			1				Reserved
			0	RW		I2S Surround	Enable 5.1- or 7.1-channel I2S audio transport 0: 2-channel or 4-channel I2S audio is enabled as configured in register 0x12 bits 3 and 0 (default) 1: 5.1- or 7.1-channel audio is enabled Note that I2S Data Island Transport is the only option for surround audio. Also note that in a repeater, this bit may be overridden by the in-band I2S mode detection.

4   Application Examples

This section describes I2S operation of various Serializer-Deserializer combination and available modes with DS90Ux92x family. Table 8 summarizes the examples considered in this section.

Table 8. Modes of Operation: I2S Interface of DS90Ux92x family

Serializer	Deserializer	Mode	Number of Audio Channels Supported			
			2	4	8	TDM
DS90Ux925	DS90Ux926 / DS90Ux928	24-bit RGB (Default)	√	-	-	√
		18-bit RGB & I2S Channel B enabled	√	√	-	√
DS90Ux927	DS90Ux926	24-bit (Default)	√	-	-	√
		18-bit RGB & I2S Channel B enabled	√	√	-	√

Table 8. Modes of Operation: I2S Interface of DS90Ux92x family (continued)

Serializer	Deserializer	Mode	Number of Audio Channels Supported			
			2	4	8	TDM
DS90UH927	DS90Ux928	Default	√	-	-	√
		I2S Channel B enabled	√	√	-	√
		Surround Sound Enabled	√	√	√	√
DS90UB927	DS90Ux928	Default	-	-	-	-
		On DS90UB927 Serializer, • Setting 0x12[1] = 1; Forward channel frame transport enabled and 0x04[4] = 0; Pass RGB independent of DE (default) OR • 0x04[4] = 1; Gate RGB with respect to DE and 0x12[1] = 0; Data Island transport (default)	√	-	-	√
		I2S Channel B enabled and on DS90UB927 Serializer, • Setting 0x12[1] = 1 and register 0x20=0x81; To enable forward channel frame transport of both I2S data-lines. and 0x04[4] = 0; Pass RGB independent of DE (default) OR • 0x04[4] = 1; Gate RGB with respect to DE and 0x12[1] = 0; Data Island transport (default)	√	√	-	√
		Surround Sound Enabled • 0x04[4] = 1; Gate RGB with respect to DE and 0x12[1] = 0; Data Island transport (default)	√	√	√	√

4.1   2-Audio Channel or Stereo Operation

As can be noted from Table 8, each of the device in DS90Ux92x family by default operates in 24-bit RGB mode and supports two channels of audio over I2S interface for the operation shown in Figure 6. Hence, no additional configuration is required, with the **exception of the DS90UB927- DS90Ux928 pair**, which requires additional register settings as given below:

1. Forward channel frame transport (Register settings on DS90UB927)
    *   Bit 0x04[4] = 0; Pass RGB independent of DE (default)
    *   Set bit 0x12[1] = 1; Forward channel frame transport.
2. Data Island transport (Register settings on DS90UB927)
    *   Bit 0x12[1] = 0 by default, which implies Data Island transport
    *   Set bit 0x04[4] = 1; Gate RGB with respect to DE.

The Serializer supports three I2S lines and they are I2S_CLK, I2S_WC and I2S_DA. The Deserializer at the other end of the serial link reproduces signal on I2S bus with additional MCLK as discussed in Section 3.4
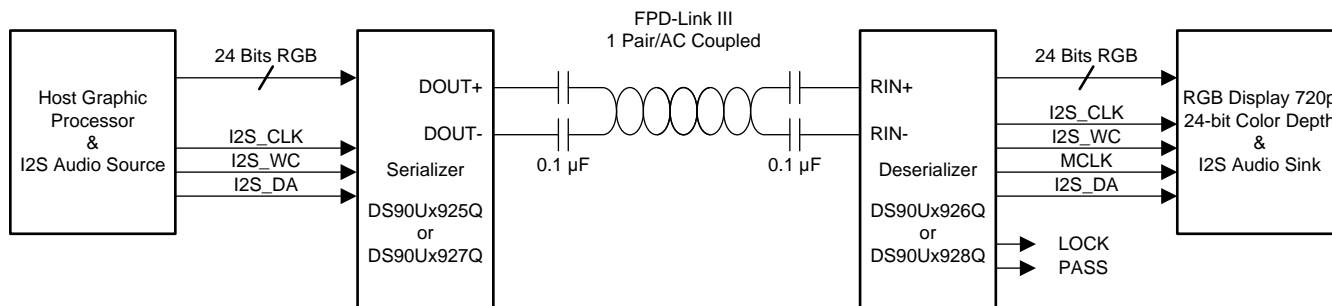
Figure 6. 2-Audio Channel or Stereo Operation

4.2   4-Audio Channel Operation with DS90Ux925/926

In 18-bit RGB mode, the secondary I2S data line (I2S_DB) can be used. The input must be synchronized to I2S_CLK and aligned with I2S_WC at the input to the serializer. Deserializer supports all these lines and default MCLK output frequency of I2S_CLK×2. MCLK frequency can be changed through 0x3A[6:4] bits of DS90Ux926. Refer to Section 3.4.

There are two alternatives to set the SER/DES link in 18-bit RGB mode,

1. Using an appropriate resistor divider on MODE_SEL pin of both the devices. Refer to the MODE_SEL configuration guidelines in the device datasheets.

2. To enable 18 bit video mode through register, configure Data Path Control 1 register as below. Refer Table 5 for more details on these registers.
   On DS90Ux925,

   (a) Set bit 0x12[3] = 1, to enable the secondary I2S data channel.

   (b) Set bit 0x12[2] = 1, to select 18-bit video mode.

   (c) Set bit 0x12[0] = 1, to enable I2S channel B.

On the DS90Ux926 (or DS90Ux928), register 0x22 is auto loaded from the serializer through forward channel data.
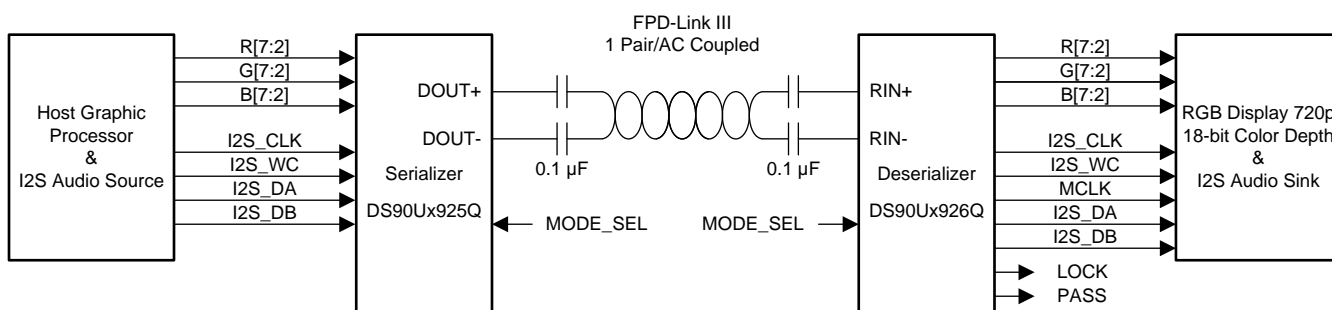
Figure 7. 4-Audio Channel Operation for DS90Ux925/926

4.3   4-Audio Channel Operation with DS90Ux927/928

Irrespective of 18-bit RGB or 24 bit RGB mode, the secondary I2S data line (I2S_DB) can be used for this pair of devices. The I2S_DB input must be synchronized to I2S_CLK and aligned with I2S_WC at the input to the serializer. The deserializer supports all these lines and default MCLK output frequencies of I2S_CLK×2. Different MCLK frequencies can also be enabled through the register bit 0x3A[6:4] of deserializer.

Configure Data Path Control register 1 as below to enable the use of second I2S data line (I2S_DB). Refer Table 5 for more details on this register.
On DS90Ux927,

1. Set bit 0x12[3] = 1, to enable secondary I2S data channel from bit 0x12[0].

2. Set bit 0x12[0] = 1, to enable I2S channel B.

DS90UB927 also requires additional settings for this mode of operation as given below,

1. Forward channel frame transport (Register settings on DS90UB927)
    - Bit 0x04[4] = 0; Pass RGB independent of DE (default)
    - Set bit 0x12[1] = 1 and 0x20[7:0]=0x81; To enable forward channel frame transport of both I2S data-lines.
2. Data Island transport (Register settings on DS90UB927)
    - Bit 0x12[1] = 0 by default, which implies Data Island transport
    - Set bit 0x04[4] = 1; Gate RGB with respect to DE.

On DS90Ux928,register 0x22 is auto loaded through the forward channel data.
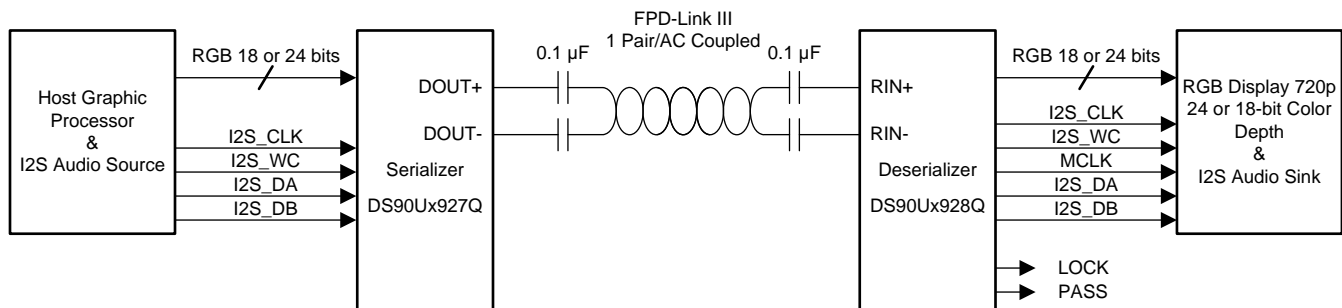
Figure 8. 4-Audio Channel Operation with DS90Ux927/928

4.4 8-Audio Channel or Surround Sound Operation

When DS90Ux927 is paired with a DS90Ux928Q deserializer, surround sound audio applications are supported.

Surround sound is a technique for enriching the sound reproduction quality of an audio source with additional audio channels from speakers. It surrounds the listener, providing sound from a 360° radius in the horizontal plane (2D). The technique enhances the perception of sound due to listener's ability to identify the origin of a detected sound in direction and distance. For example 8 channels of audio, consisting of 7 full-range channels and a single LFE (low frequency effect) channel, gives 7.1 Surround Sound.

Surround sound can be **enabled by setting 0x1A[0]=1 in DS90Ux927**. In this mode, up to four I2S data lines can be used and packetized audio information is transmitted during the video blanking periods (Forward frame transport option is not available in this mode).
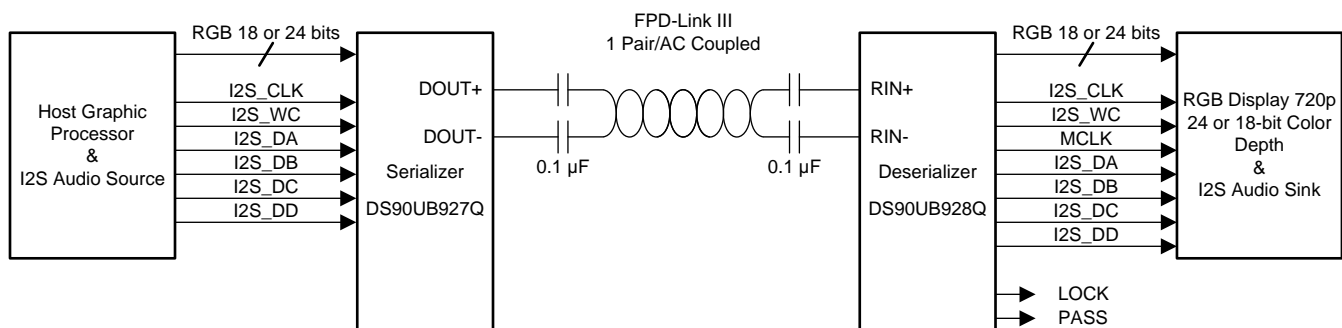
Figure 9. 8-Audio Channel or Surround Sound Operation

To summarize, on DS90Ux927
- I2S_DB can be enabled, by setting 0x12[3] = 1 and 0x12[0] = 1

- I2S_DC and I2S_DD are only activated, while operating the device in surround sound mode, i.e. 0x1A[0] = 1.

NOTE: GPIO_REG[8:5], which are shared lines with I2S bus lines are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. GPIOs will override I2S input if enabled into REG_GPIO mode.

4.5 TDM Operation

Time Division Multiplexed (TDM) interface allows multiple channels of data to be transmitted between devices on a single data line within a system. Figure 10 is a block diagram level representation of TDM implementation with SERDES devices.
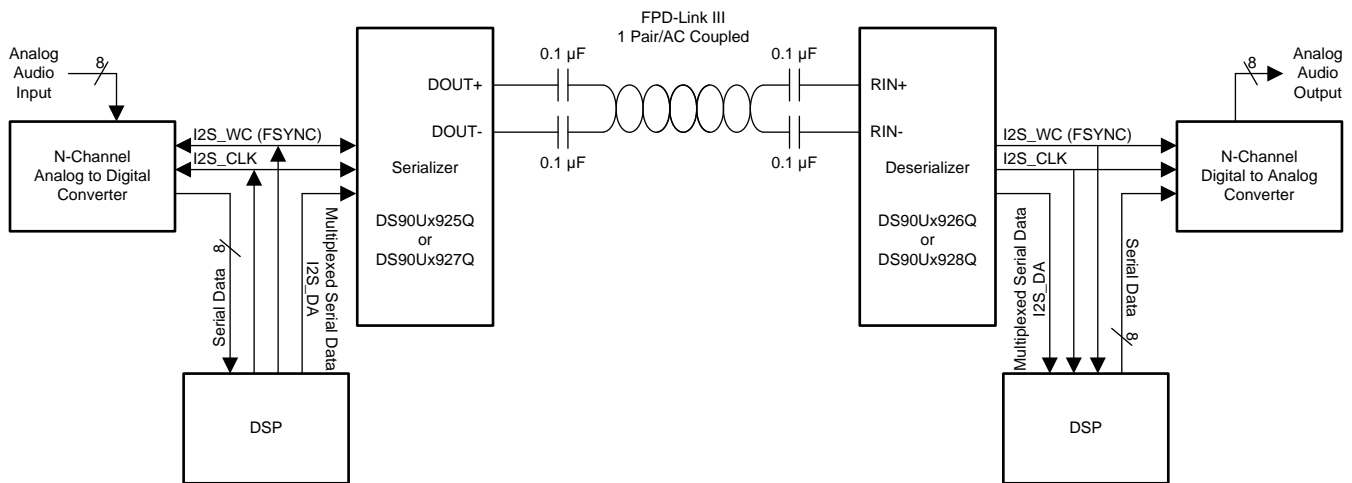
Figure 10. TDM implementation with SER/DES

TDM format can be implemented in large number of ways depending upon the word length, bit clock, and number of channels.

For example, assuming I2S_WC period of 256 bits, a single TDM channel can time multiplex up to 8 channels with a maximum sample word length of 32 bits. Figure 3 illustrates the timing for multiplexing of 8 channels with 24 bit word length.

The number of channels multiplexed on each TDM data line must be selected as a power of 2, (i.e. 2, 4, or 8). If the total number of audio channels is greater than 8, multiple data inputs can be used.

5 Conclusion

The I2S digital audio interface offered by the DS90Ux92x family of FPD-Link III devices enables transport of multi-channel digital audio throughout automotive infotainment systems. This flexible interface supports both stereo-encoded I2S channels, as well as multi-channel TDM audio formats. Using the controls and techniques described in this document, these devices enable system designers to easily implement advanced and robust audio features in the automotive environment.

6 References

1. Philips I2S bus specification
2. DS90UB925Q 5-85MHz 24-bit Color FPD-Link III Serializer with BCC ()
3. DS90UH925Q 720p 24-bit Color FPD-Link III Serializer with HDCP ()
4. DS90UB926Q 8-85MHz 24-bit Color FPD-Link III Deserializer with Bidirectional Control Channel ()
5. DS90UH926Q 720p 24-bit Color FPD-Link III Deserializer with HDCP ()
6. DS90UB927Q 5-85MHz 24-bit Color FPD-Link III Serializer with BCC ()

7. DS90UH927Q 5MHz-85MHz 24-bit Color FPD-Link III Serializer with HDCP ()
8. DS90UB928Q FPD-Link III Deserializer with BCC ()
9. DS90UH928Q 5MHz-85MHz 24-bit Color FPD-Link III to FPD-Link Deserializer ()

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		