Analysis of Line Current Harmonics for Single-Phase PFC Converters

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***Abstract*-Line current distortion for active PFC converters is usually governed by the IEC61000-3-2 harmonic standard. Feedback and feed-forward loop design for these circuits generally involves the inherent tradeoff between input current distortion and dynamic response. Typically, simulations are performed to help determine the optimal compromise between these two parameters. However creating a valid simulation model can be quite complicated and time consuming. This is generally the case with PFC converters due to the presence of multiple, low and high frequency feedback loops. Complicating matters even further, the model must properly account for crossover-distortion, which at the higher line frequencies can easily dominate the harmonic spectrum. Proposed here is an alternative approach in which we write all of the governing equations and allow the powerful symbolic processor contained within a MathCAD routine to carry out the actual computation. This method is not only faster but also provides a means for error checking not possible with a simulation. This paper outlines an elegant method using the classical Fourier series and integrals for the analysis of these harmonics. Here we predict the input line current distortion with excellent convergence between theoretical and actual results. This paper is based on a conventional boost topology utilizing the L4981 PFC chip. The equations and techniques laid out in this paper also provide a convenient basis for the evaluation of more sophisticated loops.**

I. INTRODUCTION

The introduction of the input line current harmonic standard, IEC555-2, to the electrical equipment market has had a significant impact on the design of switching power supplies [1]. This standard specifically limited harmonic currents for "non-professional" equipment with input currents less than 16A per phase. Over a period of time, IEC 555-2 had evolved into the well known European standard, IEC61000-3-2 [2]-[3]. This more stringent requirement divides electrical equipment into four classes; A through D. These classes define the maximum harmonic limit levels up to and including the 40th harmonic of line frequency. These standards, as is commonly known, had precipitated the development of the PFC converter.

Unfortunately, in order to maintain low THD, PFC converters are inherently slow. Thus since the introduction of these types of converters, there has been intense interest in speeding up the feedback and feed-forward loops with an eye on THD [4]. In many cases, designs operate very close to the IEC limits to provide the fastest possible response. Because of this inherent limitation, we have seen new techniques, including those involving digital control [5], in the attempt to further improve performance. In fact, a good amount of recent research has focused on altering these loops in some unique way to achieve this [6]-[9]. In this paper a method will be presented for evaluating these harmonics using a conventional scheme. We leave the task of evaluating more sophisticated loops as an additional exercise in transfer function algebra.

We begin with an active boost PFC converter operating in average current mode as shown in Fig. 1. To implement this technique we are using the L4981 IC. The Imo waveform, which is the output of the multiplier block, is our reference signal. Its waveshape is derived directly off of the rectified line through Iac with an amplitude that scales accordingly for line and load changes. This becomes the programming waveform for a fast, high gain current loop. The circuit's objective is to force this signal to follow the actual rectified input line voltage where we assume this as being a pure sine wave. In theory, an ideal waveform for Imo should translate into a fairly pure sinusoidal current on the input line. The scaling factor for this signal is important since it must adaptively correct for line and load levels. This parameter is derived from both the feed-forward and feedback loops. The feed-forward gets its information from the input line through a low pass filter and is fed into a square divider in order to compensate for changes in line voltage. The feedback loop is derived from an error amplifier and works off of the output bus to correct mainly for load changes. The result is a reference sinewave whose amplitude adjusts to the variation of both line and load. Done properly, this technique will make the regulator appear mostly resistive to the input source, thereby achieving near unity power factor and very low THD. Compared to a traditional bulk rectifier, it will have a much lower distortion level yielding a lower input current RMS for a given output power level. This of course is at the expense of a small amount of efficiency loss and higher circuit complexity.

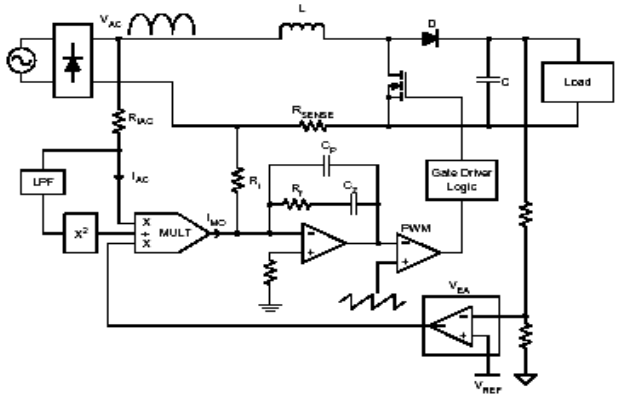

Figure 1. Active PFC Topology

II. ANALYSIS OF THE FEED-FORWARD FILTER

We start by analyzing the feed-forward loop. The purpose of this loop, although intentionally slow, is to adjust the PFC multiplier level relative to changes of the input line without having to wait for the even slower feedback loop to respond. This circuit's main responsibility is to obtain the rectified line's dc component. A typical feed-forward circuit utilizes a two pole network and is shown in Fig. 2. In this section our objective is to calculate the time domain waveform, VFF(t), as well as its Fourier series components for use later on.

The input of this network, defined as Vrect(t) in Fig. 2, is the rectified input line which we express as the absolute value of the instantaneous line voltage within the integral of (1). Vin is defined as the RMS input line voltage. Here we write the input equation for this network and use the exponential form of the Fourier integral [10] to calculate the input source coefficient matrix (1). We then evaluate it for harmonics (k=1 to 40^{th} of the line frequency).

$$\text{input}_k := \frac{1}{\text{Tline}} \cdot \int_{0\cdot\text{sec}}^{\text{Tline}} \left| \text{Vin}\sqrt{2}\cdot\sin\left(2\cdot\pi\cdot\frac{t}{\text{Tline}}\right)\right| \cdot e^{-j\cdot k\cdot 2\frac{\pi}{\text{Tline}}\cdot t}\, dt \qquad (1)$$

Next we algebraically derive the transfer function of the network (2) and evaluate it at harmonics k=1 through 40 as well using (3). Note that there is no need to simplify (2) any further within the MathCAD software.

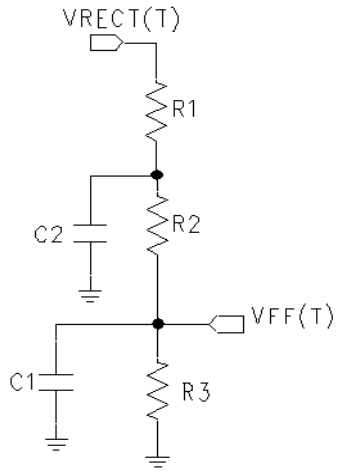

Figure 2. Feed-forward Filter

$$\text{Tran}_k := \frac{\left(\frac{\frac{R3}{s_k\cdot C1}}{\frac{1}{s_k\cdot C1}+R3}+R2\right)\frac{1}{s_k\cdot C2}}{\left(\frac{\frac{R3}{s_k\cdot C1}}{\frac{1}{s_k\cdot C1}+R3}+R2\right)+\frac{1}{s_k\cdot C2}} \cdot \frac{\frac{\frac{R3}{s_k\cdot C1}}{\frac{1}{s_k\cdot C1}+R3}+R2}{\left(\frac{\frac{R3}{s_k\cdot C1}}{\frac{1}{s_k\cdot C1}+R3}+R2\right)\frac{1}{s_k\cdot C2}+R1} \qquad (2)$$

$$s_k := j\cdot 2\frac{\pi}{\text{Tline}}\cdot k \qquad (3)$$

To get our output response (4), we simply take the product of the complex source matrix (1) and our feed-forward matrix (2). As a check, the result is plugged into the Fourier time domain expansion (6) to reconstruct the Vff(t) waveform and confirm periodicity. The frequency domain coefficients are now stored in Vff_k for use later on. Note that the DC component of Vff(t) , or Vff_0, is calculated separately using (5). This is done to avoid a divide by zero in (2).

$$\text{Vff}_k := \text{input}_k\cdot\text{Tran}_k \qquad (4)$$

$$\text{Vff}_0 := \frac{\text{Vin}\cdot 2\sqrt{2}}{\pi}\cdot\frac{R3}{R1+R2+R3} \qquad (5)$$

$$\text{VFF}(t) := \text{Vff}_0 + \sum_k\left(2\cdot\text{Re}\left(\text{Vff}_k\right)\cdot\cos\left(2\cdot k\cdot\frac{\pi}{\text{Tline}}\cdot t\right)\right) - \sum_k\left(2\cdot\text{Im}\left(\text{Vff}_k\right)\cdot\sin\left(2\cdot k\cdot\frac{\pi}{\text{Tline}}\cdot t\right)\right) \qquad (6)$$

III. ANALYSIS OF THE FEEDBACK LOOP

We now determine the PFC bus line frequency ripple in the time domain and again use Fourier math to determine the feedback error amplifier output response. A typical feedback amplifier is shown in Fig. 3. In the example used in this paper, Tline is the line period for 60Hz operation. The low frequency ripple current, IC_120(t), through the output capacitor, Co, can be expressed in (9) from (7) and (8) below, where e= efficiency. It's important that these expressions maintain the phase relationship between the inductor current (8) and capacitor voltage (10) since this current generates the bus ripple voltage sensed by the error amplifier.

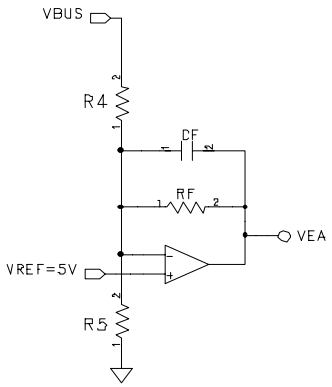

Figure 3. Feedback Error Amplifier

$$IL\_60Hz\_pk := \frac{Pin\_pfc \cdot \sqrt{2}}{Vin} \tag{7}$$

$$IL(t) := \left| IL\_60Hz\_pk \cdot \sin\left(2 \cdot \pi \cdot \frac{t}{Tline}\right) \right| \tag{8}$$

$$IC\_120(t) := \frac{IL(t) \cdot Vin \cdot \left| \sin\left(2 \cdot \pi \cdot \frac{t}{Tline}\right) \right| \cdot \sqrt{2} \cdot \varepsilon}{Vo} \tag{9}$$

We now take (9) and calculate the 120Hz output capacitor ripple voltage (10). Here we subtract out the DC component before integrating.

$$Vc(t) := \frac{1}{Cbus} \cdot \int_0^t \left(IC\_120(t) - \frac{Pin\_pfc \cdot \varepsilon}{Vo} \right) dt \tag{10}$$

The signal expressed in (10) feeds into our output error amplifier via divider resistor chain, R4 and R5. To determine the source matrix we write (11) below.

$$bus_k := \frac{1}{Tline} \cdot \int_{0 \cdot sec}^{Tline} Vc(t) \cdot e^{-j \cdot k \cdot 2 \frac{\pi}{Tline} \cdot t} dt \tag{11}$$

Now we algebraically determine the transfer function of our error amplifier (12) for k=1 to 40.

$$Toac_k := \frac{-Rf}{\left(1 + Rf \cdot s_k \cdot Cf\right) \cdot R4} \tag{12}$$

Multiplying (11) and (12), we get the error amplifier output response (13).

$$Vea_k := bus_k \cdot Toac_k \tag{13}$$

To determine the DC component of the error amplifier output, we start with (14) -the multiplier block expression for the PFC IC [11]. Imult (16) is defined as the multiplier output current which at a minimum must be able to provide enough peak current into its output resistor, which we will define as Rprog, in order to support the highest expected input line current under worst-case conditions. Thus the voltage developed across Rprog becomes the reference signal for our fast inner current loop which forces the same voltage to appear across Rshunt, the PFC current sense resistor. Vff used in (14) is expressed in (5) and is the average feed-forward voltage present at the input of the multiplier block. Iac (15) is the peak rectified line current flowing into the chip's "Iac pin".

$$Imult := \frac{\left(Vea - 1.28 \cdot volt\right)}{Vff^2} \cdot Iac \cdot volt \tag{14}$$

$$Iac := \frac{Vin \cdot \sqrt{2}}{Rac} \tag{15}$$

$$Iin := Imult \cdot \frac{Rprog}{Rshunt} \tag{16}$$

Solving for Vea using (5), (14), (15) and (16), we write (17) below. Note that due to the nature of the feed-forward, the input voltage has cancelled out and does not appear in (17).

$$Vea_0 := \frac{8 \cdot Pin \cdot Rac \cdot Rshunt \cdot R3^2}{Rprog \cdot (R1 + R2 + R3)^2 \cdot \pi^2 \cdot volt} + 1.28 \cdot volt \tag{17}$$

Actual component values are used in (17) to generate (18). The values used here are detailed in the next section. As expected, Vea_0 varies linearly with output power and the denominator in (18) approaches the maximum steady-state power capability of this design.

$$Vea_0 := 2.2 \cdot volt \frac{Pout}{\varepsilon \cdot 1500 \cdot watt} + 1.28 \cdot volt \tag{18}$$

Now we can write an equation for VEA(t). Vea0 is important since it will determine the expected input current for a given power level. This quantity will be error checked later.

$$VEA(t) := Vea_0 + \sum_k \left(2 \cdot Re\left(Vea_k\right) \cdot \cos\left(2 \cdot k \cdot \frac{\pi}{Tline} \cdot t\right) \right) - \sum_k \left(2 \cdot Im\left(Vea_k\right) \cdot \sin\left(2 \cdot k \cdot \frac{\pi}{Tline} \cdot t\right) \right) \tag{19}$$

IV. L4981 MULTIPLIER BLOCK

Since we have now have VFF(t) and VEA(t), we can finally proceed with writing an equation for the input current (20)

$$Ipredict(t) := \left(\frac{VEA(t) - 1.28 \cdot volt}{VFF(t)^2} \right) \frac{Iac(t) \cdot Rprog}{Rshunt} \cdot volt \tag{20}$$

where Iac(t) is defined in (21) below.

$$Iac(t) := \left| \frac{Vin\sqrt{2}\cdot\sin\left(2\cdot\pi\cdot\frac{t}{Ts}\right)}{Rac} \right| \qquad (21)$$

We are now ready to plot a waveform using MathCAD v.13 with the following converter engine and multiplier components (note that Co=560uF X 3 X 80% = 1344uF).

Pin=1205W, Vin=230 Vrms, Vo=400V, Co=1344uF,
Rac=903K OHM, Rprog=7.5K OHM,
Rshunt=0.025 OHM, e=94%,
Feed-Forward Component Values:
R1=282K, R2=15K, R3=7.5K, C1=1uF; and C2=1uF;
Feedback Component Values:
R5=10K; R4=790K, Rf=221K, Cf=2200pF;

Fig. 4 is a plot of our input current as compared to the ideal case for the given line and power level. For the sake of illustration our selection of component values used for this case causes significant distortion to the input line current. Note the higher peak value relative to the ideal whose peak is expressed in (7).

V. ZERO-CROSSING DISTORTION MODELING

Another form of distortion associated with these types of regulators is zero-crossing distortion, or sometimes noted as "cusp" distortion [12]. One common explanation for this is that the boost inductance is usually too large to allow a sufficient ramp in input current, for the given voltage, equal to that of the reference current near the zero-crossings. However recent research [13] has suggested that this distortion is mainly attributed to the rectifier bridge in combination with two factors: (A) The phase-lead nature of the input current relative to voltage at the bridge rectifier. (B) The lack of sufficient damping of the fast inner current loop which causes a ringing response of the input current right after turn on of the bridge diodes. This effect is most dramatically seen at the higher line frequencies (such as 600 Hz line) since the phase lead response at the bridge widens as input frequency increases. This exacerbates the issue since the bridge diodes must turn on into a higher level of current, causing larger overshoots and a longer ring time. In fact it is interesting to note that there has been a proposed scheme which solves this issue by eliminating the bridge rectifier entirely [14].

A. 50/60Hz Zero-Crossing Modeling

In this paper we will treat our zero-crossing distortion simply as a "dead-time". This is achieved simply by multiplying the time domain waveform (20) with the step function (22) to get our new input current waveform valid over a single cycle. This new input current waveform, df(t)*Ipredict, is shown in Fig. 5 along with the ideal line current for the given power level. Note the small step near zero. Periodicity of the resultant waveform is obtained in the next section once we calculate the Fourier integral.

$$df(t) := \left(\Phi(t - T\cdot d) - \Phi\left(t - \frac{T}{2}\right)\right) + \left[\Phi\left[t - \frac{T}{2}\cdot(1 + d\cdot 2)\right] - \Phi(t - T)\right] \qquad (22)$$

Where Φ(t)=unit step function, T=Tline and d=5%. The "d" term in (22) can be varied either to maximize or minimize this distortion effect. Experimental results show that at 60Hz line, "d" ranges inversely from 3% at 230 VRMS to 5% at 85V RMS input line with a typical boost inductor value of 400uH at an input power of roughly 1200W. This is also with a 2.2uF capacitor on the DC side of the rectifier bridge. The plot in Fig. 5 is for d=5%.

B. 400Hz/600Hz Zero-Crossing Modeling

Though our experimental results presented in this paper focus exclusively on the 50Hz/60Hz case, a proposed method of modeling the zero-crossing distortion at the higher line frequencies is also presented for completeness. For higher line frequencies it is recommended that one apply the findings stated in [13] before proceeding with the modeling process. Typically, higher line frequencies are employed in airborne equipment and follow the stringent RTCA/DO-160E EMC standard [15]. Because distortion generally worsens with the increase of line frequency, it is usually quite difficult to meet this requirement. Thus in order to correctly assess the harmonics associated with this type of application, it is critical that an accurate distortion model be presented. We will use a multiplying function that can realistically take into account the delayed input step current along with its associated ring response. The general form of this step function is expressed in (23). The first term of d2f(t) is represented by f1(t), or the

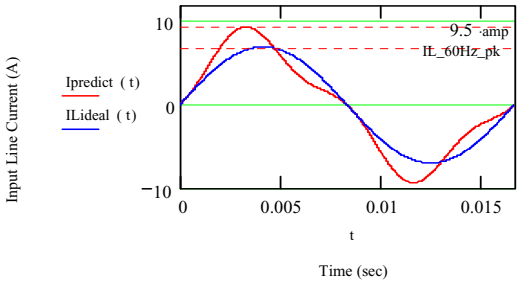

Figure 4. Predicted Input Line Current Vs Ideal Case over a full 60Hz line cycle.

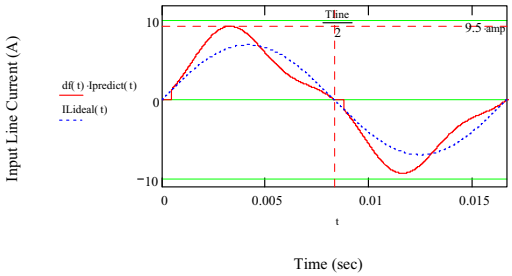

Figure 5. Predicted Input Line Current Vs Ideal Case with zero-crossing distortion.

dead-zone portion, and the 2nd term is represented by a damped sinusoidal response that is time shifted by f2(t) as defined in Table I. The values used for constants $\alpha, \beta, \omega r, \theta$ and "d" will depend on the damping ratio of the inner current loop as well as the phase lead of the input current at the bridge rectifier. It is thus left as a separate exercise for one to design a routine which extracts all of the necessary parameters, as exemplified by those shown in Table I, for a given bridge rectifier capacitance and current loop compensator design. This is necessary before proceeding with (23) below.

$$d2f(t) := f1(t) + (\alpha \cdot e)^{-(t - d \cdot Tline) \cdot \beta} \cdot \sin(\omega r \cdot t - \theta) \cdot f2(t) \quad (23)$$

The V1(t) and V2(t) waveforms shown in Fig. 6 illustrate one example of this new distortion model with its associated input current (of arbitrary amplitude) for the values given in Table I after Fourier transformation. This excludes the effects of feed-forward and feedback distortion. We are using a 1200 Hz base frequency for the distortion function since there are two zero-crossings per full 600 Hz line cycle (the "convergence tolerance" in MathCAD is set to 10E-8 for best results). Not surprisingly, the harmonics associated with the ring frequency, ωr, is the most problematic (producing significant 12th harmonic for this particular example).

Finally, one should note that there is an inherent limitation of the Fourier series method when modeling jump discontinuities or step functions. The effect is what is known as "Gibbs phenomenon" [16]. This results in a very low level decaying oscillation, predominantly near the transition edges of (22) with the frequency of this oscillation being dependent upon the number of harmonics used in the Fourier integral.

Recent research in this area has shown that there are methods for eliminating the "Gibbs" effect altogether. This involves the change of mathematical basis to a different set of orthogonal polynomials called "Gegenbauer polynomials" [17]. However for our application this effect is very small so there does not appear to be a need to modify the approach proposed here.

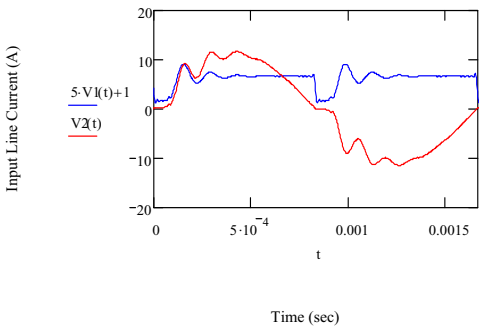

Figure 6. Input Line Current with the zero-crossing multiplier over a full 600Hz line cycle. These waveforms are generated after the Fourier transform of 40 harmonics using Table I constants. The ringing step waveform, V1(t), is scaled and slightly shifted from zero for illustration purposes only.

TABLE I
Fig. 6 Parameters

$\omega r := 2 \cdot \pi \cdot 7200 \quad d := 0.09 \quad \theta := d \cdot 20 \cdot \pi$

$Tline := 833 \cdot \mu \quad \alpha := 2 \quad \beta := 5000$

$f1(t) := 1 - (\Phi(t) - \Phi(t - d \cdot Tline))$

$f2(t) := \Phi(t - d \cdot Tline) - \Phi(t - 1 \cdot Tline)$

VI. INPUT DISTORTION AND IEC61000-3-2

Now for the last stage of our analysis we will determine the harmonic levels of our input line current shown in Fig. 5 (using the values in section IV for d=5%) and compare it against the IEC61000-3-2 limits listed in Table 1 using (24).

$$dist_k := \frac{1}{Tline} \cdot \int_{0 \cdot sec}^{Tline} Ipredict(t) \cdot df(t) \cdot e^{-j \cdot k \cdot 2 \frac{\pi}{Tline} \cdot t} dt \quad (24)$$

We can write the periodic expression for the predicted input line current Iin(t) using the time domain expansion (25) and verify it against actual currents on the input line.

$$Iin(t) := \sum_k \left(2 \cdot Re(dist_k) \cdot \cos\left(2 \cdot k \frac{\pi}{Ts} \cdot t\right)\right) - \sum_k \left(2 \cdot Im(dist_k) \cdot \sin\left(2 \cdot k \frac{\pi}{Ts} \cdot t\right)\right) \quad (25)$$

$$dist\_rms_k := dist_k \cdot \sqrt{2} \quad (26)$$

The final two equations are power factor (27) and THD (28) [18]. This is now a straight forward calculation since we have characterized Iin(t) along with its harmonics. We will compare these results with actual measurements to verify convergence. For error checking we can heavily filter our loops with 10uF caps for C1, C2 and Cf with d set to 0%. We should confirm that Iin(t) approaches a pure sinewave, $dist\_rms_1 \Rightarrow Pin/Vin$, THD⇒0% and PF⇒1. This checks a significant amount of math.

$$PF := \frac{Pin\_pfc}{\sqrt{\frac{2}{Tline} \cdot \int_{0 \cdot sec}^{\frac{Tline}{2}} Iin(t)^2 dt \cdot Vin}} \quad (27)$$

$$THD := \frac{\sqrt{\sum_{k=2}^{40} \left(|dist_k|\right)^2}}{|dist_1|} \quad (28)$$

Table II Class A Equipment:

Harmonic Order (n)	Maximum permissible harmonic current (Amperes)
	Odd Harmonics
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
15 <= n <= 39	0.15 x (15/n)
	Even Harmonics
2	1.08
4	0.43
6	0.30
8 <= n <= 40	0.23 x (8/n)

We can now plot the harmonic levels of the input current waveform shown in Fig. 7 and Fig. 8. Since the IEC limits are measured in RMS we must be careful to apply the necessary conversion factor (26). This frequency response represents the Fourier series transform of the waveform shown in Fig. 5. As can be seen in the graph, there is significant 3rd harmonic. This is mainly due to the feedback loop component values since the feed-forward values for C1 and C2 are 1uF for this example. These are fairly large feed-forward caps and result in a good amount of filtering. In fact, careful consideration must be paid to these feed-forward values since there are higher order harmonics associated with the sharp edges of the rectified line.

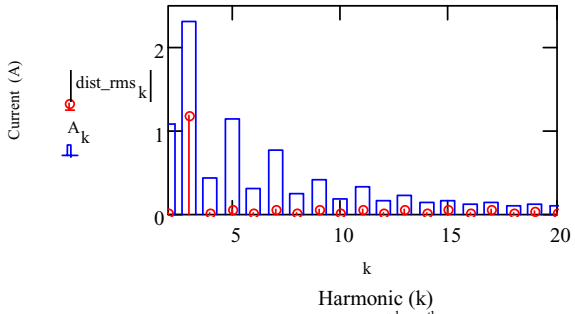

Figure 7- Frequency spectrum (2nd-20th harmonic) of Ipredict

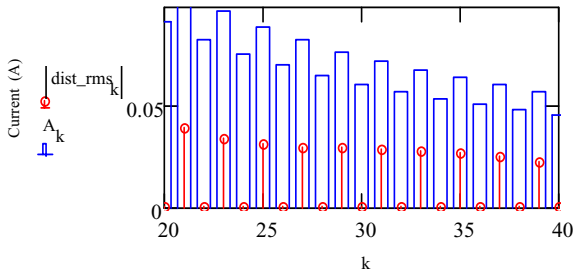

Figure 8- Frequency spectrum (20th-40th harmonic) if Ipredict

VII. EXPERIMENTAL RESULTS

In order to determine the accuracy of our method, we will compare our results for 2 cases. Case 1 is where we force the feedback loop to dominate the distortion and Case 2 is where the feed-forward dominates. We will deliberately use part values that will significantly distort the input line current to see plainly whether we have good convergence between predictions and actual results with an ordinary oscilloscope.

CASE 1 (Feedback Dominant Case):
Pin=1205 W; Vin=230 VRMS; Vo=400V; d=3%, 60Hz, Co=1344uF; Rac=903K OHM, Rprog=7.5K OHM, e=94%, Rshunt=0.025 OHM; *Feed-Forward Component Values:* R1=282K; R2=15K, R3=7.5K, C1=1uF; and C2=1uF;
Feedback Component Values:
R5=10K; R4=790K; Rf=221K;Cf=2200pF
Power Factor:
Predicted P.F.=0.891 Measured P.F.=0.912
Percent Deviation- Delta<2.4%
Total Harmonic Distortion:
Predicted THD=20.74% Measured THD=21.36%
Percent Deviation- Delta<3%.

Note in Fig. 9 the peak current (9.6A) closely correlates to the prediction in Fig. 10 (9.3A peak on CH1), though there's a slight fundamental phase shift between the predicted and actual results. This is probably due to the input filter. In general we are getting excellent correlation for this condition.

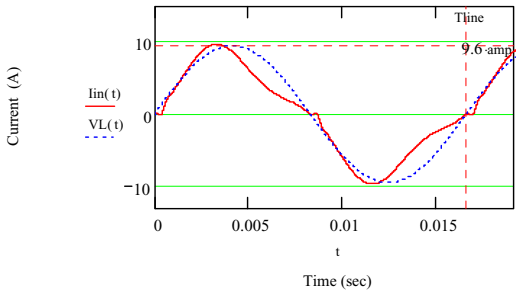

Figure 9. Predicted Input Line Current Vs input voltage over a full 60Hz line cycle. The input line voltage shown above is scaled to match the peak of Iin(t) for easy comparison with Fig. 10 below.

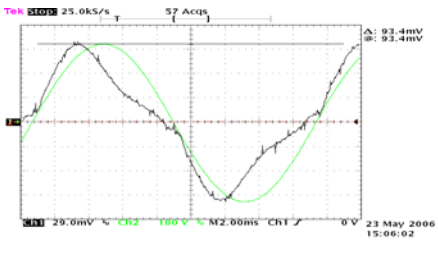

Figure 10. Case 1; Actual Input Line Current Iin(t) over a 60Hz line cycle. Ch1=100A/Volt; CH2 = Input line voltage at 100V/Div.

CASE 2 (Feed-forward Dominant Case):
Pin=1205 W; Vin=230 VRMS; Vo=400V;d=3%, 60Hz; Co=1344uF; Rac=903K OHM, Rprog=7.5K OHM,e=94%, Rshunt=0.025 OHM, Feed-Forward Component Values: R1=282K; R2=15K;R3=7.5K;C1=0.1uF; and C2=0.1uF; Feedback Component Values:
R5=10K; R4=790K; Rf=221K;Cf=1uF;
Power Factor:
Predicted P.F.=0.835 Measured P.F.=0.844
Percent Deviation- Delta<1.2%
Total Harmonic Distortion:
Predicted THD=32.2% Measured THD=32.84%
Percent Deviation- Delta<2%

For this case again the predicted peak line current in Fig. 11 (11A) closely correlates to the actual value in Fig. 12 (10.7A on CH1). We still see the phase shift as before. We are getting excellent correlation for this condition as well.

VIII. CONCLUSION

In this paper, a mathematical approach for analyzing the input line current harmonics for PFC converters was proposed. Time domain expressions for the various signals present at the feedback and feed forward loops, among other important locations, were presented. Power factor and THD were also calculated. Finally, the input current was plotted via the use of the Fourier series method, in the frequency domain and compared against the IEC61000-3-2 limits up to and including the 40th harmonic of line frequency. Our experimental results of the input current waveform, THD and power factor showed very tight correlation of <3% worst-case from theoretical predictions.

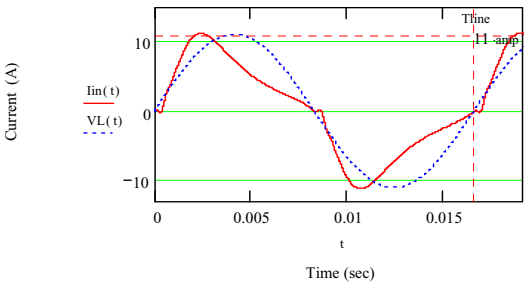

Figure 11. Predicted Input Line Current Vs Input Voltage (scaled such that it's peak coincides with Iin peak for easy comparison to fig. 12).

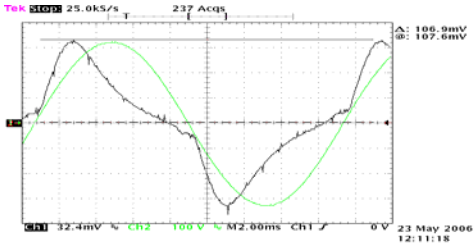

Figure 12. Case 1; Actual Input Line Current Iin(t) over a full 60Hz line cycle. Ch1=100A/Volt; CH2 = Input line voltage at 100V/Div.

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