Development of a High-PF Two-Phase Flyback Converter Based on Chasing

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***Abstract*- In this paper, a high-power-factor (high-PF) two-phase flyback converter based on current chasing without any current sharing required is presented herein, which is realized using two L6561 ICs together with a field programmable gate array (FPGA) technique. By doing so, not only the power factor (PF) and the total harmonic distortion (THD) are improved but also the output power is upgraded. Some experimental results are provided to demonstrate the proposed control scheme.**

I. INTRODUCTION

Conventionally, the AC-DC converter with power factor correction (PFC) runs in the continuous current mode (CCM) or discontinuous current mode (DCM). Under CCM, the ripple current is small and hence the core loss is reduced, and moreover, the electromagnetic noise and the input filter size are also decreased. However, the main power switch is turned on at the instant that the current flowing through the inductance is not zero, thereby requiring the voltage-boosting diode with fast reverse recovery time to avoid considerable switching loss occurring in the main power switch. Besides, there are some disadvantages under such control, such as high-value inductance increasing the volume of the inductor, complexity in control, etc. On the other hand, if the AC-DC operates in DCM, then there is no need of high-value inductance, and there is also no consideration of specifications of the reverse recovery current of the voltage-boosting diode, thereby rendering the diode to be cost down. However, in this case, the high peak current tends to flow through the main power switch and the high current ripples appear at the input and output, thereby not only increasing the total harmonic distortion (THD) but also reducing the capacitor life. Consequently, the AC-DC converter with PFC operating in the critical condition mode (CRM) has been addressed [1-4], which possesses the advantages of CCM and DCM and is widely used in industry. But, the output power of the AC-DC converter operating in the CRM is limited to some extent, and hence, two-phase interleaved control applied to the AC-DC converter is presented to enlarge its output power capability. In [5-10], the two phases of the AC-DC converter operates in CCM under the fixed switching frequency with the interleaved phase of 180 degrees, and as for [11], the two phases of the converter runs in DCM under the fixed switching frequency with the fixed interleaved phase of 180 degrees. But regarding [12], one phase of the converter works as a master in CRM under the variable switching frequency and the other phase playing a role of a slave must be operated in DCM to obtain the fixed interleaved phase of 180 degrees, thus causing complexity in control.

However, in this paper, a novel control topology based on chasing is presented, and this makes the two phases of the converter operate in CRM with random interleaved phase automatically applied, without any master or slave. Such a control topology is to be applied to the flyback converter to obtain the high PF as well as large power. Some experimental results are provided to demonstrate the proposed control topology.

II. PROPOSED OVERALL SYSTEM CONFIGURATION

Fig. 1 shows the proposed high-PF two-phase flyback converter with interleaved control automatically applied. This converter operates under voltage-mode control. The control effort created from the voltage compensator is sent to the primary side via the photo-coupler and then directly passed to two L6561s. Therefore, there are the same current commands in these two L6561s. Two L6561s have individual zero-current detectors and switching frequencies. But the signals M_1 and M_2 created from the two L6561s are modified to the gate driving signals PWM_1 and PWM_2 according to the proposed control rules, so as to obtain the required duty cycles to drive the main power switches S_1 and S_2 respectively, to be mentioned later.

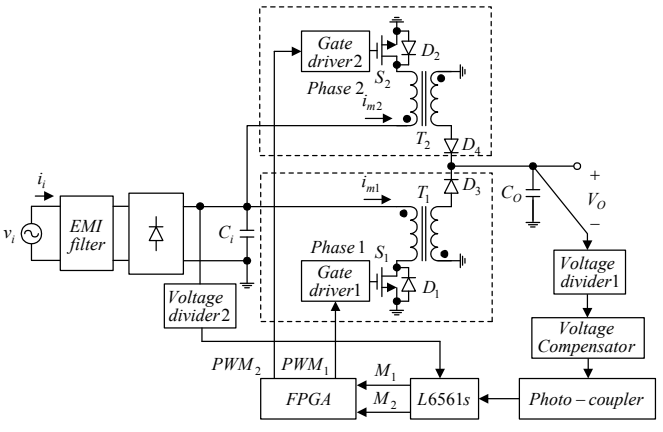

Fig. 1 Block diagram of the proposed overall system configuration.

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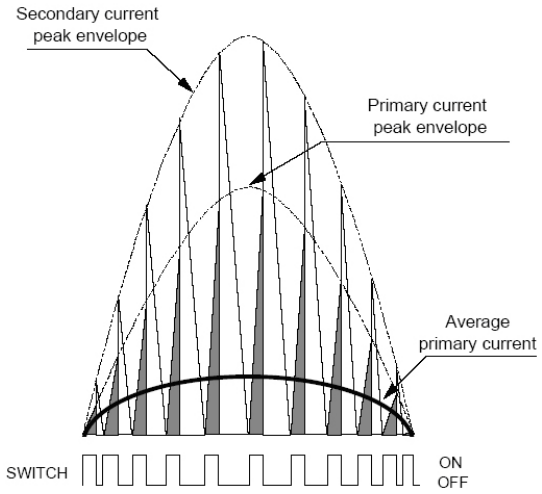

Fig. 2. Current waveform of the PF single-phase flyback converter.

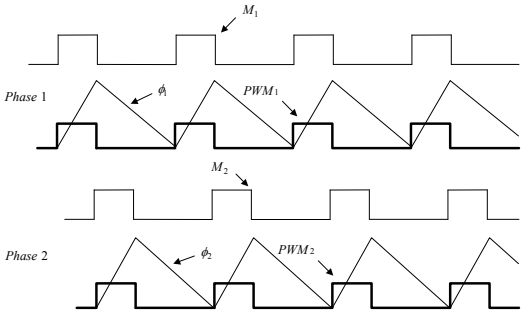

Fig. 3. Control topology at the maidanglao wave crest.

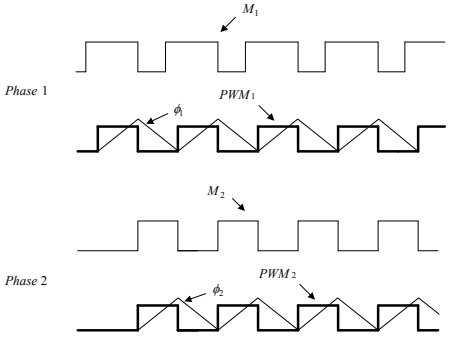

Fig. 4. Control topology at the maidanglao wave trough.

III. Mathematical Derivative

The following mathematical derivative is initially based on CRM. For the PF single-phase flyback converter to be considered, as this converter operates in CRM with the bandwidth of the voltage loop far from lower than that of the main, the turn-on period of the PWM gate-driving signal is kept constant at some value, as shown in Fig. 2.

$$T_{on} = \frac{L_p \times i_m(\omega t)}{v_i(\omega t)} = \frac{L_p \times I_m}{V_m}. \tag{1}$$

where T_{on} is the turn-on period of the PWM gate-driving signal for the main power switch, L_p is the self inductance at the primary, v_i is the input AC voltage, i_m is the current flowing through L_p, ω is the radian frequency of the main, V_m is the peak value of v_i and I_m is the peak value of i_m.

$$t_{off} = \frac{L_p \times I_m \times \left|\sin(\omega t)\right|}{n \times (V_O + V_F)}. \tag{2}$$

where t_{off} is the time duration between the instant of turning off the main power switch and the instant of detecting the current flowing through the diode at the secondary to be zero, n is turns ratio, V_O is the DC output voltage, V_F is the voltage across the forward-biased diode at the secondary.

$$t_s = T_{on} + t_{off} = \frac{L_p \times I_m}{V_m} \times \left[1 + \frac{V_m}{V_R} \times \left|\sin(\omega t)\right|\right]. \tag{3}$$

where $V_R = n \times (V_O + V_F)$ and V_R is the voltage reflected from the secondary to the primary.
Therefore, the variable switching frequency can be expressed as follows.

$$f_s = \frac{V_m}{L_p \times I_m} \times \frac{1}{1 + \frac{V_m}{V_R} \times \left|\sin(\omega t)\right|}. \tag{4}$$

And then, the minimum switching frequency can be obtained as follows.

$$f_{s-\min} = \frac{V_m}{L_p \times I_m} \times \frac{1}{1 + \frac{V_m}{V_R}}. \tag{5}$$

And also, the corresponding duty cycle D varied with the main is shown below.

$$D = \frac{T_{on}}{t_s} = \frac{1}{1 + \frac{V_m}{V_R} \times \left|\sin(\omega t)\right|}. \tag{6}$$

However, unlike the PF single-phase flyback converter, the PF two-phase flyback converter works with two L6561s operating independently, and hence the turn-on period of the PWM gate-driving signal for each phase can not be kept constant at some value. Consequently, applying the proposed control strategy to the PF two-phase flyback converter, the turn-on period of the PWM gate-driving signal for each phase can be kept constant at some value, without any current sharing loop required. Therefore, the formulas mentioned above for the PF single-phase flyback converter can be applied to the PF two-phase flyback converter with the proposed control strategy.

IV. Proposed Control Strategy

The following is to talk about the proposed control rules and the duty cycle determination. And, there are two basic control rules to be described as follows.

A. Basic Control Rules

1) Rule 1

If the current of any phase reaches the current command, then the corresponding main power switch is turned off.

2) Rule 2

If the current of one phase flowing through the diode at the secondary has been detected to be zero and that the other phase is turned off is made sure, then one phase is turned on, so as to avoid overlapping of the duty cycles of two phases and hence to decrease the current ripple.

Based on the basic two control rules mentioned above, the detailed procedures for creating gate driving signals PWM_1 and PWM_2 are described as follows. Since two L6561s operate independently, they have individual zero current detectors and switching frequencies. The duty cycles created from two L6561s are sent to FPGA and modified according to two basic control rules mentioned above, so as to determine turn-on instants and turn-on durations. For the L6561 of phase 1 to be considered, as soon as the current flowing the diode at the secondary is detected, the level of the signal M_1 is forced to be high, but not passed to render the main power switch S_1 turned on until FPGA makes sure that phase 2 is OK based on rule 2. That is to say, if phase 2 is not OK, then phase 1 considers that the current flowing through phase 2 does not reach the current command and the signal M_1 is not sent to S_1 to drive S_1, whereas if phase 2 is OK, then the gate-driving signal PWM_1 modified from M_1 by FPGA is sent to S_1 to drive S_1, the corresponding inductance current is rising until it reaches the current command, and hence S_1 is turned off. As for the L6561 of phase 1 to be considered, the analysis is the same as that mentioned above. Actually, the turn-on instant and the turn-on duration for each main power switch are determined by L6561 and FPGA, and basically, the proposed control rules are strongly influenced by the duty cycle. And there are two cases to be described as following.

B. Duty Cycle Determination

1) Case 1: Duty cycle is smaller than 50%

As illustrated in Fig. 3, this happens at the maidanglao wave crest of the input voltage. Since the input voltage in this case is in the neighborhood of the maximum value, the corresponding duty cycle is small. The duty cycles of the signals M_1 and M_2 outputted from L6561s are almost not overlapped, that is to say, M_1 and M_2 are equal to PWM_1 and PWM_2 separately. Even though they are overlapped, they are separated after the process by FPGA and modified to PWM_1 and PWM_2.

2) Case 2: Duty cycle is larger than 50%

As described in Fig. 4, this happens at the maidanglao wave trough of the input voltage. Since the input voltage in this case is in the neighborhood of the minimum value, the resulting duty cycle is over 50%, that is to say, the duty cycles of M_1 and M_2 are overlapped. But based on the proposed control rule 2, FPGA will try to separate them. To explain further, the level of the corresponding signals M_1 and M_2 will be automatically changed to the high level as soon as any L6561 detects zero current flowing through the diode at the secondary, and changed to the low level until the current reaches the current command. But FPGA will do some modifications of these signals so as to determine the turn-on instants of the main power switches, i.e. to create suitable gate driving signals PWM_1 and PWM_2. In this case, each phase wants to extend its duty cycle to over 50%. However, based on the proposed control rule 2, the maximum duty cycle for each phase is limited to 50%.

V. Experimental Results

Before entering into this section, there are some specifications given as follows: (i) rated AC input voltage is $110V_{rms}$; (ii) rated DC output voltage is 12V; (iii) rated output current is 5A; (iv) product name of two transformers is 3C92 EFD-20 made by Philips; (v) turns ratio of each main power switch is 76:14 with primary inductance about 360μH ; (vi) product name of two output capacitors in parallel is ZLH series with 16V/ 2700μF made by Rubycon; (vii) product name of two main power switches is SPD03N60S5 made by Infineon; (viii) product name of two rectification diodes is 50WQ10FN made by IR; (ix) product name of FPGA is Cyclone series with EP1C3T100 made by Altera; and (x) product name of one full-bridge rectifier is DF04 with 1A/400V made by IR.

The following waveforms are all measured in the same circuit under the rated output power, so as to remove the effect of parameter variations on experiments. Fig. 5 shows the input voltage and the input current under the rated load with PF of 0.98, based on the proposed chasing interleaved PFC control strategy. Fig. 6 illustrates the voltage in the neighborhood of the high input voltage, the corresponding input currents of phase 1 and phase 2, whereas Fig. 7 displays the input voltage and the input current under the rated load with PF of 0.96, without the proposed control scheme but with the same gate driving signals for two main power switches. Fig. 8 describes the voltage in the neighborhood of the high input voltage, the corresponding input currents of phase 1 and phase 2. From the results mentioned above, it is obvious that the input current ripple and the voltage ripple with the proposed control scheme are smaller than those without proposed control scheme. Under the same conditions shown in Figs. 5 and 7 except that the input voltage in the neighborhood of the low input voltage, it is obvious that there is a negligible difference in input voltage ripple due to low primary currents, as shown in Figs. 9 and 10.

To explain Further, Figs. 11 and 12 show the L6561 signals M_1 and M_2 and the gate driving signals PWM_1 and PWM_2 with the proposed control scheme in the neighborhood of the high input voltage and the low input voltage respectively. Evidently, in the neighborhood of the high input voltage shown in Fig. 11,

the signals PWM_1 and PWM_2 are almost the same as the signals M_1 and M_2 due no overlap between them for most of the time. Even though the duty cycles of the signals M_1 and M_2 are overlapped, the duty cycles of the gate driving signals PWM_1 and PWM_2 are immediately separated after FPGA process. Since the proposed chasing interleaved control strategy makes the converter operate under random interleaved angles and various switching frequencies, the corresponding spectrum is dispersed and suppressed.

On the other hand, in the neighborhood of the low input voltage shown in Fig. 12, although the duty cycles of the L3561 signals M_1 and M_2 are different and overlapped, the duty cycles of the gate driving signals PWM_1 and PWM_2 are close to 50% and interleaved by 180^0 after FPGA process, implying that the switching frequencies for two phases in this case are almost the same and held constant at same value. Besides, from Figs. 11 and 12, it is obvious that each phase has its fixed turn-on duration via the proposed control scheme, thus the formulas for the PF single-phase flyback converter, mentioned in Sec. III, can be applied to the PF two-phase flyback converter with the proposed control strategy.

Furthermore, Fig. 13 shows comparison of the harmonics of the input current between without and with the proposed control strategy. It is obvious that the third harmonic is reduced significantly based on the proposed control scheme, thereby causing the total harmonic distortion (THD) to be 15.4%, which is lower than 19.7% created from without the proposed control scheme.

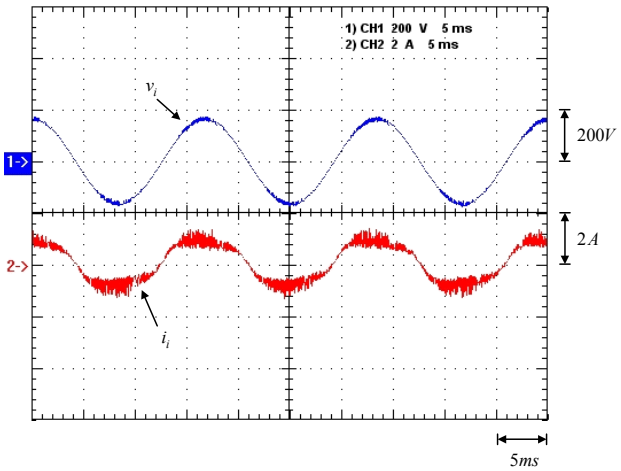

Fig. 5. Input voltage v_i and input current i_i under the rated load with the proposed chasing interleaved PFC control strategy.

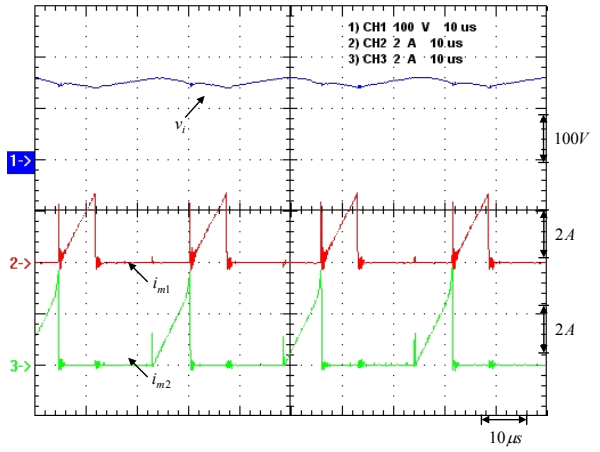

Fig. 6. Input voltage v_i, phase 1 primary current i_{m1} and phase 2 primary current i_{m2} in the neighborhood of the high input voltage corresponding to Fig. 5.

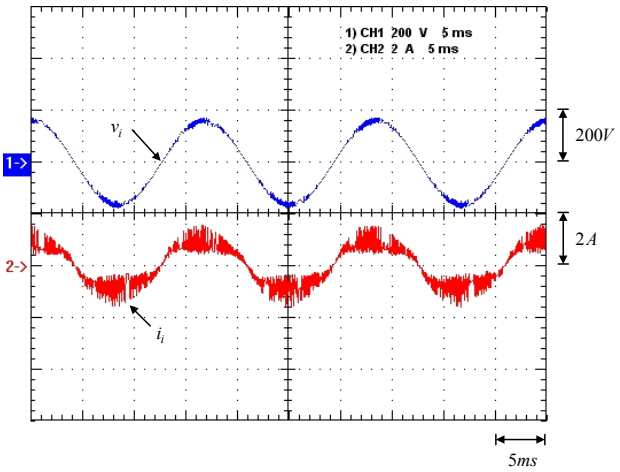

Fig. 7. Input voltage v_i and input current i_i under the rated load without the proposed chasing interleaved PFC control strategy.

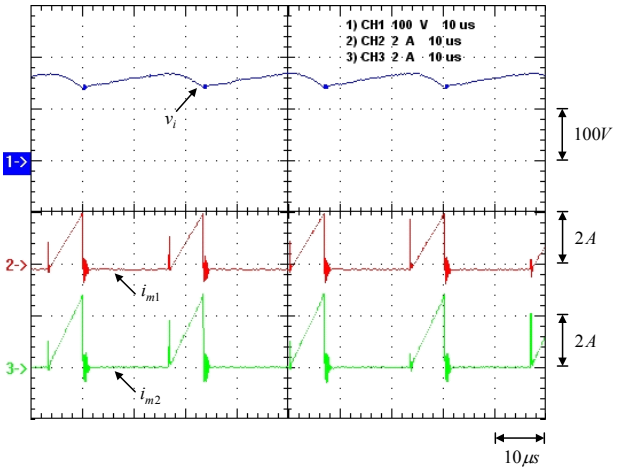

Fig. 8. Input voltage v_i, phase 1 primary current i_{m1} and phase 2 primary current i_{m2} in the neighborhood of the high input voltage at corresponding to Fig. 7.

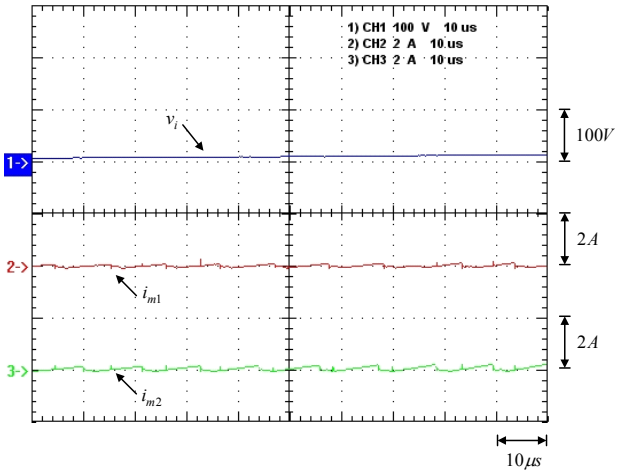

Fig. 9. Input voltage v_i, phase 1 primary current i_{m1} and phase 2 primary current i_{m2} in the neighborhood of the low input voltage corresponding to Fig. 5.

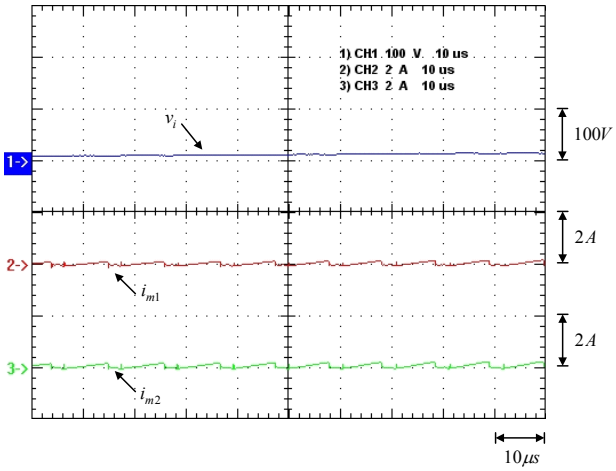

Fig. 10. Input voltage v_i, phase 1 primary current i_{m1} and phase 2 primary current i_{m2} in the neighborhood of the low input voltage associted to Fig. 7.

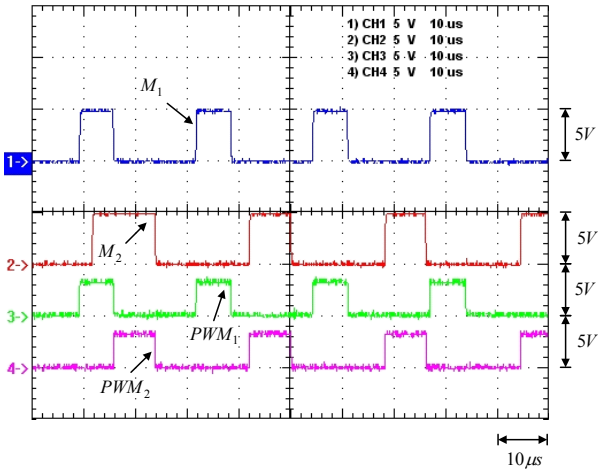

Fig. 11. M_1, M_2, PWM_1 and PWM_2 in the neighborhood of the high input voltage.

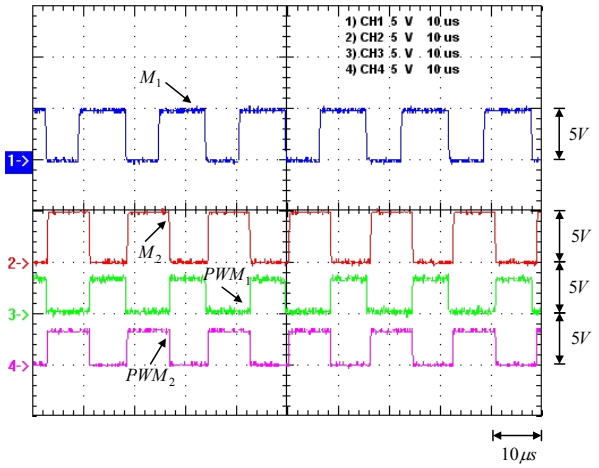

Fig. 12. M_1, M_2, PWM_1 and PWM_2 in the neighborhood of the low input voltage.

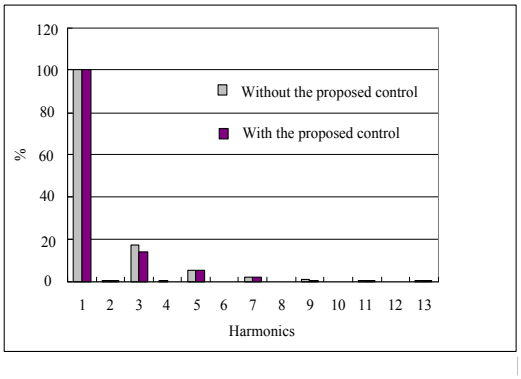

Fig. 13. THD comparison.

VI. Conclusion

A two-phase flyback converter based on chasing without current sharing added are presented to enhance the output power capability. At the same time, the converter with the proposed control strategy has higher PF due to reduction of the third harmonic, as compared with the converter without the proposed control strategy.

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