A Design of Single Phase Converter with Active Power Factor Correction Module

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***Abstract*--According to the requirement of the power factor and the dynamic performance of the asynchronous machine tool field, an asynchronous motor inverter with active power factor correction is proposed. The proposed inverter is a 3kW asynchronous motor drive control platform. At first, the proposed single phase converter with APFC is realized by using the MATLAB/SIMULINK. Then, the boost APFC is designed based on the UC3854. Finally, in rated load conditions, experimental results about the power factor and the dynamic performance highlight the effectiveness of the APFC module.**

***Index Terms*—Active power correction module, Power factor, Matlab/Simulink, UC3854.**

I. INTRODUCTION

The current industrial general inverter has low power factor (about 0.6~0.7), large harmonic pollution and serious harm to power grid. With the development of frequency conversion technology, the APFC circuit is more and more applied to the power supply circuit. In those kind of inverters, the ripple current of APFC circuit is smaller and the output voltage is more stable. Meanwhile, it can greatly reduce output ripple voltage, which could prolong the lifetime of the capacitor.

The fundamental theory and control methods of the APFC are introduced[1]. It analyzes and studies the APFC based on the average current control single-phase Boost type APFC circuit.

The boost interleaved converter has the advantage of paralleled semiconductors. It also reduces output capacitor high frequency ripple, but it still has the problem of heat management for the input diode bridge rectifiers [2][3].

Several PFC topologies were introduced, depending on the required source-load characteristics and system performance[4]. The comparative study of the most popular PFC converters is proposed, with an emphasis on their major features, their benefits and limitations in terms of performance. More specifically, the averaged model of each topology is presented, on the basis of which steady-state characteristics, current tracking ability and design criteria are elaborated and analyzed.

In this paper, a chip UC3854 was used to realize the control of APFC module. The chip UC3854 provide all the functions necessary for APFC preregulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to that of AC input line voltage. Average current mode control maintains stable, low distortion sinusoidal line current without the need for slope compensation, unlike peak current mode control[8].

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II. PRINCIPLE

A. System Structure

As shown in Figure 1, the system includes the rectifier module, APFC module, inverter module, etc. The APFC is shown in Figure 2. It is the boost main circuit with feedback system using the average current control strategy. By this way, it is effective to reduce the current ripple and the EMI.

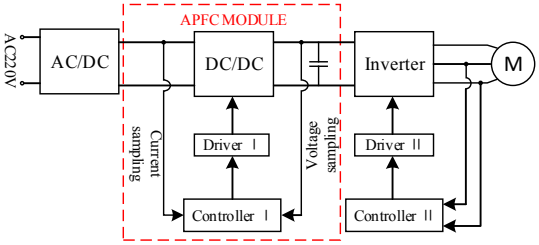

Fig.1 System configuration

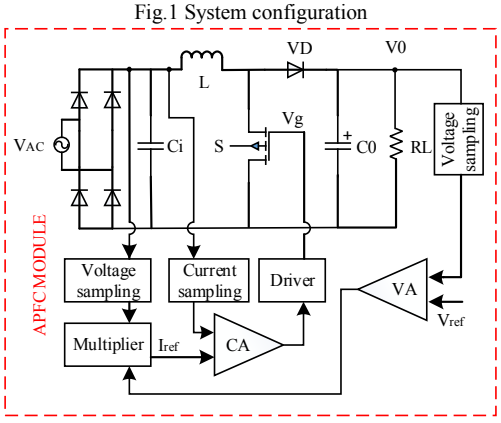

Fig.2 Structure diagram of APFC

The main circuit topology is usually brought out with DC-DC converter. The main circuit topology is consisted of Buck, Boost, Cuk, and Flyback circuit. Buck circuit is only used reduced voltage situation. Cuk circuit is complex. Flyback circuit is usually used in low power application.

The advantages of Boost APFC are as follows:

- The input current is continuous and easy filtering.
- It can be used in high power application and realize a higher power factor in the range of all input voltage.
- The output voltage is higher than the input.

In this paper, the average current control mode is used.

The advantages of this way are as follows:

- The fixed switching frequency.
- The low total harmonic distortion (THD) and EMI.
- The high efficiency.

B. Modeling and Control of the Boost APFC

In this paper, the main circuit is the Boost-type circuit, and the control circuit uses the average current mode control of voltage and current double closed loop. The control of current closed loop makes the rectified current track automatically the input voltage and improve the power factor. The control of voltage closed loop make the output voltage keep stable.

The Structure diagram of the APFC current closed loop is shown in Figure 3.

Fig.3 The Structure diagram of the APFC current closed loop

The transfer function of the current compensation circuit:

$$G_{CA}(s) = k_{cp} + \frac{k_{ci}}{s} \tag{1}$$

The transfer function of the PWM driver circuit:

$$G_{PWM}(s) = \frac{1}{V_{PP}} \tag{2}$$

The transfer function of the power stage of Boost circuit:

$$G_P(s) = \frac{V_S(s)}{D_{\text{on}}(s)} = \frac{V_0 \times R_s}{sL} \tag{3}$$

Where V_{PP} is the peak-to-peak value of reference sawtooth in the PWM driver circuit, V_0 is the output voltage of the Boost circuit, R_s is the samping resistor, L is the Boost inductance.

The Structure diagram of the APFC voltage closed loop is shown in Figure 4.

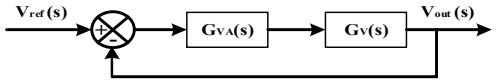

Fig.4 The Structure diagram of the APFC voltage closed loop

The transfer function of the voltage compensation circuit:

$$G_{VA}(s) = k_{vp} + \frac{k_{vi}}{s} \tag{4}$$

The transfer function of the Boost stage:

$$G_V(s) = \frac{P_o}{C \times V_o \times \Delta V_{VEA} \times s} \tag{5}$$

Where P_0 is the output power of the Boost circuit, C is filter capacitance of the Boost circuit, ΔV_{VEA} is the output voltage range of the voltage compensation circuit.

III. SIMULATION

A. The Boost main circuit design

The following table shows the requirements of APFC module.

TABLE I
THE DESIGN REQUIREMENT OF APFC MODULE

The design requirement	The value of the parameters
Input AC voltage	198~242V
Grid frequency	49~51Hz
Switching frequency	50kHz
Output DC voltage	351~429V
Output power	3kW
The power factor	PF>0.99
Total harmonic distortion factor	THD<10%

According to the principle of the boost circuit, the boost inductance calculation is as follows:

$$L = \frac{V_{in} D_{\max}}{f_s \Delta I} \tag{6}$$

Where V_{in} is the input voltage, $D_{\max}$ is the biggest duty ratio, f_s is the switching frequency, ΔI is the input ripple current.

Calculate the maximum peak line current I_{peak}. where P_{in} is the input power which is equal to the output power P_{out}.

$$I_{peak} = \frac{\sqrt{2} P_{in}}{V_{in(\min)}} \tag{7}$$

In this paper, when the input current maximum is required to limit the ripple current in the 20% range.

$$\Delta I = 20\% I_{peak} \tag{8}$$

Determine the biggest duty ratio $D_{\max}$, where $V_{in(peak)}$ is the peak of the rectified line voltage at low line.

$$D_{\max} = \frac{V_o - V_{in(peak)}}{V_o} \tag{9}$$

According to the above formula, you can calculate the inductance $L = 0.5mH$.

The DC output flat wave capacitor calculation is as follows:

$$C = \frac{2 P_{out} \Delta t}{V_o^2 - V_1^2} \tag{10}$$

Where P_{out} is the output power, Δt=30ms is the maintain time, V_0 is the output voltage of the APFC module, V_1 is the minimum output voltage which is 311V, you can obtain the required capacitance is 3250 uF.

B. The Boost APFC simulation based on MATLAB

Fig.5 is the input voltage and current of the Boost circuit without APFC under 3kW load.

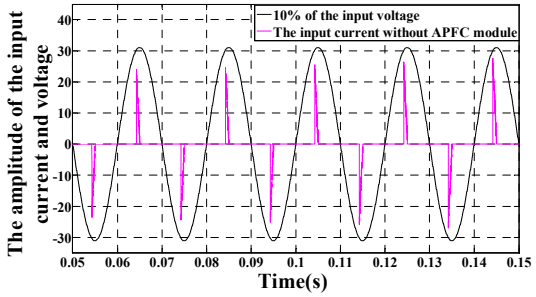

Fig.5 The input voltage and current of the Boost circuit without APFC

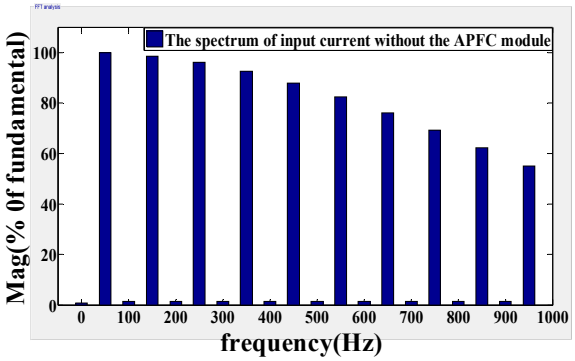

Fig.6 The histogram of the input current harmonic analysis

Fig.6 is a histogram of the input current harmonic analysis. Select the fundamental frequency of 50Hz, analyzes the harmonic spectrum of 1 to 20, we can see the bigger harmonic content.

Fig.7 is the input voltage and current of the Boost circuit with APFC under 3kW load. From the figure can be seen: the input current and input voltage is substantially the same phase. Fig.8 shows that the output voltage waveform.

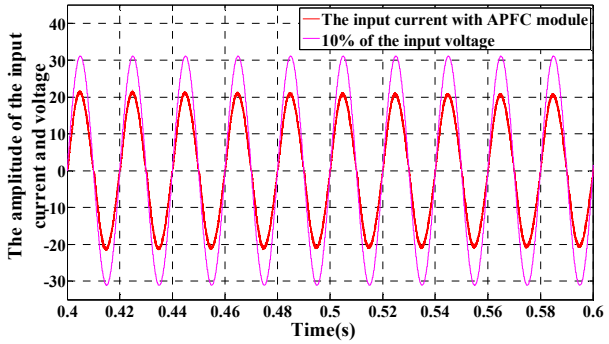

Fig.7 The input voltage and current of the Boost circuit with APFC

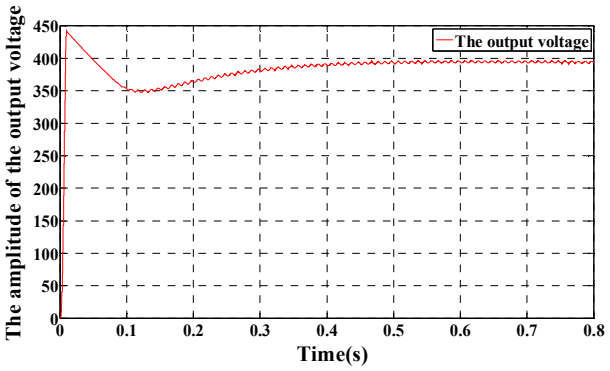

Fig.8 The output voltage waveform

IV. System Design and Experiments Results

A. *The control circuit design based on the chip UC3854*

According to the requirements of APFC module, specifications as shown in table Ⅰ. There are several steps to gain the parameters of the Boost APFC control circuit system as follows.

Voltage loop is made of the type Ⅱ compensation circuit. C_{vf} is the feedback capacitance; R_{vf} is the feedback resistor; V_{ref} is the reference voltage.

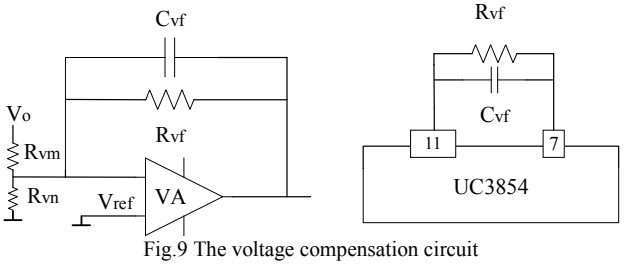

Fig.9 The voltage compensation circuit

The output the second harmonic ripple voltage is given by the following equation.

$$V_{o(pk)} = \frac{P_o}{2\pi \times 2f \times CV_o} \tag{11}$$

Amplifier output ripple voltage and gain. $V_{o(pk)}$ must be reduced to the ripple voltage allowed at the output of the voltage error amplifier.

$$G_{va} = \frac{\Delta V_{vao} \times 1.5\%}{V_{o(pk)}} \tag{12}$$

Feedback network values. Find the component values to set the gain of the voltage error amplifier. The value of R_{vm} is reasonably arbitrary. Choose $R_{vm} = 511k\Omega$.

$$C_{vf} = \frac{1}{2\pi(2\times f)\times R_{vm}G_{va}} \tag{13}$$

$$R_{vn} = \frac{R_{vm}V_{ref}}{V_o - V_{ref}} \tag{14}$$

Calculate the unity gain frequency of voltage loop f_{va}.

$$f_{va}^{\ 2} = \frac{P_{in}}{\Delta V_{vao} V_o R_{vm} C C_{vf} (2\pi)^2} \tag{15}$$

The value of R_{vf} is:

$$R_{vf} = \frac{1}{2\pi f_{va} C_{vf}} \tag{16}$$

In order to make system work stably, the current loop must be compensated.

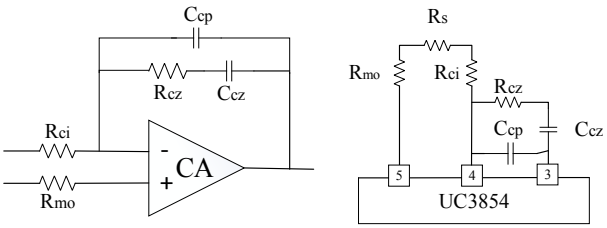

Fig.10 Current compensation circuit

Where R_s is the bus current sampling resister, R_{mo} and R_{ci} would help the current error amplifier compensation circuit to provide flat gain near the switching frequency. In the paper, R_s is connected in series in the bus in the sampling resistance, ΔV_s is the voltage fluctuation on R_s.

$$\Delta V_s = \frac{V_o R_s}{L f_s} \tag{17}$$

V_{pp} is the peak value, that is, the timing capacitor voltage (5.2V), so the current error amplifier gain is:

$$G_{ca} = \frac{V_{pp}}{\Delta V_s} \tag{18}$$

The feedback resistance is:

$$R_{cz} = G_{ca} R_{ci} \tag{19}$$

The current loop crossing frequency is:

$$f_{ca} = \frac{V_o R_s R_{cz}}{V_{pp} 2\pi L R_{ci}} \tag{20}$$

R_S is the bus current sampling resistance. ($V_S = 1V$)

$$R_S = \frac{V_S}{I_{peak} + \frac{\Delta I}{2}} \tag{21}$$

In the response of the current error amplifier, the position of the zero point should be located at or below the position of the crossing frequency point, then there is a large phase margin.

The zero compensation capacitor is:

$$C_{cz} = \frac{1}{2\pi f_{ca} R_{cz}} \tag{22}$$

Design the feedforward circuit as followed:

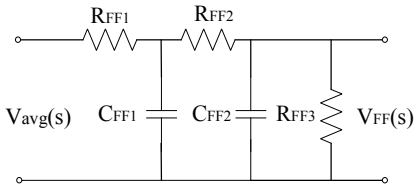

Fig.11 The feedforward circuit

Where $V_{avg}(s)$ is the rectifier voltage, $V_{FF}(s)$ is the feedforward voltage signal, and the voltage signal is added to the multiplier of the UC3854.

$$V_{avg}(s) = \frac{2\sqrt{2}}{\pi} V_{in(RMS)} \tag{23}$$

$$V_{FF} = \frac{R_{FF3}}{R_{FF1} + R_{FF2} + R_{FF3}} \times V_{avg}(s) \tag{24}$$

$$V_{C_{FF1}} = \frac{R_{FF2} + R_{FF3}}{R_{FF1} + R_{FF2} + R_{FF3}} \times V_{avg}(s) \tag{25}$$

The Second harmonic voltage attenuation gain:

$$G = \frac{1.5\%}{66\%}$$

$$C_{FF1} = \frac{1}{2\pi \times 2 \times f \times R_{FF2} \times \sqrt{G}} \tag{26}$$

$$C_{FF2} = \frac{1}{2\pi \times 2 \times f \times R_{FF3} \times \sqrt{G}} \tag{27}$$

B. *Experiments Results*

Based on the simulation analysis, we designed a single phase converter with Active Power factor Correction Module for driving asynchronous motor load. In order to verify the hardware design, we have done experiment in rated load conditions. Experimental results about the power factor and the dynamic performance highlight the effectiveness of the APFC module. Fig.12 shows that the real photo of a 3kW asynchronous motor drive control platform.

Fig.12 Real photo of an asynchronous motor drive control platform

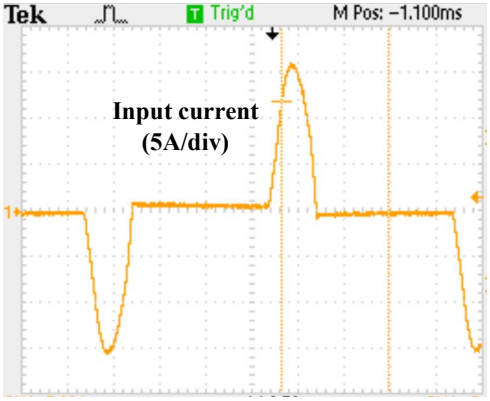

Fig.13 Conventional inverter input current waveform (3KW)

In Figure13, there is the input current waveform that is not controlled rectifier using a conventional inverter-driven induction motor at 3kW load. Compared with the fig5, it is the same that the input current has severe distortion, large harmonic components. We can do FFT analysis, and the THD was 140.21%. At this time, the power factor is 0.50;

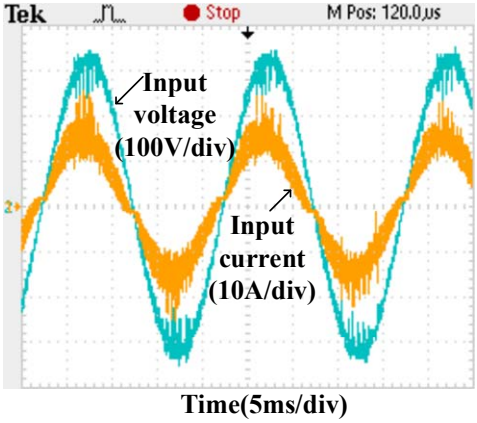

Fig.14 The input voltage and current at 3kW load

In Figure 14, there is the input voltage and current waveforms that the inverter with active power factor correction drive induction motor at 3kW load. We can see from the figure, the input current is in phase with the input voltage. At the same time, the input current is very sinusoidal. After analysis, THD is 30.66% and the power factor is 0.98 which meets the design requirements.

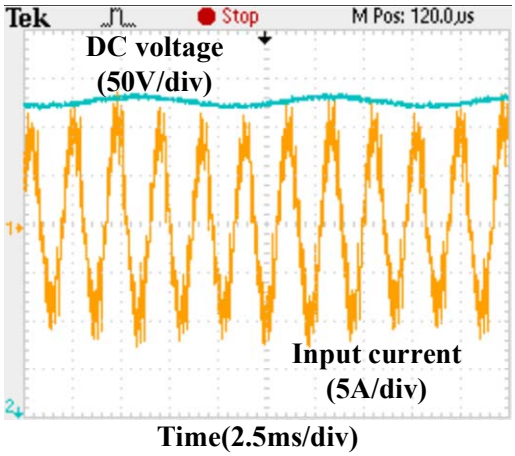

Fig.15 DC bus voltage and current waveform of the inverter with APFC module

In fig.15, there is DC bus voltage and current waveform of the inverter with APFC module. From the fig.15 can be seen that DC bus voltage is kept constant with APFC module, the motor current is no longer appear fluctuations.

V. CONCLUSIONS

In this paper, a high power factor single-phase inverter is designed and implemented. In rated load conditions, experimental results shows that we can gain a better DC bus voltage and a better power factor.

ACKNOWLEDGMENT

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