AN1059
APPLICATION NOTE

DESIGN EQUATIONS OF HIGH-POWER-FACTOR FLYBACK CONVERTERS BASED ON THE L6561

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Despite specific for Power Factor Correction circuits using boost topology, the L6561 can be successfully used to control flyback converters. Among the various configurations that an L6561-based flyback converter can assume, the high-PF one is particularly interesting because of both its peculiarity and the advantages it is able to offer. AC-DC adapters for mobile or office equipment, off-line battery chargers and low-power SMPS are the most noticeable examples of application that this configuration can fit.

This paper describes the equations governing such a kind of flyback converter with the aim of providing a number of relationships useful to the system designer.

INTRODUCTION

Three different configurations that an L6561-based flyback converter can assume have been identified. They are illustrated in fig. 1.

Configurations a) and b) are basically conventional flyback converters. The former works in TM (Transition Mode, i.e. on the boundary between continuous and discontinuous inductor current mode), therefore at a frequency depending on both input voltage and output current. The latter works at a fixed frequency, imposed by the synchronisation signal, and is therefore completely equivalent to a flyback converter based on a standard PWM controller.

Configuration c), which most exploits the aptitude of the L6561 for performing power factor correction, works in TM too but quite differently: the input capacitance is so small that the input voltage is very close to a rectified sinusoid. Besides, the control loop has a narrow bandwidth so as to be little sensitive to the twice mains frequency ripple appearing at the output.

Figure 1a. TM Flyback Configuration

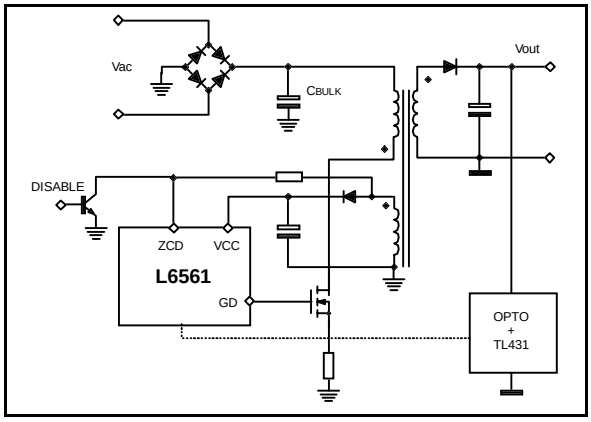


Figure 1b. Synchronised Flyback Configuration

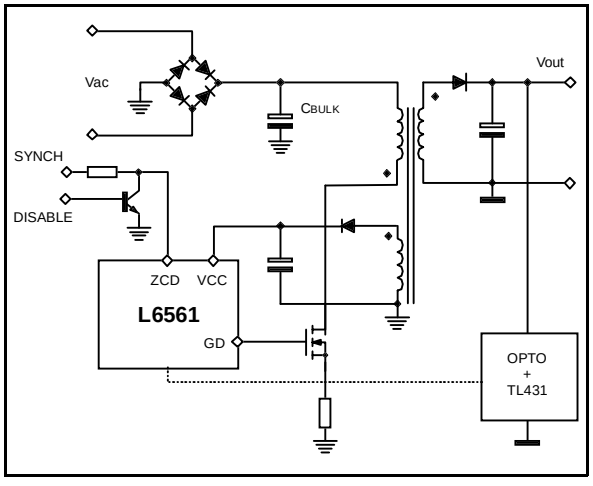
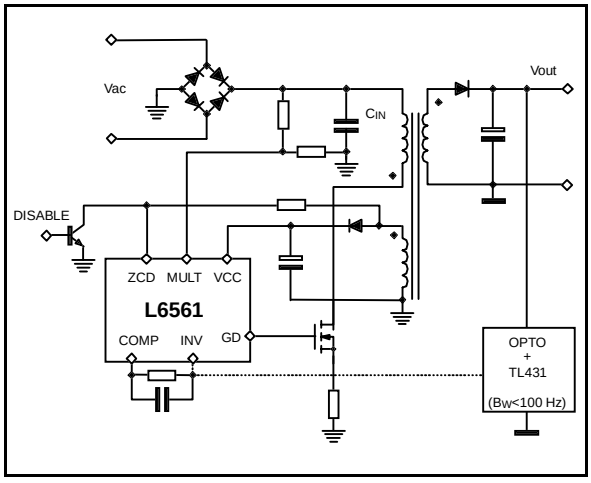


Figure 1c. High-PF Flyback Configuration



Actually, the high power factor (PF) exhibited by this topology can be considered just as an additional benefit but not the main reason that makes this solution attractive. In fact, despite a PF greater than 0.9 can be easily achieved, it is a real challenge to comply with EMC norms regarding the THD of line current, especially in universal mains applications.

There are, however, several applications in the low-power range (to which EMC norms do not apply) that can benefit from the advantages offered by a high-PF flyback converter. These advantages can be summarised as follows:

- for a given power rating, the input capacitance can be 200 times less, thus the bulky and costly high voltage electrolytic capacitor after the rectifier bridge will be replaced by a small-size, cheaper film capacitor.
- efficiency is high at heavy load, more than 90% is achievable: TM operation ensures low turn-on losses in the MOSFET and the high PF reduces dissipation in the rectifier bridge. This, in turn, minimises requirements on heatsinks;
- low parts count, which helps reduce encumbrance and assembly cost.

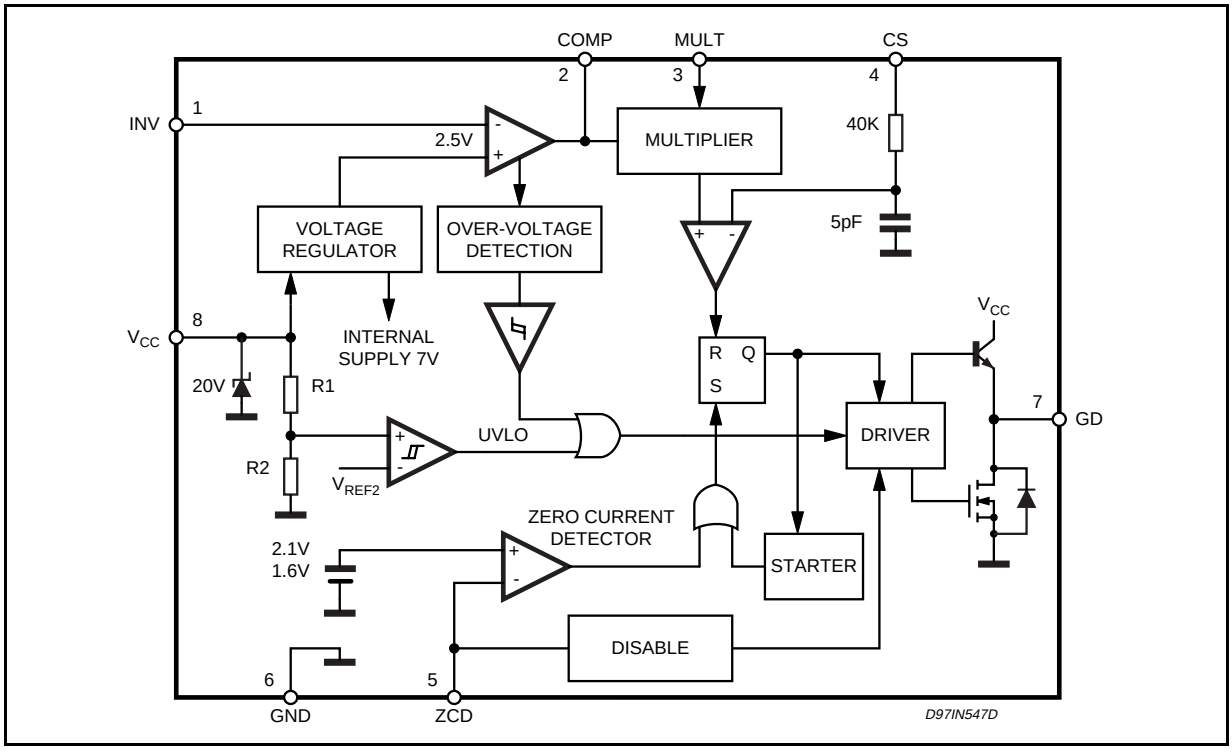
In addition, the unique features of the L6561 offer remarkable advantages in numerous applications:

- efficiency is high even at very light load: the low current consumption of the L6561 minimises the power dissipated by both the start-up resistor and the self-supply circuit. An L6561-based high-PF flyback converter can easily meet Blue Angel regulations;
- additional functions available: the L6561 provides overvoltage protection as well as the possibility to enable/disable the converter by means of its ZCD pin.

There are, on the other hand, some drawbacks, inherent in high-PF topologies, limiting the applications that such a converter can fit (AC-DC adaptors, battery chargers, low-power SMPS, etc.) and which one has to be aware of:

- twice-mains-frequency ripple on the output: unavoidable if a high PF is desired. A large output capacitance will reduce its amount. Speeding up the control loop may lead to a compromise between a reasonably low output ripple and a PF still reasonably high;
- poor transient response: as to this point too, speeding up the control loop may lead to a compromise between an acceptable transient response and a reasonably high PF;

Figure 2. Internal Block Diagram of the L6561.



- large output capacitance (in the thousand μF, depending on the output power) is required: however, cheap standard capacitors and not costly high-quality parts are needed. In fact, a low ESR and an adequate AC current capability are automatically achieved. Besides, in conventional flyback converters there is usually plenty of output capacitance too, thus this is not so dramatic as it may seem at first sight;
- secondary post-regulation will be required where tight specifications on the output ripple and/or on the transient behaviour are given. However, this is true also for a standard flyback;
- the system is unable to cope with line missing cycles at heavy load unless an exceedingly high output capacitance is used.

In the following, the operation of a high-PF flyback converter will be discussed in details and numerous relationships, useful for its design, will be established.

Preliminary statements

In order to generate the equations governing the operation of a high-PF flyback converter working in TM, refer also to the internal block diagram of the L6561(see fig. 2). For details concerning the operation of the L6561, please refer to Ref. [1].

The following assumptions will be made:

1. the line voltage is perfectly sinusoidal and the rectifier bridge is ideal, thus the voltage downstream the bridge, sensed by the input of the L6561's multiplier (MULT, pin 3) is a rectified sinusoid:

$$V_{in}(t) = V_{PK} \cdot |\sin(2 \cdot \pi \cdot f_L \cdot t)|$$

   where V_{PK} is equal to the RMS line voltage, V_{RMS}, times the square root of 2, and f_L is the line frequency (usually 50 or 60 Hz).
2. the output of L6561's Error Amplifier (V_{COMP}) is constant for a given line half-cycle;
3. transformer's efficiency is 1 and its windings are perfectly coupled.
4. ZCD circuit's delay is negligible thus the converter works exactly on the boundary between continuous and discontinuous current conduction mode (TM operation).

As a result of the first two assumptions, the peak primary current is enveloped by a rectified sinusoid:

$$I_{pkp}(t) = I_{PKp} \cdot |\sin(2 \cdot \pi \cdot f_L \cdot t)| \quad (1)$$

One consequence of assumption 3 is that the peak secondary current is proportional to the primary one, depending on transformer's primary-to-secondary turns ratio n:

$$I_{pks}(t) = n \cdot I_{pkp}(t)$$

To simplify the notation, in the following the phase angle $\theta = 2 \cdot \pi \cdot f_L \cdot t$ of the sinusoidal quantities will be indicated and all the quantities depending on the instantaneous line voltage will be considered as a function of θ, instead of time.

Timing relationships

The ON-time of the power switch is expressed by:

$$T_{ON} = \frac{L_p \cdot I_{pkp}(\theta)}{V_{in}(\theta)} = \frac{L_p \cdot I_{PKp}}{V_{PK}} \quad (2),$$

where L_p is the inductance of transformer's primary winding. Eqn. (2) shows that T_{ON} is constant over a line half-cycle, exactly like in boost topology. The OFF-time is instead variable:

$$T_{OFF} = \frac{L_s \cdot I_{pks}(\theta)}{(V_{out} + V_f)} = \frac{\frac{L_p}{n^2} \cdot n \cdot I_{pkp}(\theta)}{(V_{out} + V_f)} = \frac{L_p \cdot I_{PKp} \cdot |\sin(\theta)|}{n \cdot (V_{out} + V_f)} \quad (3),$$

where L_s is the inductance of the secondary winding, $I_{pks}(\theta)$ the peak secondary current, V_{out} the output voltage of the converter (supposed to be a regulated DC value) and V_f the forward drop on the output catch diode.

Since the system works in TM, the sum of the ON and the OFF times equals the switching period:

$$T = T_{ON} + T_{OFF} = \frac{L_p \cdot I_{PKp}}{V_{PK}} \cdot \left[1 + \frac{V_{PK}}{V_R} \cdot |\sin(\theta)|\right] \quad (4)$$

where $V_R = n \cdot (V_{out} + V_f)$ is the so-called reflected voltage.

The switching frequency $f_{sw} = T^{-1}$, therefore, varies with the instantaneous line voltage:

$$f_{sw} = \frac{V_{PK}}{L_p \cdot I_{PKp}} \cdot \frac{1}{1 + \frac{V_{PK}}{V_R} \cdot |\sin(\theta)|}$$

and reaches its minimum value on the peak of the sinusoid (sin (θ)=1):

$$f_{sw\,min} = \frac{V_{PK}}{L_p \cdot I_{PKp}} \cdot \frac{1}{1 + \frac{V_{PK}}{V_R}} \quad (5)$$

This value, calculated at the minimum line voltage, must be greater than the maximum one of the internal starter of the L6561 (≈14 kHz), in order to ensure a correct TM operation. To accomplish with this requirement, the primary inductance L_p will be properly selected (not exceeding an upper limit). Actually, to minimise the size of the transformer, the minimum frequency will usually be selected quite higher than 15 kHz, say 25-30 kHz or more, so the value of L_p needs not have a tight tolerance.

The duty cycle, that is the ratio between the ON-time and the switching period, will vary with the instantaneous line voltage as well (because of the variation of T_{OFF}), as it is possible to find by dividing eqn.(2) by (4):

$$D = \frac{T_{ON}}{T} = \frac{1}{1 + \frac{V_{PK}}{V_R} \cdot |\sin(\theta)|} \quad (5')$$

Equations (2) and (4) show that T_{ON} and T, respectively, can be short at will if I_{PKp} (i.e. the load) tends to zero, especially at high input voltage. In the real-world operation, it must be considered that T_{ON} cannot go below a minimum amount and so will do the switching period as well. This minimum (typically, 0.4-0.5µs) is imposed by the internal delay of the L6561 and by the turn-off delay of the MOSFET.
When this minimum is reached, the energy drawn each cycle exceeds the short-term demand from the load, thus the control loop causes some cycles to be skipped so as to maintain the long-term energy balance. When the load is so low that many cycles need to be skipped, the amplitude of the drain voltage ringing becomes so small that it can no longer trigger the ZCD Block of the L6561. In that case the internal starter of the IC will start a new switching cycles sequence.

Something similar applies to the duty cycle as well, which eqn. (5') predicts to be unity when θ = 0, that is at the zero-crossings of the mains voltage. In reality, a number of parasitic effects cause T_{ON} and T_{OFF} not to follow the ideal relationships (2) and (3). The effect of that on the overall operation is however negligible because the energy processed near a zero-crossing is very little.

In the following, the ratio between the line peak voltage V_{PK} and the reflected voltage V_R will be indicated with K_v:

$$K_v = \frac{V_{PK}}{V_R}$$

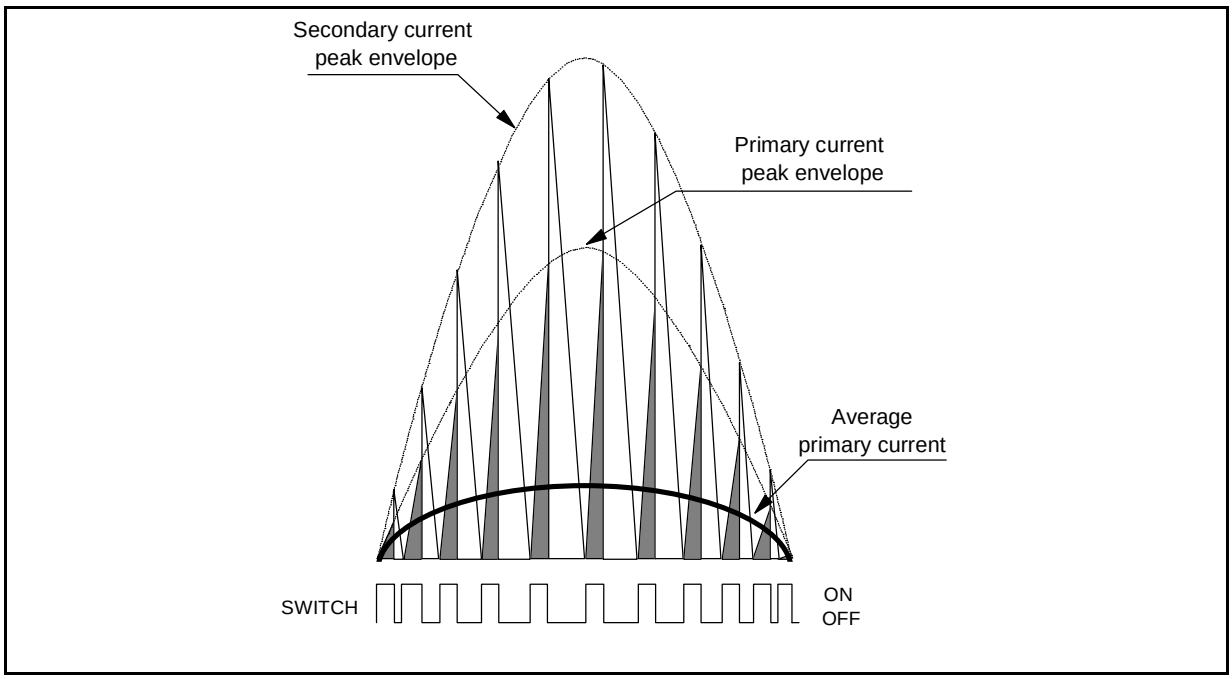
Energetic relationships

Apart from the duty cycle, all the quantities expressed in the timing relationships depend on the throughput power, which is represented in the above equations by I_{PKp}, the peak primary current occurring at

the peak of the sinusoid of the primary voltage.

The following relationships relate I_{PKp} to the input power P_{in} and allow both to explicate the timing relationships and to calculate all the currents circulating in the circuit.

Figure 3. High-PF Flyback current waveforms



The primary current $I_p(t)$ is triangular-shaped and flows only during the switch ON-time, as illustrated by the shaded triangles shown in fig. 3. As earlier stated by equation (1), during each half-cycle the height of these triangles varies with the instantaneous line voltage:

$$I_{pkp}(\theta) = I_{PKp} \cdot |\sin(\theta)|,$$

their width is constant but they are spaced out by a variable amount given by (3).

Looking at the primary on a "f_L" time scale, the current $I_{in}(\theta)$ downstream the bridge rectifier is the average value of each triangle over a switching cycle (the thick black curve of fig. 3):

$$I_{in}(\theta) = \frac{1}{2} \cdot I_{pkp}(\theta) \cdot D = \frac{1}{2} \cdot I_{PKp} \cdot \frac{|\sin(\theta)|}{1 + K_v \cdot |\sin(\theta)|}$$

Figure 4a. Primary Current (@ f_L time scale)

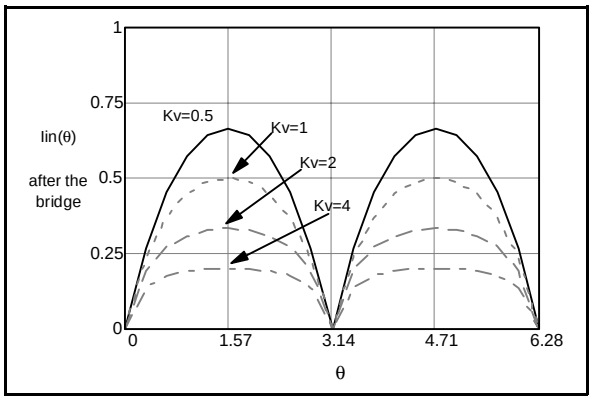
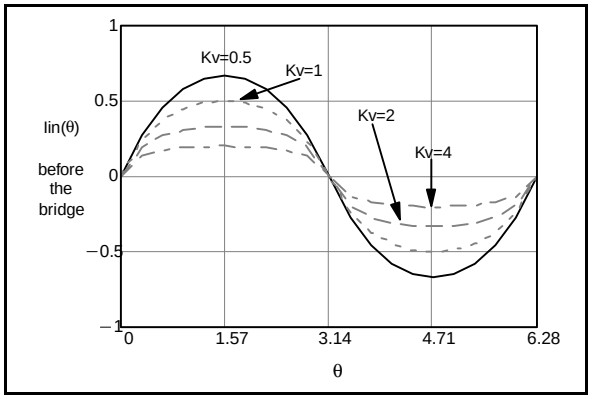


Figure 4b. Line Current (@ f_L time scale)



This function, shown in fig. 4a for different values of K_v, is a periodic even function, at twice line frequency, not negative because of the bridge rectifier. Conversely, the current drawn from the mains will be the "odd counterpart" of (6), at line frequency, as shown in fig. 4b).

Actually, it is realistic to think that a filtering action eliminates the switching frequency component of the current upstream the rectifier bridge, so that the mains "can see" only the average value. This current would be sinusoidal for $K_v = 0$ but will be distorted from an ideal sinusoid so much as K_v increases. Since K_v cannot be zero (which would require the reflected voltage to tend to infinity), flyback topology does not permit unity power factor even in the ideal case, unlike boost topology.

In order to simplify the following calculations, it is possible to eliminate the absolute value from $|\sin(\theta)|$ by considering $\theta \in [0, \pi]$ and assuming the various functions to be either even or odd by definition, depending on their physical role.

The input power P_{in} will be calculated by averaging the product $V_{in}(\theta) \bullet I_{in}(\theta)$ over a line half-cycle:

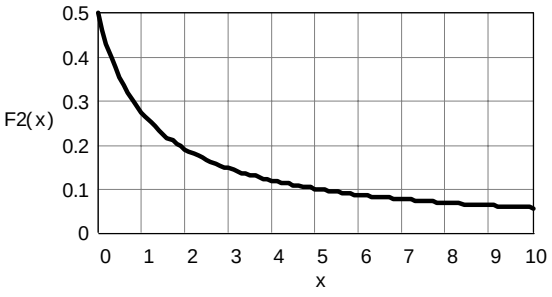
$$P_{in} = \overline{V_{in}(\theta) \cdot I_{in}(\theta)} = \frac{1}{2} \cdot V_{PK} \cdot I_{PKp} \cdot \overline{\frac{\sin^2(\theta)}{1 + K_v \cdot \sin(\theta)}} \qquad (7).$$

It is now advantageous to introduce the following function:

$$F2(x) = \overline{\frac{\sin^2(\theta)}{1 + x \cdot \sin(\theta)}} = \frac{1}{\pi} \cdot \int_0^{\pi} \frac{\sin^2(\theta)}{1 + x \cdot \sin(\theta)} d\theta \quad (8),$$

whose diagram as a function of the variable x is shown in fig. 5.

Figure 5. High-PF Flyback characteristic functions: F2(x) diagram



Although a closed form exists for the integral in (8), it is not so handy, thus for practical use it is more convenient to provide a "best fit" approximation:

$$F2(x) \approx \frac{0.5 + 1.4 \cdot 10^{-3} \cdot x}{1 + 0.815 \cdot x}.$$

From (7), taking (8) into account, it is possible to calculate I_{PKp}:

$$I_{PKp} = \frac{2 \cdot P_{in}}{V_{PK} \cdot F2(K_v)},$$

which will assume its maximum value at minimum mains voltage.

The total RMS value of the primary current, useful for power loss estimate on the primary side, is calculated considering the RMS value of each triangle of $I_p(t)$ and averaging over a line half-cycle:

$$I_{RMSp} = \sqrt{\frac{1}{3} \cdot \overline{I_{pkp}^2(\theta) \cdot D}} = I_{PKp} \cdot \sqrt{\frac{1}{3} \cdot \overline{\frac{\sin^2(\theta)}{1 + K_v \cdot \sin(\theta)}}} = I_{PKp} \cdot \sqrt{\frac{F2(K_v)}{3}} \qquad (9).$$

The DC component of the primary current, useful to discriminate DC and AC losses in the transformer, is the average value of $I_{in}(\theta)$ over a line half-cycle:

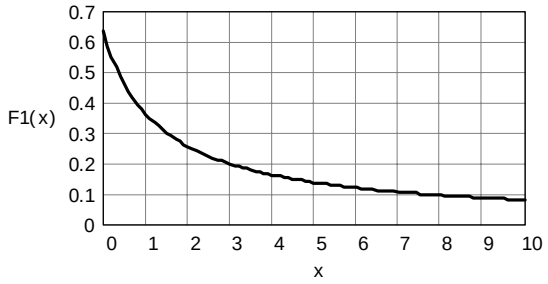
$$I_{DCp} = \overline{I_{in}(\theta)} = \frac{1}{2} \cdot I_{PKp} \cdot \overline{\frac{\sin(\theta)}{1 + K_v \cdot \sin(\theta)}} \qquad (10).$$

Considering the following function:

$$F1(x) = \overline{\frac{\sin(\theta)}{1 + x \cdot \sin(\theta)}} = \frac{1}{\pi} \cdot \int_0^{\pi} \frac{\sin(\theta)}{1 + x \cdot \sin(\theta)} d\theta,$$

equation (10) can be rewritten as follows:

Figure 6. High-PF Flyback characteristic functions: F1(x) diagram



$$I_{DCp} = \frac{1}{2} \cdot I_{PKp} \cdot F1(K_v).$$

Also for F1(x) it is more practical to furnish a best fit approximation rather than the exact expression:

$$F1(x) \approx \frac{0.637 + 4.6 \cdot 10^{-3} \cdot x}{1 + 0.729 \cdot x}.$$

As to the current on the secondary side, $I_s(t)$, it is the series of triangles complementary to the primary's (the white ones in fig. 3). Its twice line frequency representation will be again the average over a switching cycle:

$$I_o(\theta) = \frac{1}{2} \cdot I_{pks}(\theta) \cdot (1 - D) = \frac{1}{2} \cdot I_{PKs} \cdot K_v \cdot \frac{\sin^2(\theta)}{1 + K_v \cdot \sin(\theta)} \quad (11).$$

Like the primary current (6), also (11) is a not negative periodic even function.

According to assumption 3), I_{PKs} would equal $n \bullet I_{PKp}$. To consider a more realistic case (the secondary peak current is slightly less than $n \bullet I_{PKp}$ because of transformer's losses and other non-idealities) it is possible to derive I_{PKs} from the DC value of the output current, Iout, of the converter, which is one of the design data.

By equalling the average value of (11) over one line half-cycle to I_{out}, it is possible to find:

$$I_{PKs} = \frac{2 \cdot I_{out}}{K_v \cdot F2(K_v)}.$$

The total RMS secondary current is calculated as follows:

$$I_{RMSs} = \sqrt{\frac{1}{3} \cdot \overline{I_{pks}^2(\theta) \cdot (1 - D)}} = I_{PKs} \cdot \sqrt{\frac{K_v}{3} \cdot \overline{\frac{\sin^3(\theta)}{1 + K_v \cdot \sin(\theta)}}} \quad (12)$$

It will be now introduced the third characteristic function of the high-PF flyback:

$$F3(x) = \overline{\frac{\sin^3(\theta)}{1 + x \cdot \sin(\theta)}} = \frac{1}{\pi} \cdot \int_0^{\pi} \frac{\sin^3(\theta)}{1 + x \cdot \sin(\theta)} d\theta \approx \frac{0.424 + 5.7 \cdot 10^{-4} \cdot x}{1 + 0.862 \cdot x}.$$

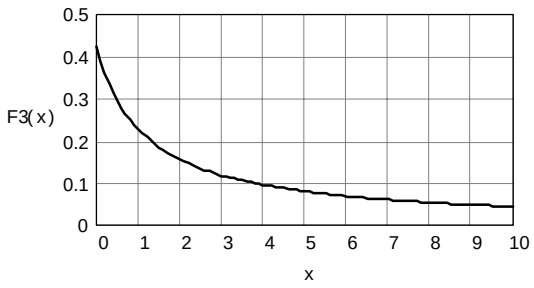
With this definition, it is possible to express (12) as follows:

$$I_{RMSs} = I_{PKs} \cdot \sqrt{K_v \cdot \frac{F3(K_v)}{3}}.$$

For both primary and secondary side, the AC component of current can be calculated with the general relationship:

$$I_{ACi} = \sqrt{I_{RMSi}^2 - I_{DCi}^2} \quad (i = p,s).$$

Figure 7. High-PF Flyback characteristic functions: F3(x) diagram



Power Factor and Total Harmonic Distortion

Under the assumption of a sinusoidal line voltage, the Power Factor PF can be expressed as:

$$PF = \frac{\text{Real Input Power}}{\text{Apparent Input Power}} = \frac{V_{RMS} \cdot I_{RMS1}}{V_{RMS} \cdot I_{RMSin}} = \frac{I_{RMS1}}{I_{RMSin}} \quad (13)$$

where V_{RMS} is the (effective) line voltage, I_{RMS1} is the effective value of the first harmonic (it will be in phase with the line voltage) and I_{RMSin} the total effective value of the input current waveform (6).

I_{RMS1} can be simply calculated from the numerator of (13):

$$I_{RMS1} = \frac{P_{in}}{V_{RMS}} = \sqrt{2} \cdot \frac{P_{in}}{V_{PK}} \quad (14).$$

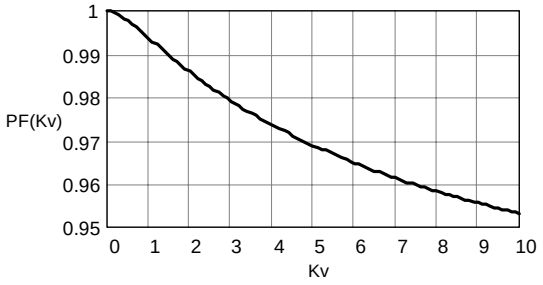
It is worth noticing that $I_{RMSin} \neq I_{RMSp}$. In fact (9) contains also the energy contribution due to the switching frequency, while equation (13) - and therefore I_{RMSin} too - refers only to line frequency quantities. I_{RMSin} is the RMS value of (6), which is by definition:

$$I_{RMSin} = \sqrt{\overline{I_{in}^2(\theta)}} = \frac{1}{2} \cdot I_{PKp} \cdot \sqrt{\frac{1}{\pi} \cdot \int_0^{\pi} \left[\frac{\sin(\theta)}{1 + K_v \cdot \sin(\theta)} \right]^2 d\theta} \quad (15).$$

Inserting (14) and (15) in (13) yields the theoretical expression of PF (note that it depends only on K_v). Its diagram, depicted in fig. 8, shows how it keeps quite close to 1. For practical use, PF can be approximated by:

$$PF(K_v) \approx 1 - 8.1 \cdot 10^{-3} \cdot K_v + 3.4 \cdot 10^{-4} \cdot K_v^2 \quad (16)$$

Figure 8. Theoretical Power Factor of high-PF Flyback converters



Obviously numerous non-idealities, basically the ones mentioned in the section "Timing Relationships", contribute to achieve a real-world PF lower than the theoretical value given by (16), especially at light load and high mains voltage.

The Total Harmonic Distortion (THD) of the line current is defined in percentage as:

$$THD\ \% = 100 \cdot \frac{\sqrt{\sum_2^{\infty} I_{RMSn}^2}}{I_{RMS1}},$$

where I_{RMSn} is the RMS amplitude of the n-th harmonic. Still under the assumption of an ideally sinusoidal input voltage, the THD is related to the Power Factor by the following relationship:

$$THD\% = 100 \cdot \sqrt{\frac{1}{PF^2} - 1}.$$

Figure 9. THD% as a function of Kv

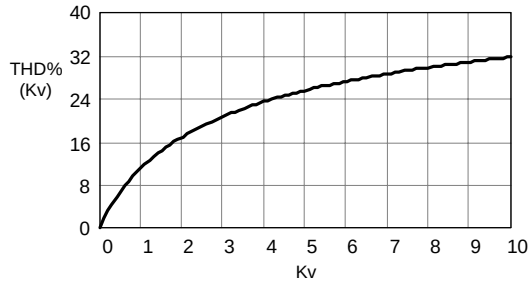


Fig. 9 illustrates the dependence of THD% on Kv. For a given reflected voltage, it shows how the Total Harmonic Distortion degrades when the line voltage builds up.

Transformer

The design of the transformer is a complex procedure that involves several steps: selecting the core material and geometry, determining the maximum peak magnetic flux density (and whether this is lim-

ited by core saturation or losses), determining the core size, defining the primary and secondary windings (turns number and wire gauge) as well as calculating the air-gap necessary to achieve the desired inductance. Moreover, additional considerations concerning the assembly are needed for meeting safety requirements, maximising magnetic coupling and minimising parasitic high frequency effects, not to mention the constraints imposed by the specific application, if any.

Some parameters are needed to start the design of the transformer. The (maximum) primary inductance will be calculated by solving (5) for L_p:

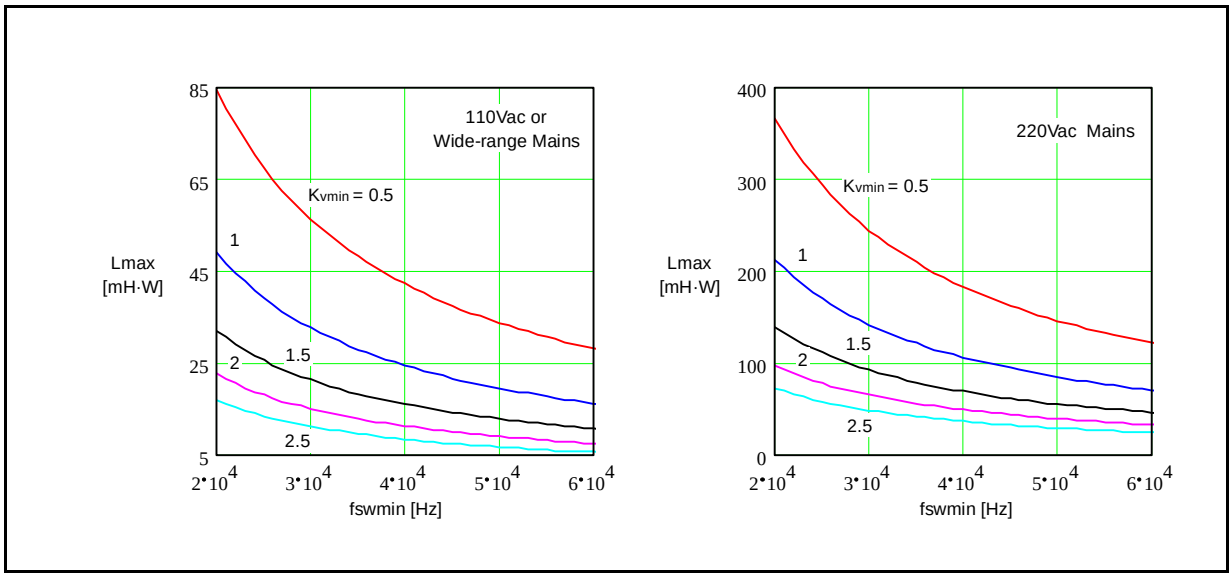
$$L_p \le \frac{1}{2} \cdot \frac{F2(K_{vmin})}{1 + K_{vmin}} \cdot \frac{V_{PKmin}^2}{f_{swmin} \cdot P_{inmax}},$$

or by simply looking up the diagram of fig. 10, where the primary inductance required for 1W input power is plotted against f_{swmin}, for different values of K_{vmin} and for the two typical mains voltage ranges. The value taken from fig. 10 (in mH), will be divided by the maximum input power to get the actual primary inductance required by the specific application.

The primary-to-secondary turns ratio will be given by:

$$n = \frac{V_R}{V_{out} + V_f}$$

Figure 10. Maximum specific primary inductance required



With the peak and RMS current values calculated in the "Energetic relationships" section, the design can be carried out just like for any conventional flyback transformer, thus no particular procedure will be considered.

Anyway, as a design aid to core selection, two expressions for determining the minimum required core Area-Product (winding window area times effective magnetic cross section) will be provided:

$$AP_{min} = \left[\frac{460 \cdot P_{in}}{f_{swmin} \cdot (1 + K_v) \cdot \sqrt{F2(K_v)}} \right]^{1.316} \quad (17);$$

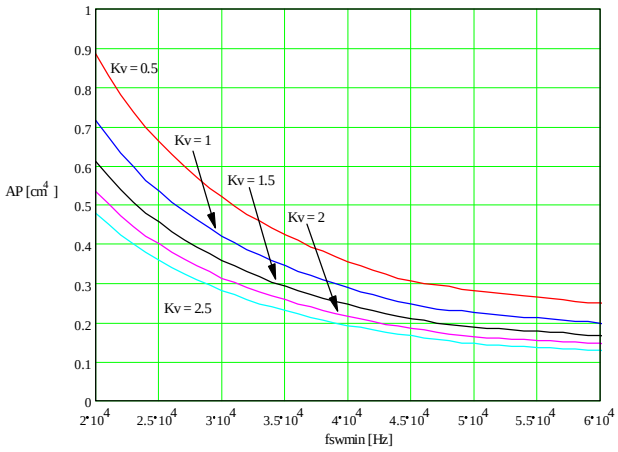
$$AP_{min} = \left[\frac{480 \cdot P_{in}}{f_{swmin} \cdot (1 + K_v) \cdot \sqrt{F2(K_v)}} \right]^{1.585} \cdot [\, J_H(K_v) \cdot f_{swmin} + J_E(K_v) \cdot f_{swmin}^2 \,]^{0.66} \quad (18);$$

where J_H (Kv) and J_E (Kv) are functions related to hysteresis and eddy current losses, whose best fit approximation are respectively:

$$J_H(K_v) \approx \frac{1.87 + 1.26 \cdot K_v}{1 + 0.55 \cdot K_v} \cdot 10^{-5} \quad J_E(K_v) \approx \frac{1.88 + 1.06 \cdot K_v}{1 + 0.34 \cdot K_v} \cdot 10^{-10}.$$

Formula (17) assumes that the maximum peak flux density inside the core is limited by core saturation and that all transformer losses are located in the windings; (18) assumes that core losses limit the flux swing and the total dissipation are half due to core losses and half to windings losses.

Figure 11. Minimum Transformer AP required for a 30W application.



Common to both formulae are the following assumptions:

1. the material is a typical power ferrite (3C85 from Philips, N67 from Siemens or similar grades) with a saturation flux density above 0.3 Tesla;

2. the windings occupy 40% of the total window area to leave space for isolation layers, creepage and clearance distances;

3. primary and secondary winding wires are proportioned for equal RMS current density;

4. core and/or copper losses result in 30 °C hot spot temperature rise (no forced cooling);

5. skin and proximity effects are neglected, considering the frequency range involved.

For a given f_{swmin}, one should try both formulae (considering K_v at minimum line voltage) and use the higher resulting value. Core losses become dominant for core selection above 45 kHz at this power level.

In fig. 11, the higher value resulting from (17) and (18) is plotted against f_{swmin} for different values of K_v, considering 30W output power with an estimate of 85% efficiency.

Clamp network

The overvoltage spikes due to the leakage inductance of the transformer are usually limited by an RCD clamp network, as illustrated in fig. 12a. It can be advantageous the use of a zener (or transil) clamp (see fig. 12b) when minimisation of power losses at light load is desired.

Considering the RCD clamp, the capacitor is selected so as to have an assigned overvoltage ΔV (as a rule of thumb, half the reflected voltage) at turn-off such that the voltage rating of the MOSFET is never exceeded. From energetic balance, it is possible to write:

$$C_{min} = \frac{L_{lk} \cdot I^2_{PKpmax}}{\Delta V \cdot (\Delta V + 2 \cdot V_R)},$$

where L_{lk} is the leakage inductance, which can be estimated in the range of 1 to 3% of the primary inductance if the transformer is properly manufactured, and:

$$I_{PKpmax} = \frac{2 \cdot P_{inmax}}{V_{PKmin} \cdot F2(K_{vmin})}$$

The capacitor undergoes large current spikes and therefore it should be a very low ESR type with polypropylene or polystyrene film dielectric.

Figure 12a. RCD Clamp.

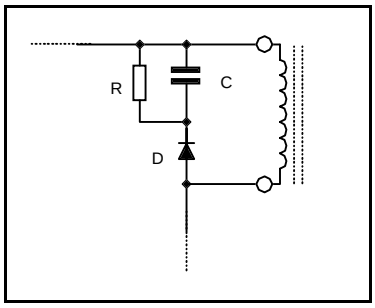
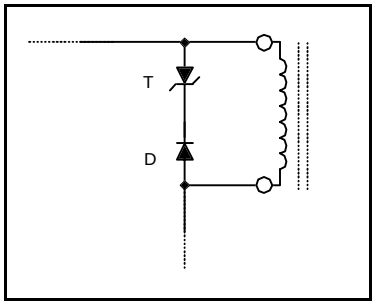


Figure 12b. Zener (Transil) Clamp.



The minimum resistor value can be found by imposing that the voltage on the capacitor at the beginning of each switching cycle never falls below the reflected voltage :

$$R_{min} = \frac{1}{f_{swmin} \cdot C \cdot \ln\left(1 + \frac{\Delta V}{V_R}\right)}$$

The power rating of this resistor can be estimated by considering the DC dissipation due to the reflected voltage and the leakage inductance energy:

$$P_R = \frac{V_R^2}{R} + \frac{1}{2} \cdot (1 + K_{vmin}) \cdot F2(K_{vmin}) \cdot L_{lk} \cdot I_{PKpmax}^2 \cdot f_{swmin}.$$

The blocking diode will be not only a very fast recovery type but will also feature a very fast turn-on time. In fact, the instantaneous forward drop at turn-on generates a spike, exceeding the overvoltage ΔV, that must be small. The diode will be rated for repetitive peak currents equal to I_{PKp}, and with a breakdown voltage greater than $V_{PKmax} + V_R$.

Considering a zener or a transil, its clamping voltage can be approximated with its breakdown voltage. In fact, the peak current is quite small and it is possible to neglect the contribution due to the dynamic resistance. The breakdown voltage, which should account for the drift due to the temperature rise, will then be:

$$V_{(BR)} \approx V_{CL} = V_R + \Delta V.$$

The steady-state power dissipation capability must be at least:

$$P_{transil} = \frac{V_{(BR)}}{2 \cdot (V_{(BR)} - V_R)} \cdot (1 + K_{vmin}) \cdot F2(K_{vmin}) \cdot L_{lk} \cdot I_{PKpmax}^2 \cdot f_{swmin},$$

while there is no concern about its peak power dissipation, since this is defined for power pulses of 1 ms (leakage inductance is typically demagnetized in less than 1 µs).

As to the blocking diode, what said earlier about the one of the RCD clamp still applies.

Output Capacitor

The output capacitor undergoes the AC component of the secondary current $I_s(t)$, (see fig 3).

Besides, to achieve a reasonably high PF, the voltage control loop is slow (typically, its bandwidth is below 100 Hz). As a result, there is a quite large voltage ripple appearing across the output capacitor. This ripple has two components.

One is related to the high frequency triangles and depends almost entirely on the ESR of the output capacitor, being the capacitive contribution practically negligible. Its maximum amplitude, occurring on the peak of the sinusoid, will be:

$$\Delta V_0^{(HF)} = I_{PKs} \cdot ESR.$$

The second component of the ripple is related to the twice line frequency envelope and, unlike the high frequency component, depends on the capacitance value, while the ESR contribution can be neglected.

To calculate the amplitude of this component, only the fundamental harmonic of (11), at twice line frequency, will be taken into account. In fact, the amplitude of the higher order (even) harmonics is much smaller and the impedance of the capacitor decreases with frequency as well.

According to Fourier's analysis, the (peak) amplitude of the fundamental harmonic of (11) is:

$$I_{o2} = \frac{I_{PKs} \cdot K_v}{\pi} \cdot \int_0^{\pi} \frac{\sin^2(\theta) \cdot \cos(2 \cdot \theta)}{1 + K_v \cdot \sin(\theta)} d\theta,$$

that, defining the following function:

$$H2(x) = \frac{1}{\pi} \cdot \left| \int_0^{\pi} \frac{\sin^2(\theta) \cdot \cos(2 \cdot \theta)}{1 + x \cdot \sin(\theta)} \right| d\theta \approx \frac{0.25 - 1.5 \cdot 10^{-3} \cdot x}{1 + 1.074 \cdot x} \qquad (19),$$

can be expressed as:

$$I_{o2} = I_{PKs} \cdot K_v \cdot H2(K_v) = 2 \cdot I_{out} \cdot \frac{H2(K_v)}{F2(K_v)}.$$

The absolute value in (19) is needed since the integral results negative, because the harmonic is 180° out of phase. Finally, the peak-to-peak amplitude of the low frequency output ripple is:

$$\Delta V_o = 2 \cdot I_{o2} \cdot Z^{(2fL)}(C_o) = \frac{1}{\pi} \cdot \frac{H2(K_v)}{F2(K_v)} \cdot \frac{I_{out}}{f_L \cdot C_o}.$$

In most cases, once a capacitor is selected so as to meet the requirement on the low frequency ripple, the ESR will be low enough to make the high frequency ripple negligible.

Multiplier Bias and Sense Resistor Selection

A resistor divider feeds a portion of the input voltage into pin 3 (MULT) to build the sinusoidal reference for the peak primary current. To set properly the operating point of the multiplier the following procedure is recommended.

First, the maximum peak value for V_{MULT}, $V_{MULTpkmax}$, is selected. This value, which will occur at maximum mains voltage, should be 2.5 to 3V in wide range mains applications and 1 to 1.5V in case of single mains. The minimum peak value, occurring at minimum mains voltage will be:

$$V_{MULTpkmin} = V_{MULTpkmax} \cdot \frac{V_{PKmin}}{V_{PKmax}}$$

This value, multiplied by the minimum guaranteed $\Delta V_{CS}/\Delta V_{COMP}$ will give the maximum peak output voltage of the multiplier:

$$V_{cxpk} = 1.65 \cdot V_{MULTpkmin}$$

If the resulting V_{cxpk} exceeds the linearity limit of the current sense (1.6 V), the calculation should be repeated beginning with a lower $V_{multpkmax}$ value.

In this way, the divider ratio will be:

$$K_P = \frac{V_{MULTpkmax}}{V_{PKmax}}$$

and the individual resistor values can be chosen by setting the current through them, in the hundreds μA or less, to minimise power dissipation.

The value of the sense resistor, connected between the source of the MOSFET and ground, across which the L6561 reads the primary current, is calculated as follows:

$$R_s \leq \frac{V_{cxpk}}{I_{PKpmax}}.$$

The resistor will be rated for a power dissipation equal to:

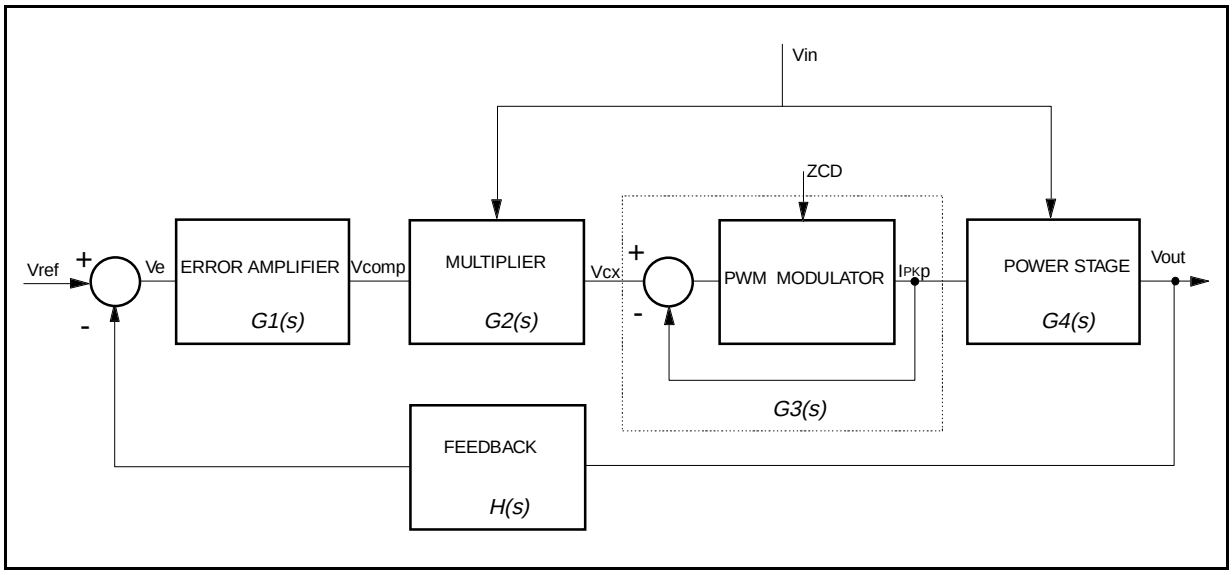
$$P_s = R_s \cdot I_{PKpmax}^2 \cdot \frac{F2(K_{vmin})}{3}$$

Closing the Control Loop

The control loop of a high-PF flyback converter based on the L6561, can be synthesised as in the block diagram of fig. 13.

Unlike conventional converters, in such regulators the control loop will have quite a narrow bandwidth so as to maintain V_{COMP} fairly constant over a given line cycle, as assumed at the beginning. This will ensure a high PF. On the other hand, it is not possible to achieve a very high PF (>0.99), thus it makes no sense to have a very narrow bandwidth (<20 Hz) like in boost PFC preregulators. This would degrade the transient response to line and load changes without any benefit. A compromise will then be found between these two contrasting terms.

Figure 13. Block Diagram of the Control Loop of an L6561 - based high-PF flyback.

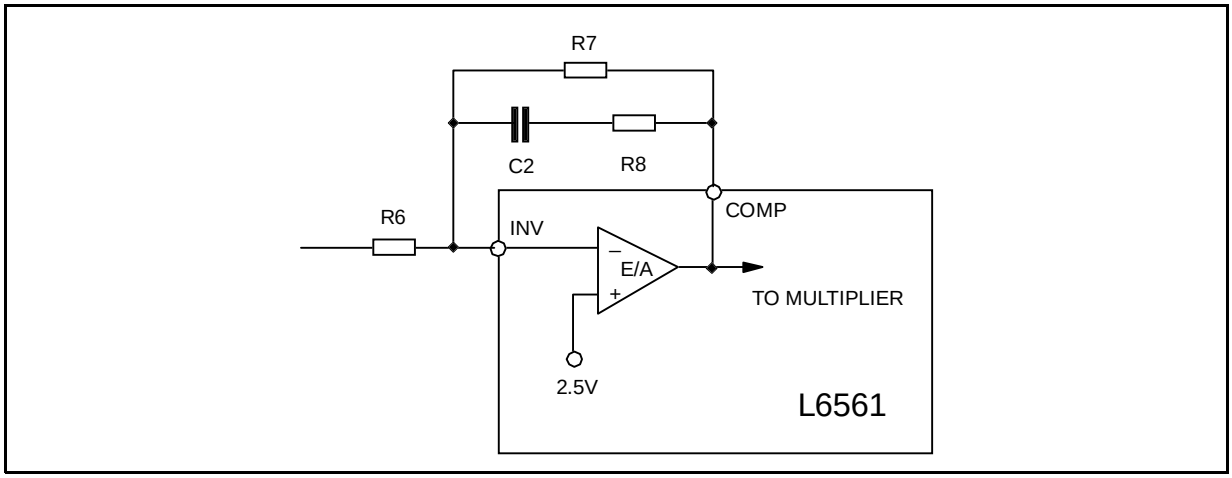


To the aim of deriving the transfer functions of the blocks in fig. 13, the narrow bandwidth of the control loop allows to assume that the control action takes place on the peak amplitude of the various quantities.

The error amplifier (E/A) of the L6561 is compensated as illustrated in fig. 14. The transfer function G1(s) will be then:

$$G1(s) = \frac{\Delta V_{COMP}}{\Delta V_E} = -\frac{R_7}{R_6} \cdot \frac{1 + s \cdot (C_2 \cdot R_8)}{1 + s \cdot [C_2 \cdot (R_7 + R_8)]}.$$

Figure 14. Compensation of the Error Amplifier.



The pole is placed at a very low frequency so that the gain at twice line frequency is quite less than unity, while the zero boosts the phase in the neighbourhood of the open-loop crossover frequency so as to provide phase margin.

A variation ΔV_{COMP}, due to a line and/or load change, modifies the amplitude V_{cx} of the rectified sinusoid at the output of the multiplier. This considering, the transfer function of the multiplier block will be:

$$G2 = \frac{\Delta V_{cx}}{\Delta V_{COMP}} = K_M \cdot K_P \cdot V_{PK}$$

where K_M is the gain of the multiplier (= 0.75 max.).

The gain of the PWM modulator, which includes the current loop, is simply:

$$G3 = \frac{\Delta I_{PKp}}{\Delta V_{cx}} = \frac{1}{R_s}$$

where R_s is the sense resistor.

Small-Signal analysis shows that the gain G4(s) of the power stage is:

$$G4(s) = \frac{\Delta V_{out}}{\Delta I_{PKp}} = \frac{n \cdot K_v \cdot F2(K_v)}{\Gamma(K_v) + 1} \cdot \frac{R_o}{2} \cdot \frac{1 + s \cdot (C_o \cdot ESR)}{1 + s \cdot (C_o \cdot \frac{R_o}{\Gamma(K_v) + 1})},$$

where the function $\Gamma(x)$ is defined as follows:

$$\Gamma(x) = 1 + \frac{x}{F2(x)} \cdot \frac{dF2(x)}{dx} \approx \frac{1 + 0.01 \cdot x}{1 + 0.8 \cdot x}.$$

The feedback network can have different configurations, depending on the requirements on the tolerance and on the regulation of the output voltage.

In this context a popular configuration (see fig. 15) will be taken into consideration. It uses an optocoupler for galvanic isolation between primary and secondary and a TL431, a cheap voltage reference/op-amp housed in a three pin package.

The gain, H(s), at twice line frequency must be low. In fact, being the output voltage ripple quite high, a high gain could saturate the dynamics of the TL431 and/or of the optocoupler, besides complicating things in getting a narrow overall bandwidth.

Referring to fig. 15, it is possible to write:

$$H(s) = \frac{\Delta V_E}{\Delta V_{out}} = \frac{1}{R_4} \cdot \frac{R_5 \cdot R_6}{R_5 + R_6} \cdot CTR \cdot \frac{1 + s \cdot C_1 \cdot (R_1 + R_3)}{s \cdot (C_1 \cdot R_1)},$$

where CTR is the Current Transfer Ratio of the optocoupler.

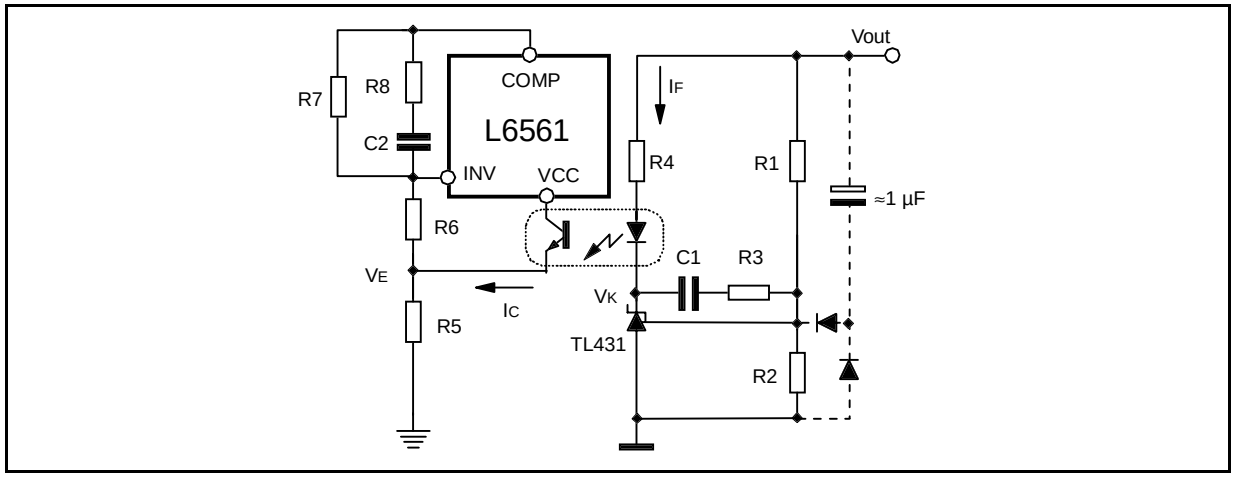
When designing the control loop, first select the operating current of optocoupler's transistor (I_C). It is advantageous to selects a low I_C value (e.g. 1 mA): this will not only extend the lifetime of the device but, in the present case, will also help keep low the gain of the feedback network at twice line frequency.

Since in closed-loop operation the quiescent value of V_E will be in the neighbourhood of 2.5V (internal reference of the L6561 E/A), R_5 will be:

$$R_5 = \frac{2.5}{I_C}.$$

R_4 will be selected so as to maintain V_K voltage above 2.5V for a correct functionality of the TL431 even in the worst case, that is when the optocoupler exhibits its minimum CTR, because of the statistical spread of this parameter.

Figure 15. Feedback network and connection to the error amplifier.



Therefore:

$$R_4 < \frac{V_{out} - 1 - 2.5}{2.5} \cdot CTR_{min} \cdot R_5,$$

where 1V is the typical drop across optocoupler's photodiode. Keep R_4 close to the maximum for a low gain. R_1 and R_2 are selected to get the desired output voltage:

$$R_2 = \frac{2.5}{I_{R2}}; \; R_1 = \frac{V_{out} - 2.5}{2.5} \cdot R_2$$

where 2.5 is the internal reference of the TL431 and I_{R2} the current flowing through R_2.

To have a low gain at twice line frequency, the zero of H(s) will be placed below 100Hz and R_3 will be 4-5 times less than R_1. This yields the value of C_1.

The value of R_6 will be such that the twice mains frequency ripple superimposed on the static V_E cannot trip the dynamic overvoltage protection of the L6561 (40 µA entering pin COMP). Approximately:

$$R_6 > R_5 + \frac{R_5}{R_4} \cdot \frac{CTR_{max} \cdot \Delta V_o}{40 \cdot 10^{-6}}$$

R_7 will be selected so as to allow the output of the error amplifier to swing all the dynamics. Finally, R_8 and C_2 will be adjusted so that the crossover frequency of the open-loop gain is a good compromise between a high enough PF and an acceptable transient response, ensuring also sufficient phase margin.

The optional capacitor (in the µF range) connected in parallel to R_1 acts as a soft-start circuit that prevents overvoltages of the output at start-up, especially at light load. The two diodes decouple the capacitor during steady-state operation so that it does not interfere with the loop gain and provide a discharge path when the converter is turned off.

CALCULATION EXAMPLE

An example of step-by-step design procedure of an L6561-based, high-PF flyback converter will be here described for reference. It concerns a 30W AC adapter for portable equipment. The application was actually realised and some experimental results are here presented.

1. Design Specifications:

- Mains voltage range: V_{ACmin} = 88 Vac, V_{ACmax} = 264 Vac
- Minimum mains frequency: f_L = 50 Hz
- DC Output Voltage: V_{out} = 15 V
- Maximum output current: I_{out} = 2A
- Maximum $2f_L$ output ripple: ΔV_o = 1V peak-to-peak

2. Pre-design Choices:

- Minimum switching frequency: f_{swmin} = 25 kHz
- Reflected voltage: V_R = 100V
- Leakage inductance overvoltage: ΔV =70V
- Expected efficiency: η = 85%

3. Preliminary Calculations:

- Minimum Input Peak Voltage: $V_{PKmin} = V_{ACmin} \cdot \sqrt{2} = 88 \cdot \sqrt{2} - 4 = 120V$
  (4V total drop on $R_{DS(on)}$, Rs, ...)
- Maximum Input Peak Voltage: $V_{PKmin} = V_{ACmin} \cdot \sqrt{2} = 264 \cdot \sqrt{2} = 373V$
- Maximum Output Power: $P_{out} = V_{out} \cdot I_{out} = 15 \cdot 2 = 30W$
- Maximum Input Power: $P_{in} = \frac{P_{out}}{\eta} \cdot 100 = \frac{30}{85} \cdot 100 = 35.3W$
- Peak-to-reflected Voltage Ratio: $K_v = \frac{V_{PKmin}}{V_R} = \frac{120}{100} = 1.2$
- Characteristic functions value: F1(1.2)=0.343; F2(1.2)=0.254; F3(1.2)=0.209; F5(1.2)=0.108

4. Operating Conditions:

- Peak Primary Current: $I_{PKp} = \frac{2 \cdot P_{in}}{V_{PKmin} \cdot F2(K_v)} = \frac{2 \cdot 35.3}{120 \cdot 0.254} = 2.32A$
- RMS Primary Current: $I_{RMSp} = I_{PKp} \cdot \sqrt{\frac{F2(K_v)}{3}} = 2.32 \cdot \sqrt{\frac{0.254}{3}} = 0.675A$
- Peak Secondary current: $I_{PKs} = \frac{2 \cdot I_{out}}{K_v \cdot F2(K_v)} = \frac{2 \cdot 2}{1.2 \cdot 0.254} = 13.1A$
- RMS Secondary Current: $I_{RMSs} = I_{PKs} \cdot \sqrt{K_v \cdot \frac{F3(K_v)}{3}} = 13.1 \cdot \sqrt{1.2 \cdot \frac{0.209}{3}} = 3.79A$

5. Transformer:

- Primary inductance: $L_p = \frac{V_{PKmin}}{(1 + K_v) \cdot f_{swmin} \cdot I_{PKp}} = \frac{120}{(1 + 1.2) \cdot 25 \cdot 10^3 \cdot 2.32} = 940\mu H$
- Primary-to-secondary turns ratio: $n = \frac{V_R}{(V_{out} + V_f)} = \frac{100}{15 + 0.6} = 6.41$

From diagram of fig. 11, by interpolation, the minimum AP required is about 0.5 cm^4. An ETD29 core (AP = 0.684 cm^4), 3C85 grade is selected. From the relevant datasheet, with 1

mm air gap 90 primary turns will result in about 970µH primary inductance. 14 secondary turns give a 6.43 turns ratio, very close to the target. Estimating the thermal resistance of the ETD29 equal to 26°C/W, the maximum power dissipation (supposed to be on copper only) for 30°C hot-spot temperature rise will be 1.15W (half will be allocated to the primary and half to the secondary). This requires the resistance of the primary to be no more than 1.26 Ω and the secondary's no more than 40 mΩ. An AWG27 (∅ ≈ 0.4 mm) wire for the primary and a strand of 5xAWG27 for the secondary will meet the requirement.The primary winding will be split in two halves of 45 turns each, series connected, and the secondary will be sandwiched in between to reduce leakage inductance.

6. MOSFET selection

- Maximum Drain Voltage:$V_{DSmax} = V_{PKmax} + V_R + \Delta V = 373 + 100 + 70 = 543V$

There is margin to select a 600 V device. This will minimise gate drive and capacitive losses. Assuming that the MOSFET will dissipate 5% of the input power, that losses are due to conduction only, and that $R_{DS(on)}$ doubles at working temperature, the $R_{DS(on)}$ at 25°C should be about 2Ω. An STP4NA60 ($R_{DS(on)}$ = 2.2 Ω max.) is selected.

7. Catch diode selection

- Maximum reverse voltage: $V_{REVmax} = \frac{V_{PKmax}}{n} + V_{out} = \frac{373}{6.41} + 15 = 73.2V$

A 100V Schottky diode will minimise conduction losses. As to its current rating, a tentative value can be 40% of the peak current: $I_F = 0.4 \cdot I_{PKs} = 0.4 \cdot 13.1 = 5.2A$. A suitable device could be the STPS8H100D. From the relevant datasheet, the power dissipation is estimated as: $P_{diode} = 0.48 \cdot I_{out} + 0.013 \cdot I^2_{RMSs} = 0.55 \cdot 2 + 0.013 \cdot 3.79^2 = 1.15W$, which is acceptable.

8. Output Capacitor Selection

The minimum capacitance value that meets the specification on the 100/120 Hz ripple is:

$$C_{outmin} = \frac{1}{\pi \cdot f_L} \cdot \frac{H2(K_v)}{F2(k_v)} \cdot \frac{I_{out}}{\Delta V_o} = \frac{0.108 \cdot 2}{3.14 \cdot 50 \cdot 0.254 \cdot 1} = 5417\mu F$$

Three 2200µF electrolytic capacitors will have an ESR low enough to consider the high frequency ripple negligible as well as sufficient AC current capability.

9. Clamp network

With a proper construction technique, the leakage inductance can be reduced to as much as 2% of the primary inductance, that is 20µH in the present case. A transil clamp is selected. The clamp voltage will be $V_{CL} = V_R + \Delta V = 100 + 70 = 170V$. The steady-state power dissipation is estimated to be about 2W. A P6KE170A transil is selected. The blocking diode is an STTA106.

10. Multiplier bias and sense resistor selection

Assuming a peak value of 2.4V (@V_{AC} = 264V) on the multiplier input (MULT, pin 3), the peak value at minimum line voltage will be $V_{MULTpkmin} = 2.4 \cdot 88/264 = 0.8V$ which, multiplied by the maximum slope of the multiplier, 1.65, gives 1.32V peak voltage on current sense (CS, pin 4). Since the linearity limit (1.6V) is not exceeded, this is acceptable. The divider ratio will then be $2.4/(\sqrt{2} \cdot 264) = 6.43 \cdot 10^{-3}$. Considering 120µA current for the divider, the lower resistor will be 20kΩ, and the upper one 3MΩ.The sense resistor will not exceed 1.32/2.32 = 0.57Ω (0.5Ω is selected), while its power rating will be $0.5 \cdot I^2_{RMSp} = 0.5 \cdot 0.675^2 = 228mW$

11. Feedback and Control Loop

The selected optocoupler is a 4N35 from Toshiba. 1 mA quiescent collector current is selected. From opto's datasheet, with 1mA collector current, the diode current can be between 1 and 2 mA approximately (0.5 < CTR < 1).

An emitter resistor of 2.4kΩ, will give the desired collector current, thus the bias resistor should satisfy the inequality $R_4 < \frac{15 - 1.2 - 2.5}{2.5} \cdot 0.5 \cdot 2.4 = 5.4k\Omega$.

Select R_4 = 5.1kΩ. As to the output divider, with R_2 = 2.4kΩ, the upper resistor will be R_1 = 12kΩ. Select R_3 = 2.2 kΩ. With C_1 = 1µF the zero will be at about 70 Hz, which is acceptable. R_6 should be so that $R_6 > 2.4 \cdot 10^3 + \frac{2.4}{5.1} \cdot \frac{1 \cdot 1}{40 \cdot 10^{-6}} = 14k\Omega$. Select R_6 = 20 kΩ. By selecting R_7 = 39 kΩ, R_7 = 9.1 kΩ and C_2 = 220 nF, the open-loop crossover frequency and phase margin will be 50 Hz and 42° respectively.

The complete electrical schematic of this application is illustrated in fig.16, fig. 17 presents some results of its bench evaluation and fig. 18 shows some significant waveforms.

Figure 16. 30W High-PF Flyback with the L6561: electrical schematic

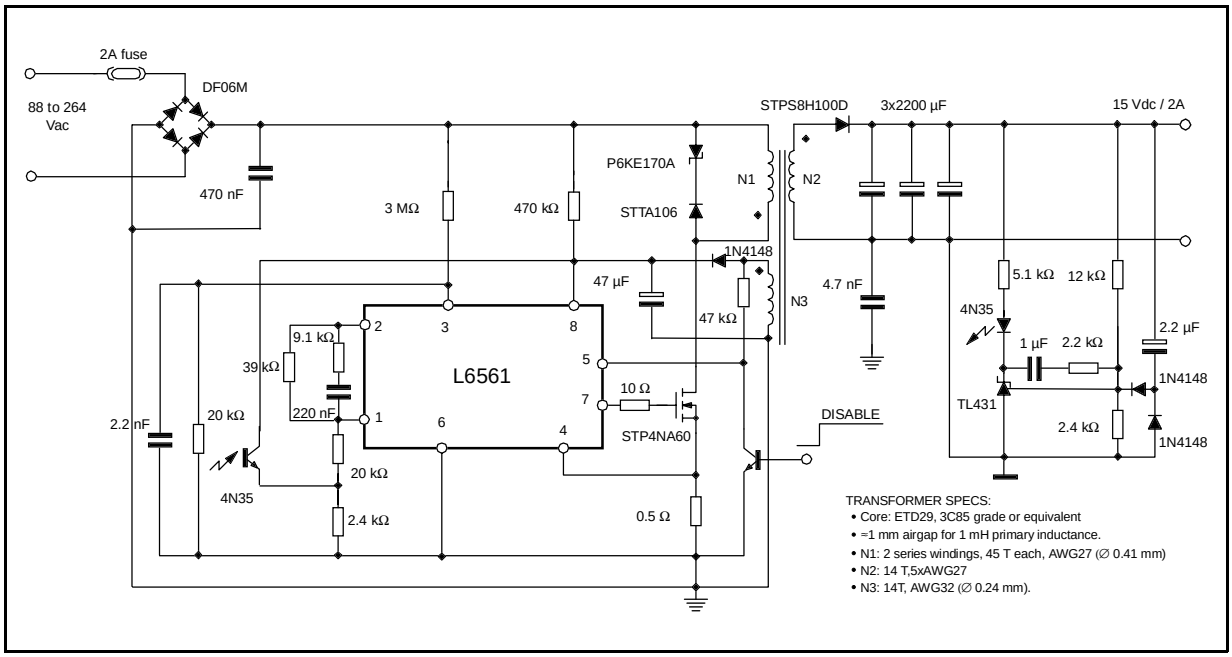


Figure 17. 30W High-PF Flyback with the L6561: evaluation results

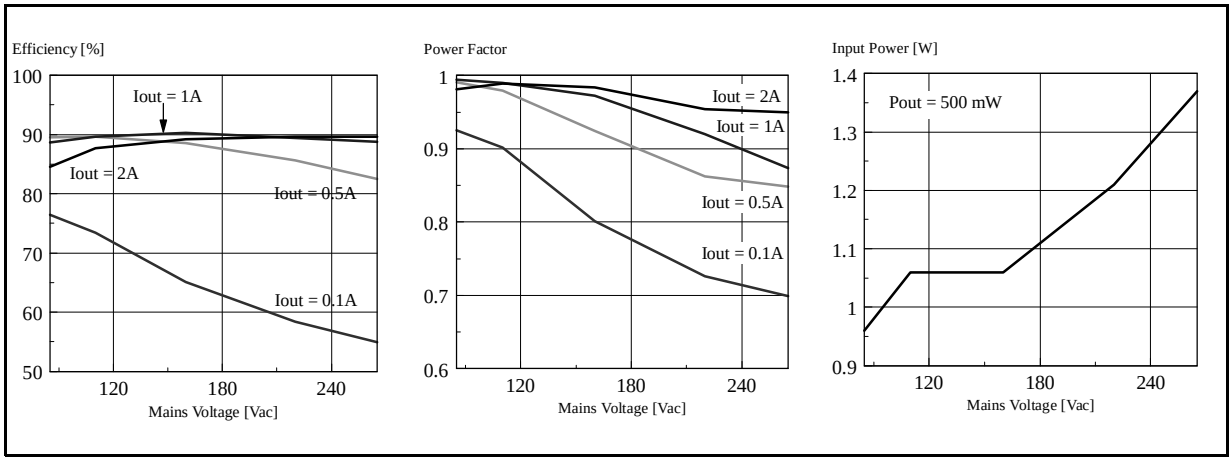
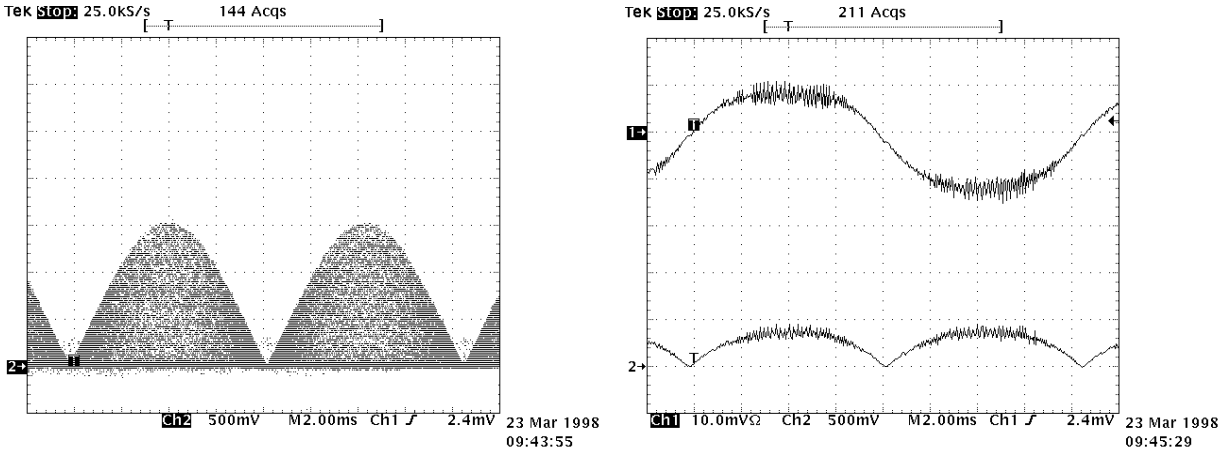


Figure 18. 30W High-PF Flyback with the L6561: principal waveforms



V_{in} = 90 V_{AC}, P_{out} = 30W
Left : Peak primary current envelope
Right, upper trace: Mains current
Right, lower trace: Low-frequency primary current

References

[1] "L6561, Enhanced Transition Mode Power Factor Corrector", (AN966)
[2] "Flyback Converters with the L6561 PFC Controller", (AN1060)