Small-Signal Modeling and Controller Design of BCM Boost PFC converters

Sung-Pei Yang, Shin-Ju Chen and Chao-Ming Huang
Department of Electrical Engineering,
Kun Shan University
Tainan, Taiwan, R.O.C.
spyang@mail.ksu.edu.tw

***Abstract*—In this paper, the small-signal model of a boundary conduction mode (BCM) boost power factor correction (PFC) converter controlled by a peak control current control IC L6561 is derived. Based on the derived mathematical model, a Type II compensator is thus well designed to make the boost converter exhibits the performances of high power factor and output voltage regulation. Finally, a 300 W prototype of the BCM boost PFC converter with IC L6561 is implemented. The performance of high power factor and power efficiency is validated by experimental results. Furthermore, the regulation of output voltage despite the variations of the peak line voltage and load resistances is also verified.**

Keywords- Small-signal model, PFC, BCM, boost converter

I. INTRODUCTION

In general, the active power factor correction (PFC) circuits are usually added between the rectifier and the load to eliminate high harmonics. The two-stage approach includes a PFC stage and a dc/dc stage [1]. The PFC stage is operated in continuous conduction mode (CCM) for higher power applications [2]-[4]. The current control techniques such as multiplier approach control, hysteresis current control, peak current control and average current control were used to correct the power factor. It results in less current stress in the main devices and a reduction of the EMI filter. On the other hand, when the PFC stage is operated in discontinuous conduction mode (DCM), it has an inherent gift of high power factor, and the input current control is thus not necessary for power factor correction to reduce the circuit complexity [5]-[7]. However, the output power of a PFC stage operated in DCM is difficult to increase and thereby just used for lower power applications. Furthermore, converters operated at the boundary of CCM and DCM are said to operate in boundary conduction mode (BCM) or critical mode (CM) [8]-[10]. During a switching cycle, the switch is turned on as the input current drops to zero, and turned off while the input current reaches a desired value. Notably, the diode reverse recovery problem is removed owing to the diode current is zero when the switch turns on. As a result, converters operated in BCM exhibit higher power efficiency than those operated in CCM, and lower current peak value than those operated in DCM.

A well-known commercial integrated circuit (IC) L6561 made by ST Company [X] applied to boost ac/dc converter has been widely accepted in power electronics equipment for high PFC. The boost ac/dc converter controlled by IC L6561 is operated in BCM. However, because and the switching frequencies of a BCM boost PFC converter are variable, its small-signal model is thus rarely investigated in the literature. Accordingly, in this paper, the current injected equivalent circuit approach [11] is adopted to derive the mathematical model. Therefore, a controller can be well designed for the boost converter with IC L6561 to have the performance of output voltage regulation in the presence of input line peak voltage and output load variations.

The paper is organized as follows. The operating principle of the BCM boost PFC converter with IC L6561 is described by using simplified functional block diagrams of IC L6561 in Section II. Section III derives the small-signal model of the proposed converter. Controller design is presented in Section IV. The experimental results are shown in Section V to verify the performances of the BCM boost PFC converter. The conclusion is given in Section VI.

II. OPERATING PRINCIPLE

Fig. 1 depicts a boost PFC converter which is controlled by a control IC L6561 to exhibit the performance of high power factor and output voltage regulation. This control IC make the boost converter operate in boundary conduction mode (BCM) with variable switching frequencies. In order to simplify the analysis, the control IC L6561 is thus presented by the internal block diagrams herein.

Some assumptions about the proposed converter are made before the circuit is analyzed.

1) The inductors and capacitors of the converter are considered to be ideal without parasitic resistances.
2) All switches and diodes of the converter are regarded as the ideal components without switching and conduction losses.
3) The output capacitor voltage ripple Δv_{C_o} are much less than the averaged output capacitor voltage $\overline{v}_{C_o}$. Hence

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the output capacitor voltage v_{C_o} can be regarded as constant during one switching period T_s.

4) The rectified line voltage $v_g(t) = |v_m \sin(\omega t)|$ with $\omega = \pi / T_L$ can be assumed to be constant over one switching period, because the switching period T_S is much less than one half line period T_L.

Moreover, the truth table of a SR Flip-Flop is shown as Fig.2 and used for the steady-state analysis.

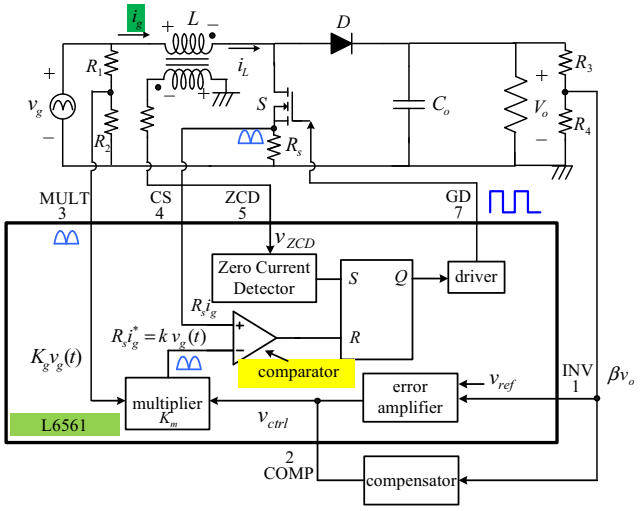


Fig. 1. Boost PFC converter controlled by IC L6561.

Table I Truth table of SR Flip-Flop.

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	forbidden

Based on the switching of the switches and diodes, the proposed converter operating in BCM can be divided into two linear stages in one switching period T_s. The operating principle is described as follows.

Stage 1 [0, t_{on}] (S: on, D: off): The linear equivalent circuit is depicted in Fig. 2. In this stage, since the output of the SR Flip-Flop $Q = 1$, the switch S is turned on and the diode D is reverse-biased. During this stage, the voltage v_g is applied across the inductor L and thus the inductor current i_L rises linearly. As the current i_L increases to the reference input current i_g^*, the state of the output of the current comparator is changed from 0 to 1. Moreover, because the current i_L is still more than zero in this stage, the output of the zero current detector maintain the state 0. Based on the truth table of SR Flip-Flop shown in Table I, its output Q changes state 1 to state 0. The switch S is thus turned off and this stage is finished.

Stage 2 [0, t_{on}] (S: off, D: on): The linear equivalent circuit is depicted in Fig. 3. In this stage, as $Q = 0$, the switch S is off and the diode D is forward-biased. During this stage, the voltage across the inductor L is v_o and thus the inductor current i_L falls linearly. As the current i_L decreases to zero, the output of the zero current detector becomes state 1. Simultaneously, the inductor current i_L is less than i_g^*, so the output of the current comparator is state 0. Accordingly, Q changes state 0 to 1. The switch S is thus turned on again.

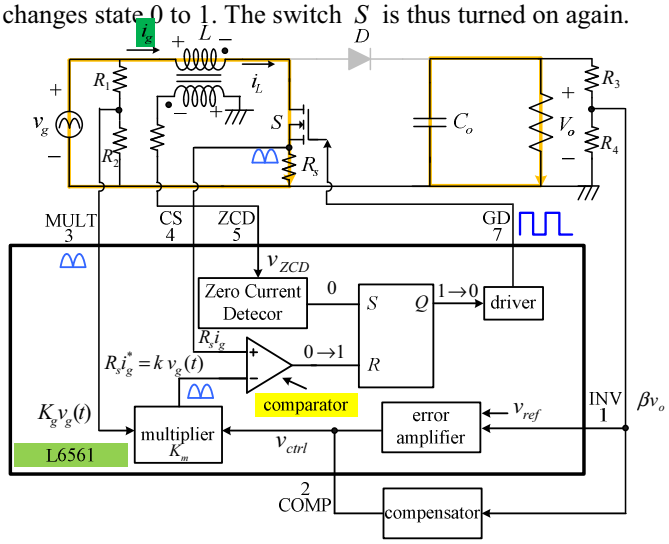


Fig.2. Equivalent circuit in stage 1.

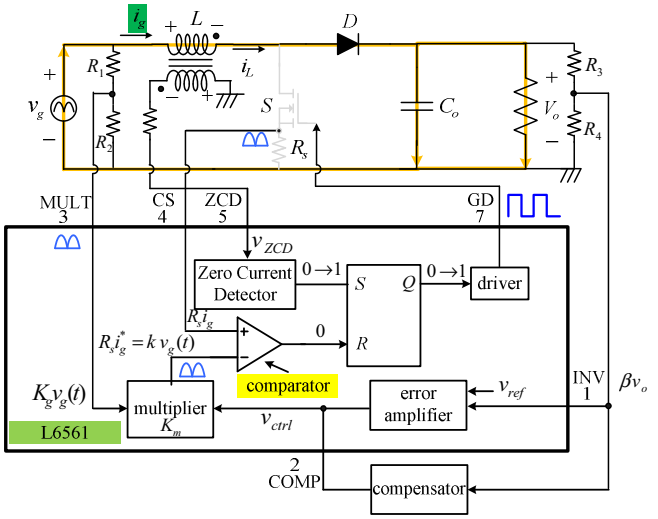


Fig.3. Equivalent circuit in stage 2.

According to the aforementioned analysis, the key waveforms over one switching period T_s are schematically depicted in Fig. 4. It also shows that the converter operates in BCM.

III. Small-Signal Model Derivation

In this section, the ac small-signal model is derived by the current injected equivalent circuit approach to investigate the dynamical behavior of the BCM boost PFC converter. It reveals from Fig. 4 that the averaged diode current $i_D(t)$ over one switching period T_S are given by

$$\bar{i}_D(t)=\frac{1}{2}i_g^*\cdot\frac{t_{off}}{T_s}=\frac{1}{2}i_g^*\cdot\frac{k\,v_g(t)\cdot L}{v_o-v_g(t)}\cdot\frac{1}{kL}\left(\frac{v_o-v_g(t)}{v_o}\right)$$
$$=\frac{1}{2}i_g^*\cdot\frac{v_g(t)}{v_o} \tag{1}$$

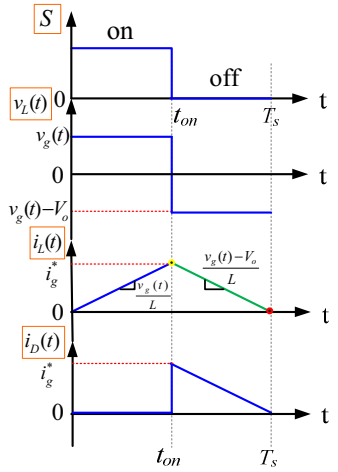


Fig.4. Key waveforms over one switching period T_s.

Moreover, from the inner block diagram of L6561 shown in Fig. 1, the output of the multiplier is

$$R_s i_g^*(t)=k v_g(t)=K_g K_m v_{ctrl} v_g(t) \tag{2}$$

where R_s is the input current sense resistor, K_g is the voltage division ratio of the voltage divider built up by the resistors (R_1, R_2), K_m is the gain of the multiplier and v_{ctrl} is the output of the controller. Substituting (2) into (1), it yields

$$\bar{i}_D(t)=\frac{K_g K_m v_{ctrl} v_g^2(t)}{2R_s v_o} \tag{3}$$

Hence, the moving average over one half line period T_{2L} is given by

$$\left\langle \bar{i}_D(t)\right\rangle_{T_{2L}}=\frac{1}{T_{2L}}\int_0^{T_{2L}}\frac{K_g K_m v_{ctrl}}{2R_s v_o}v_m^2\cdot\left|\sin^2(\omega_{2L}t)\right|dt$$
$$=\frac{K_g K_m v_{ctrl} v_m^2}{4R_s v_o}=:f(v_{ctrl},v_o,v_m) \tag{4}$$

with $v_g(t)=\left|v_m\sin(\omega t)\right|$. To proceed, small perturbations:

$$\begin{cases} v_m=V_m+\tilde{v}_m & V_m>>\left|\tilde{v}_m\right| \\ \left\langle v_o\right\rangle_{T_{2L}}=V_o+\tilde{v}_o & \text{where} \quad V_o>>\left|\tilde{v}_o\right| \\ \left\langle v_{ctrl}\right\rangle_{T_{2L}}=V_{ctrl}+\tilde{v}_{ctrl} & V_{ctrl}>>\left|\tilde{v}_{ctrl}\right| \end{cases}$$

are introduced into (4) and neglect the high order terms, we thus have the linearized small-signal model given by

$$\tilde{i}_D=g_1\tilde{v}_{ctrl}+g_2\tilde{v}_m-\frac{1}{r_1}\tilde{v}_o\,. \tag{5}$$

The parameters are defined as

$$g_1=\frac{K_g K_m V_m^2}{4R_s V_o},\quad g_2=\frac{K_g K_m V_{ctrl} V_m}{2R_s V_o},\quad \frac{1}{r_1}=\frac{K_g K_m V_{ctrl} V_m^2}{4R_s V_o^2}\,. \tag{6}$$

Therefore, the small-signal equivalent output circuit of the BCM boost PFC converter described by (5) is schematically depicted in Fig. 5. Moreover, Fig. 6 presents the block diagram of the small-signal equivalent output circuit in Fig. 5.

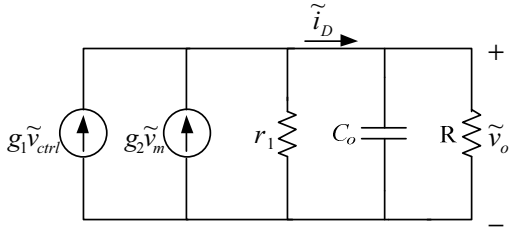


Fig. 5. Small-signal equivalent output circuit of the BCM boost PFC converter.

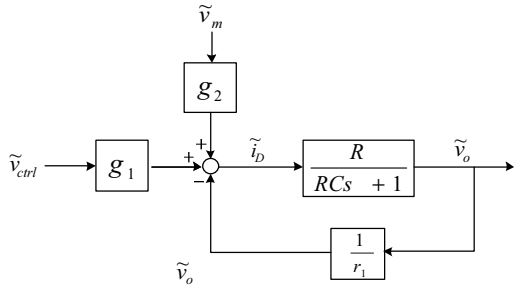


Fig. 6. Block diagram of the Small-signal equivalent output circuit.

Based on Fig. 6, the transfer functions from line to output and control signal to output are

$$\left.\frac{\tilde{v}_o(s)}{\tilde{v}_m(s)}\right|_{\tilde{v}_{ctrl}=0}=\frac{g_2 r_1 R}{RC_o r_1 s+(r_1+R)}=\frac{\frac{g_2}{C_o}}{s+\frac{r_1+R}{Rr_1C_o}} \tag{7}$$

$$\left.\frac{\tilde{v}_o(s)}{\tilde{v}_{ctrl}(s)}\right|_{\tilde{v}_m=0}=\frac{g_1 r_1 R}{RC_o r_1 s+(r_1+R)}=\frac{\frac{g_1}{C_o}}{s+\frac{r_1+R}{Rr_1C_o}}\,. \tag{8}$$

However, in order to derive the numerical small-signal model, the value of V_{ctrl} around dc operating point and gain of the multiplier K_m must be also determined. According to the conservation of power, one gets

$$K_m=\frac{2R_s\left\langle P_o\right\rangle_{T_{2L}}}{K_g V_{ctrl}\eta\cdot v_{in,rms}^2}\,. \tag{9}$$

On the other hand, from the application note of IC L6561 [12], it gives the equation

$$K_m=0.651\cdot(1-85.29e^{-1.776V_{ctrl}})\,. \tag{10}$$

For the design specifications listed in Table II, the values of $V_{ctrl}=2.995$ and $K_m=0.38$ can be determined from the

intersection of the curves (a) and (b) in Fig. 7 defined in (9) and (10), respectively. As a result, the transfer functions in (7) and (8) are given by

$$\left.\frac{\tilde{v}_o(s)}{\tilde{v}_m(s)}\right|_{\tilde{v}_{ctrl}=0} = \frac{84.6}{s+45} \tag{11}$$

$$\left.\frac{\tilde{v}_o(s)}{\tilde{v}_{ctrl}(s)}\right|_{\tilde{v}_m=0} = \frac{5194.6}{s+45}. \tag{12}$$

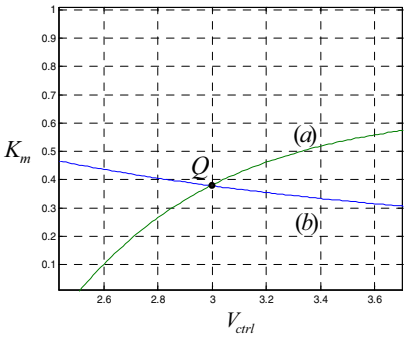


Fig. 7. Dependence of K_m on V_{ctrl}.

IV. Controller Design

It reveals from Fig. 6 that the model dynamics of the proposed converter depends on the line peak voltage variation $\tilde{v}_m$ and load R. Based on the transfer function depicted in (12), a voltage controller is thereby needed to tightly regulate the output voltage despite variations in the line voltage and load resistance. Fig. 8 is the block diagram of the closed-loop system. The controller $C(s)$ is designed to make the overall system to satisfy the following conditions:

1) Steady state error $e_{ss}|_{step}$ is zero.

2) Phase Margin is more than $45°$.

3) Bandwidth of the closed-loop system is 10~20 Hz.

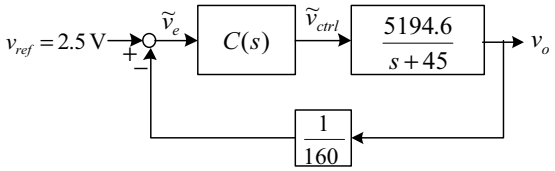


Fig. 8. Block diagram of the closed-loop system.

Therefore, from a control point of view, an integrator is needed to eliminate the steady-state error, and a phase lead compensator is added to improve the transient response. As a result, a Type-II controller is designed as

$$C(s) = 1000\frac{s+45}{s(s+450)}. \tag{12}$$

As a result, the Bode plot of the closed-loop transfer function from the reference voltage input to the output is depicted in Fig. 9. The bandwidth is 85.2 rad/sec (=13.6 Hz).

TABLE II

Specifications and Component Values

Input voltage $V_{in,rms}$	90~265 V	Output power P_o	300 W
Inductance L_i	300 μH	Output voltage V_o	400 V
Output capacitance C_o	300 μF	Load resistances R_L	3200~ 533 Ω

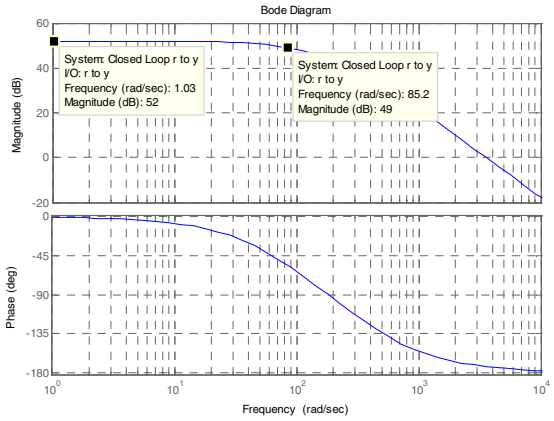


Fig. 9. Bode plot of the closed-loop system.

V. Experimental Results

A 300 W prototype of the BCM boost PFC converter controlled by IC L6561 is built and tested to verify the performances of high power factor, output voltage regulation and power efficiency.

A) High Power Factor

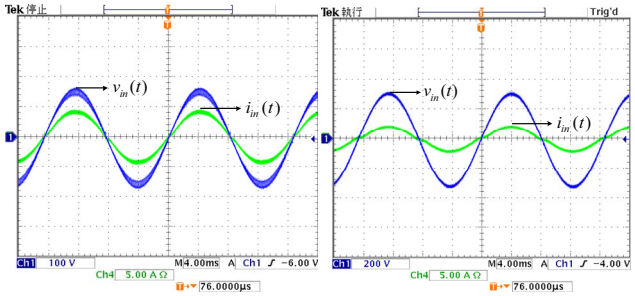
It reveals from Fig. 10 that the input line current can follow the input line voltage, and the converter thereby exhibits high power factor. Moreover, the harmonic spectrum for the input line current is presented in Fig. 11. The comparison with the IEC 61000-3-2 Class D standards is shown in Fig. 12. It shows that all input line current harmonics are below the requirements of IEC 61000-3-2 Class D standards. Moreover, the power factor graph varies with the output power is depicted in Fig. 13.

B) Output Voltage Regulation

Fig. 14 and Fig .15 are the output voltage responses under input line peak voltage and output load variations, respectively. These experimental results are measured to verify that the designed controller can well regulate the output voltage in the presence of variations in line peak voltage and output load.

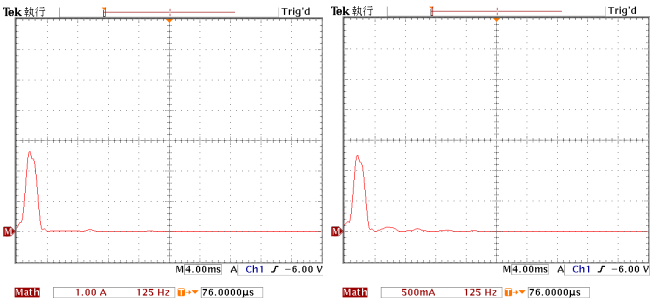
C) Power Efficiency

Fig. 16 shows the measured efficiency versus various output power for two different input line voltages. It reveals that the higher input line voltage resulted in the higher efficiency. The highest efficiency of the implemented converter is 96.4 %.



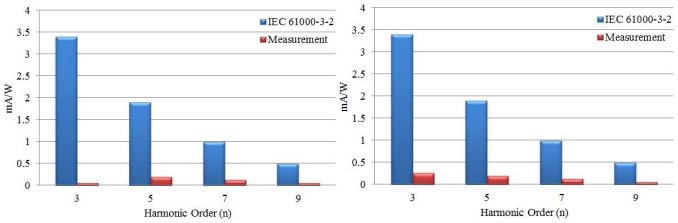
(a) $V_{in,rms}=110$ V (b) $V_{in,rms}=220$ V

Fig. 10. Waveforms of input voltage and input current.



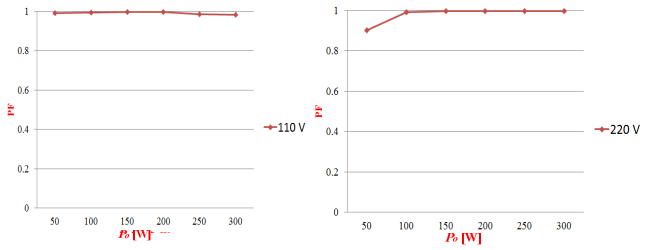
(a) $V_{in,rms}=110$ V (b) $V_{in,rms}=220$ V

Fig. 11. Harmonic spectrum for input line current.



(a) $V_{in,rms}=110$ V (b) $V_{in,rms}=220$ V

Fig. 12. Harmonic spectrum for input line current compared with the IEC 61000-3-2 Class D standards.



(a) $V_{in,rms}=110$ V (b) $V_{in,rms}=220$ V

Fig. 13. Power factor vs. output power.

VI. Conclusions

A boost converter controlled by IC L6561 is operated in BCM. Therefore, the boost converter exhibits high power factor. The small-signal model of the BCM boost PFC converter is derived by the current injected equivalent circuit approach in this paper. The Type II controller is thereby well designed to regulate the output voltage despite the variations of input line peak voltage and output load. Finally, a 300 W prototype of the BCM boost PFC converter is built. The experimental results are measured to validate the performances of high power factor, output voltage regulation and power efficiency.

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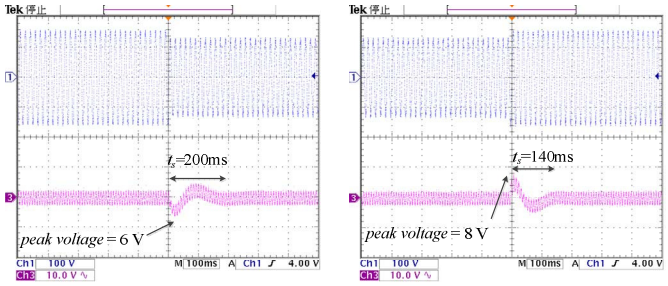
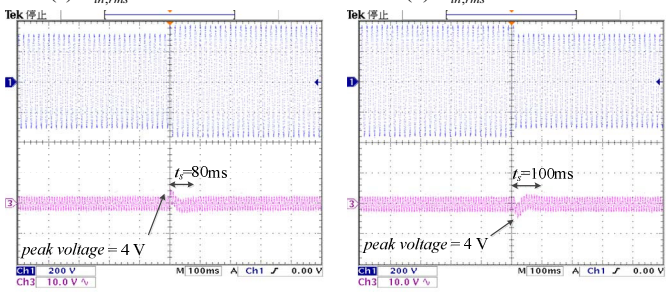
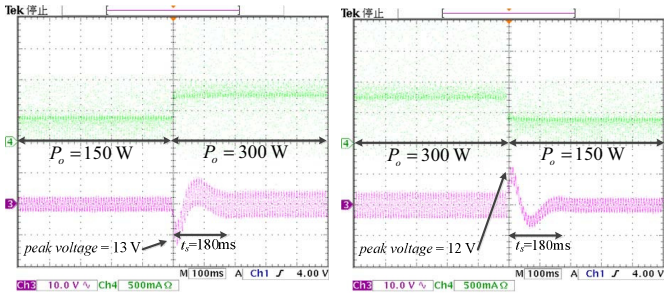


(a) $V_{in,rms}=110\rightarrow 90$ V (b) $V_{in,rms}=90\rightarrow 110$ V

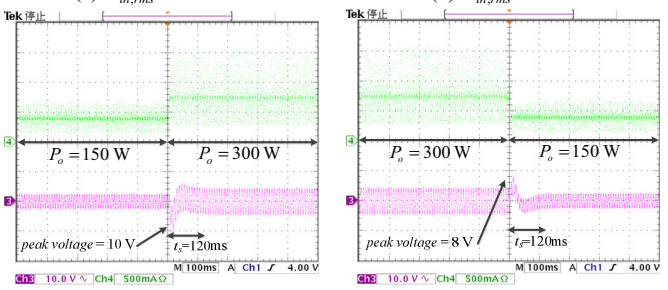


(c) $V_{in,rms}=220\rightarrow 260$ V (d) $V_{in,rms}=260\rightarrow 220$ V

Fig. 14. Output responses under input line voltage variations at $P_o=300$ W .



(a) $V_{in,rms}=110$ V (b) $V_{in,rms}=110$ V



(c) $V_{in,rms}=220$ V (d) $V_{in,rms}=220$ V

Fig. 15. Output responses under output load variations.

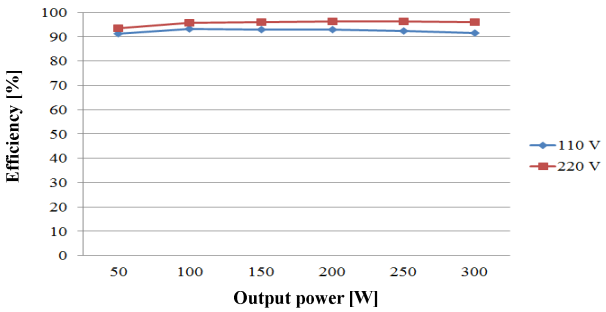


Fig. 16. Measured efficiency curves at various input line voltages.

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