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Single-phase ac to high-voltage dc converter with soft-switching and diode-capacitor voltage multiplier

Chung-Ming Young[1], Sheng-Feng Wu[1], Ming-Hui Chen[2], Sing-Jhao Chen[1]

[1]Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan
[2]Instrument Division, Motech Industries, Inc., New Taipei city, Taiwan
E-mail: young@ee.ntust.edu.tw

Abstract: This paper proposes a single-phase, soft-switching, high step-up ac–dc converter based on a diode-capacitor voltage multiplier (DCVM) with a power factor correction (PFC). By applying the PFC technology, the proposed converter promises a near-unity power factor and a low distortion line current, while providing an adjustable, high step-up dc voltage that the conventional DCVM circuits cannot achieve. To reduce the switching losses, an auxiliary circuit for implementing a soft commutation is added to the power stage of the proposed converter. For operating at a fixed switching frequency, both the main and the auxiliary switches in the power stage are turned off with the zero-current transmission (ZCT). The operating principle, the design considerations and the control strategy of the proposed converter all are detailed and investigated in this paper. A 1.2 kV/500 W laboratory prototype, which employs a commercial PFC IC UC3854 as a controller, is built for test, measurement and evaluation. Under the full-load conditions, the measured power factor, the total harmonic distortion of the line current and the system efficiency are 99.6, 4.86 and 94%, respectively. The experimental results demonstrate the validity of the proposed converter.

1 Introduction

High-voltage dc power supplies are necessary in many industrial applications, such as lasers, lamps, X-ray systems, dust-filtering, insulating test and electrostatic coating. Some isolated, high step-up dc–dc converters, designed to achieve a high-voltage gain by using high step-up transformers, have been proposed [1–3]. One problem with these converters is that the power devices have to withstand high-voltage and current spikes, induced by the non-ideal characteristics of these high-turn-ratio transformers. To increase the efficiency and reduce the voltage and/or the current stresses, these converters are often associated with the soft-switching and regeneration techniques [4–6]. Without the transformers, many non-isolated, high step-up dc–dc converters employing coupled inductors [7], cascaded techniques [8] and voltage multipliers [9] have been developed. These non-isolated converters were popular for the renewable energy systems, such as the photovoltaic and the fuel cell systems. In most applications, conventional full-bridge diode rectifiers were used as the front-end converter because of their reliability, simplicity and cost-effectiveness. Nevertheless, the diode rectifiers produce poor power factors and rich current harmonics at the input ac mains in these applications, and poorly regulate the dc voltage. To improve these problems and comply with the existing harmonic standards, such as EN61000-3-2, power factor correction (PFC) techniques became good candidates for the ac-sourced power conversion systems [10].

Conventional PFC boost topologies, integrating a full-bridge diode rectifier and a boost dc–dc converter to obtain a high-power factor and a low ac current distortion, were subsequently proposed and well developed [11]. In these topologies, more than two semiconductor switches in the current path lead to an increased conducting loss, which causes a deterioration in the system's efficiency. Many bridgeless PFC converters, then, have been proposed to reduce the conduction loss by eliminating the diode bridge [12]. To further improve the efficiency, various soft-switching technologies for the conventional or the bridgeless PFC converters have also been proposed [13]. However, when a high-voltage gain is desired, these front-end PFC converters strain to provide a high-voltage gain, because of their limited duty range in the practical applications, and still have to integrate an extra high step-up dc–dc converter. These two-stage PFC topologies produce higher costs, losses and complexities in the system implementation.

Recently, a number of single-stage PFC converters using a single controller and fewer power components have been presented for simplifying the control design, saving cost and improving the efficiency. However, most of these converters have been introduced in the low-voltage dc applications [14]. Until now, only a few single-stage PFC topologies have been presented in the high-voltage dc applications. Shenkman *et al.* [15] proposed a single-stage, transformerless topology integrated with a single-phase ac–ac converter with a Dickson charger pump circuit for achieving a high-voltage gain and improving the line

condition. Nevertheless, in this topology, the voltage gain depended on the duty cycle of the switch current, the capacitor current, the switching frequency and the switching load resistance, leading to complicated design considerations. Suryawanshi and Tarnekar [16] presented an ac–dc converter composed of a diode rectifier, a series resonant converter with an H-bridge configuration, a high-frequency high step-up transformer and a second diode rectifier. This topology achieved a high-power factor without any active control on the line current, and both the variable frequency control and the duty ratio control could be used to regulate the output voltage; however, it drew a poor line quality at a light load.

Providing the advantages of a high-voltage gain, low-voltage stress on the diodes and the capacitors, compactness and cost efficiency, the well-known diode-capacitor voltage multiplier (DCVM) shown in Fig. 1*a*, which is also known as the Cockcroft–Walton VM, has been widely applied in the high-voltage dc applications for a long time [17–19]. However, its disadvantages include a poor power factor, a half-wave asymmetry and a high-distorted line current and a bad output voltage regulation. Young and Chen [1] presented a single-stage, single-phase ac to high-voltage dc converter based on the conventional DCVM without a step-up transformer for reducing the aforementioned drawbacks. As shown in Fig. 1*b*, by placing one boost inductor and one bidirectional switch between the ac mains and a DCVM, this converter provided simplicity, high efficiency, good line conditioning and regulated the dc output. Moreover, the control strategy used in the conventional PFC boost converters could be easily adapted for this converter, which simplifies the design process. However, only a hard switching was investigated in this topology.

To improve the efficiency, this paper deploys a soft-switching auxiliary circuit into the converter shown in Fig. 1*b*, and forms the proposed topology as shown in Fig. 1*c* [20]. The proposed converter not only maintains the

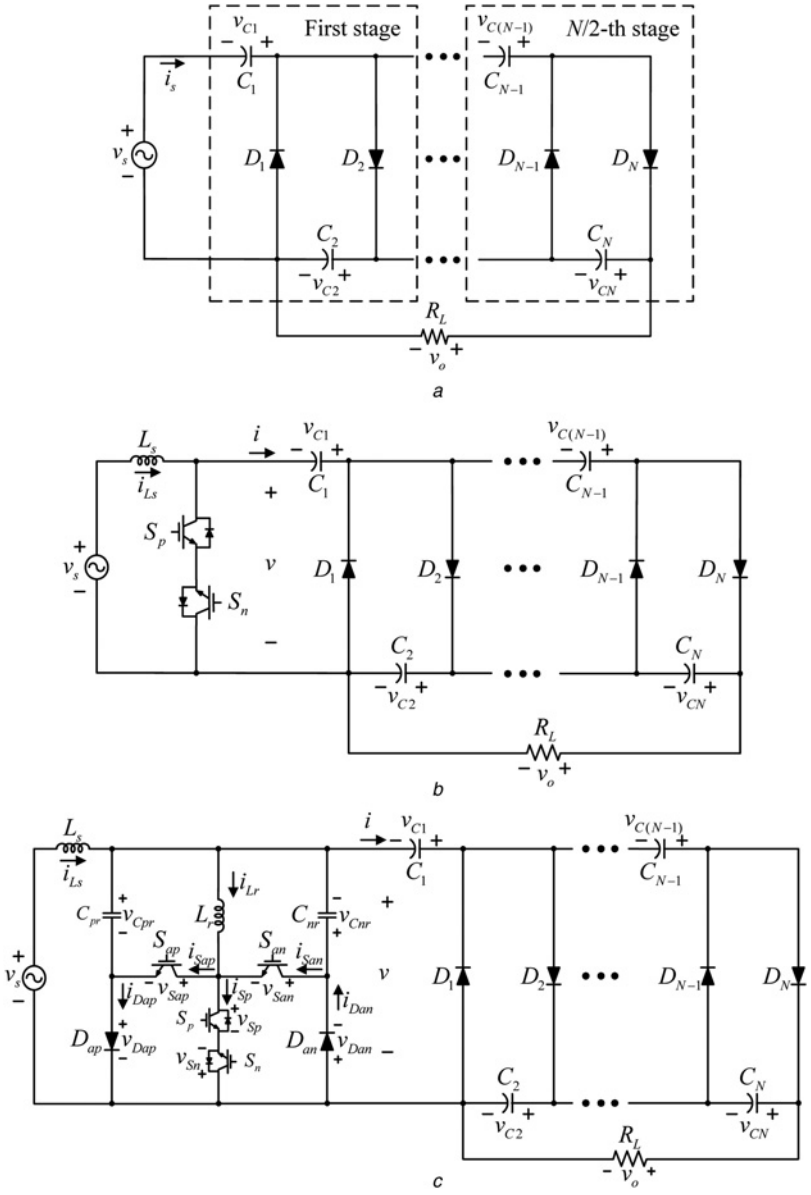

Fig. 1 *Evolution of the proposed soft-switching diode-capacitor voltage multiplier*

a Conventional asymmetric DCVM topology
b Topology with a hard-switching operation proposed by Young and Chen [1]
c Proposed topology with a soft-switching operation

advantages of Fig. 1*b*, but also increases efficiency through the soft switching mechanism, in which both the main and the auxiliary switches are turned off with the ZCT. Originally, the auxiliary soft-switching topology, as shown in Fig. 2*a*, was proposed by Lee *et al.* [21] to achieve the ZCT for a DC/DC converter. In this paper, the main switch was replaced by a bidirectional switch and two auxiliary switches, two resonant capacitors and two diodes deployed symmetrically to deal with both the positive- and the negative-half cycles. For the high-power and the high-voltage applications, an insulated gate bipolar transistor (IGBT) is preferred, because the IGBTs have a lower conduction loss and a higher voltage rating. In addition, the ZCS techniques can be used to solve the IGBTs' tail current problem [22]. The operating principle, the design considerations and the control strategy of the proposed converter will be investigated in this paper. A 1.2 kV/500 W laboratory prototype, which adapts a commercial PFC IC (UC3854) as its controller, has been built for test, measurement and evaluation.

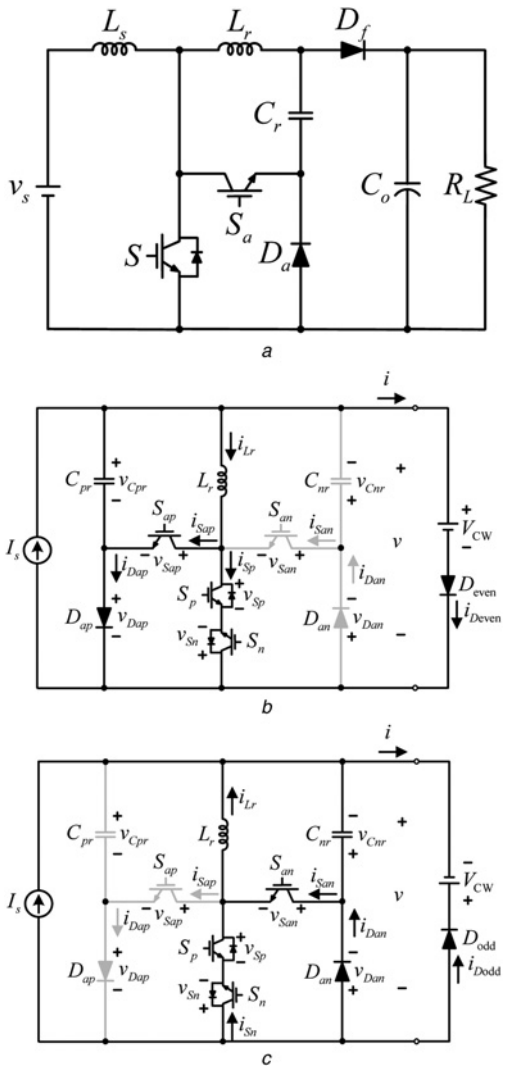

Fig. 2 *Topology of an earlier soft-switching dc/dc converter and the two equivalent circuits of the proposed converter*

a Soft-switching dc/dc boost converter proposed by reference [21]
b Equivalent circuit of the proposed converter during a positive-half line cycle
c Equivalent circuit of the proposed converter during a negative-half line cycle

2 Operation principle

In the following section, the soft switching mechanism will be investigated. As shown in Fig. 1*c*, the proposed converter is comprised of one boost inductor L_s, one bidirectional switch formed by two anti-series IGBTs (S_p, S_n) as the main switches, an auxiliary soft-switching circuit, and one n-stage DCVM. The auxiliary soft-switching circuit consists of two auxiliary switches (S_{ap}, S_{an}), two auxiliary diodes (D_{ap}, D_{an}), two resonant capacitors (C_{pr}, C_{nr}) and one resonant inductor L_r, where the subscripts p and n denote the operations corresponding to the positive- and the negative-half line cycles, respectively. The n-stage DCVM is constructed by the cascading n diode-capacitor stages, with each stage containing two capacitors and two diodes. For convenience, both the capacitors and the diodes are divided into odd groups and even groups according to their suffixes, as denoted in Fig. 1*c*. The operation of the proposed soft-switching converter is almost similar to that of its hard-switching counterpart in Fig. 1*b*, except during the switching transients. For obtaining soft switching properly, a minimum turn-on time is required for the auxiliary switches S_{ap} and S_{an}. Only the steady-state condition is considered, to simplify the description of the circuit operation. Before analysing, some assumptions are made as follows:

(1) All the circuit components are ideal, and there is no power loss in the system.
(2) The proposed converter operates in the continuous conduction mode.
(3) The boost inductor L_s is much larger than the resonant inductor L_r, thus the line current i_s can be considered as a constant current within one switching cycle.
(4) All the capacitors in the DCVM are sufficiently large, and the voltage fluctuations and the ripples of each capacitor can be ignored under a reasonable load condition. Therefore, the voltages across all the capacitors are equal, except for the first capacitor whose voltage is one half of the others, that is, V_o/N for the first capacitor and $2V_o/N$ for the others, where V_o is the average dc output voltage and $N = 2n$.
(5) When the input terminal current i_γ of the DCVM is positive (negative), only one of the even (odd) diodes will conduct. These phenomena and the sequence of the conductions were investigated in [1].

According to these assumptions, two current-fed equivalent circuits, related to the positive- and the negative-half line cycles of the proposed converter within one switching cycle, are depicted in Figs. 2*b* and *c*, respectively, in which I_s represents the line current according to assumption 3, D_{even} (D_{odd}) represents the only conducting even (odd) diode and $V_{CW} = V_o/N$ represents the equivalent combined voltage of the capacitors in the DCVM. For convenience, only the operation in the positive-half line cycle is investigated in this section. The operation in the negative-half cycle can be obtained by a similar process. In one switching cycle, there are seven operation stages; the corresponding subcircuits are shown in Figs. 3*a*–*g*, respectively. Fig. 4 shows some selected theoretical waveforms including the switching signals for the main and the auxiliary switches, in which S_n keeps the on-state, S_{an} keeps the off-state in the whole positive-half cycle and D is the duty ratio of the main switch S_p. Prior to the first stage, the main switch S_p remains in the off-state, the line current flows into the DCVM through one of the conducting even diode, the resonant inductor current

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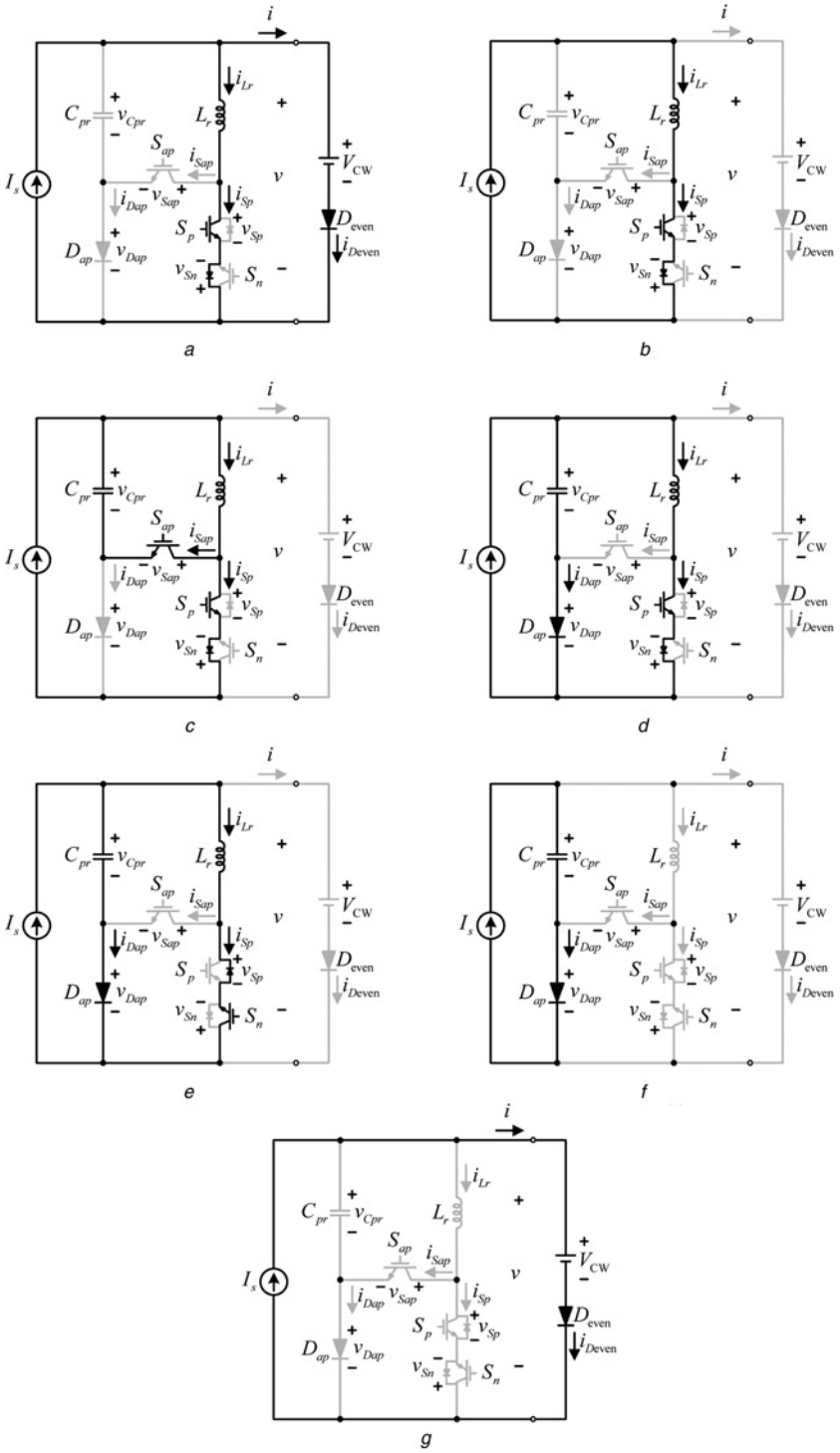

Fig. 3 *Seven sub-circuits of the proposed converter in one switching cycle during a positive-half cycle*

a Stage 1: $[t_0 < t < t_1]$
b Stage 2: $[t_1 < t < t_2]$
c Stage 3: $[t_2 < t < t_3]$
d Stage 4: $[t_3 < t < t_4]$
e Stage 5: $[t_4 < t < t_5]$
f Stage 6: $[t_5 < t < t_6]$
g Stage 7: $[t_6 < t < t_7]$

i_{Lr} falls to zero and the resonant capacitor voltage v_{Cpr} is charged to V_{o}/N.

Stage 1: $[t_0 < t \leq t_1]$ (Fig. 3*a*)

This stage begins when the S_p turns on with the ZCT at $t = t_0$, because of the resonant inductor L_r. The equivalent voltage $V_{\mathrm{CW}} = V_{\mathrm{o}}/N$ is across on the L_r, thus the i_{Lr} increases linearly from zero. During stage 1, the resonant capacitor voltage v_{Cpr} keeps the pre-charged voltage V_{o}/N. This stage ends when the i_{Lr} reaches I_s, then the D_{even} turns off at $t = t_1$ with the ZCT. The time interval of this stage is

$$\Delta t_1 = t_1 - t_0 = \frac{NL_rI_s}{V_{\mathrm{o}}} \tag{1}$$

Stage 2: $[t_1 < t \leq t_2]$ (Fig. 3*b*)

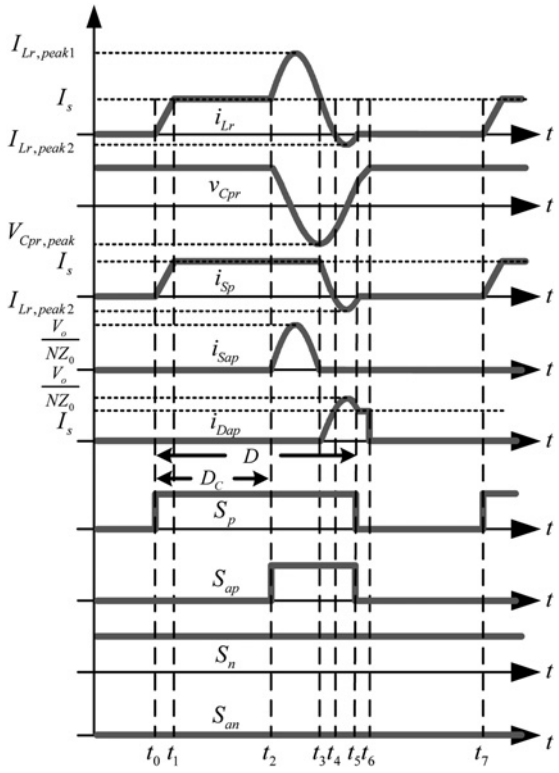

Fig. 4 *Theoretical waveforms of the proposed converter in one switching period during a positive-half line cycle including the switching signals of the main and the auxiliary switches*

In this stage, i_{Lr} flows through the L_r, the S_p and the body diode of the S_n. During this stage, the circuit operation is similar to the turn-on stage of a conventional boost converter, and the v_{Cpr} still keeps the pre-charged voltage V_o/N. This stage ends when the auxiliary switch S_{ap} turns on. The relative equations of this stage are given as

$$i_{Lr}(t) = I_s \tag{2}$$

$$v_{Cpr}(t) = \frac{V_o}{N} \tag{3}$$

$$\Delta t_2 = t_2 - t_1 = D_c T_{sw} - \Delta t_1 \tag{4}$$

where D_c is generated from the controller (UC3854), which is the duty ratio between the rising edges of S_p and S_{ap} and T_{sw} is the switching period.

Stage 3: $[t_2 < t \le t_3]$ (Fig. 3*c*)

When the S_{ap} turns on with the ZCT at $t = t_2$, the resonant behaviour between L_r and C_{pr} starts with I_s and V_o/N as the initial conditions. The inductor current and the capacitor voltage and their corresponding peaks are given as

$$i_{Lr}(t) = I_s + \frac{V_o}{NZ_0}\sin\omega_0(t - t_2) \tag{5}$$

$$v_{Cpr}(t) = \frac{V_o}{N}\cos\omega_0(t - t_2) \tag{6}$$

$$I_{Lr,peak1} = I_s + \frac{V_o}{NZ_0} \tag{7}$$

$$V_{Cpr,peak} = -\frac{V_o}{N} \tag{8}$$

where Z_0 and ω_0 are the characteristic impedance and the resonant frequency. During this stage, I_s still flows through L_r, S_p and the body diode of S_n. This stage ends when the i_{Lr} reaches I_s again. The time interval of this stage is

$$\Delta t_3 = t_3 - t_2 = \frac{\pi}{\omega_0} \tag{9}$$

Stage 4: $[t_3 < t \le t_4]$ (Fig. 3*d*)

When the i_{Lr} equals I_s again, the S_{ap} turns off with the ZCT. The resonance still continues with the path of the C_{pr}, the L_r, the D_{ap}, the S_p and the body diode of S_n; thus, the resonant current and the voltage can still be obtained from (5) and (6). This stage ends when i_{Lr} falls to zero at $t = t_4$, and the time interval of this stage is

$$\Delta t_4 = t_4 - t_3 = \frac{1}{\omega_0}\sin^{-1}\left(\frac{NI_sZ_0}{V_o}\right) \tag{10}$$

Stage 5: $[t_4 < t \le t_5]$ (Fig. 3*e*)

When i_{Lr} becomes negative, the S_p turns off with the ZCT. The resonance still continues with the paths of the C_{pr}, the L_r, the D_{ap}, the S_n and the body diode of S_p; thus, the resonant current and the voltage can still be obtained from (5) and (6). The negative peak inductor current is given by

$$I_{Lr,peak\ 2} = I_s - \frac{V_o}{NZ_0} \tag{11}$$

This stage ends when the i_{Lr} reaches zero again at $t = t_5$, S_n and the body diode of S_p turn off with the ZCT, and the time interval of this stage is

$$\Delta t_5 = t_5 - t_4 = \frac{1}{\omega_0}\left[\pi - 2\sin^{-1}\left(\frac{NI_sZ_0}{V_o}\right)\right] \tag{12}$$

Stage 6: $[t_5 < t \le t_6]$ (Fig. 3*f*)

In this stage, without the resonance, I_s flows through C_{pr} and D_{ap}, thus v_{Cpr} increases linearly towards V_o/N. The inductor current i_{Lr} remains zero and the v_{Cpr} is given as

$$v_{Cpr}(t) = \frac{I_s}{C_{pr}}(t - t_5) - \frac{V_o}{N}\cos\left[\pi - \sin^{-1}\left(\frac{NI_sZ_0}{V_o}\right)\right] \tag{13}$$

This stage ends at $t = t_6$ when the v_{Cpr} reaches V_o/N. Then, the D_{ap} turns off and the D_{even} turns on. The time interval of this stage is

$$\Delta t_6 = t_6 - t_5 = \frac{V_oC_{pr}}{NI_s}\left\{1 + \cos\left[\pi - \sin^{-1}\left(\frac{NI_sZ_0}{V_o}\right)\right]\right\} \tag{14}$$

Stage 7: $[t_6 < t \le t_7]$ (Fig. 3*g*)

In this stage, all the main and auxiliary switches are turned off, the line current I_s flows through V_{CW} and D_{even} and the circuit operation is similar to the turn-off state of a conventional boost converter. This stage ends when the S_p turns on again and the next switching cycle starts. The time interval of this stage is

$$\Delta t_7 = t_7 - t_6 = T_{sw} - \sum_{i=1}^{6}\Delta i \tag{15}$$

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Before investigating the soft commutation of the proposed converter, the operation of its predecessor in Fig. 1*b* will be described briefly in the following paragraphs. According to [1], there are four operational modes of this circuit, which are determined by the polarity of the ac source and the state of the bidirectional main switch. The static voltage ratio between the dc output voltage and the ac line voltage was derived as

$$M(D) = \frac{V_o}{|V_s|} = \frac{N}{1-D} \tag{16}$$

where $M(D)$ represents the static voltage gain of the proposed converter, $|V_s|$ is the absolute value of the input line voltage and D is the duty cycle of the bidirectional main switch over one switching period. Then, the current ratio between the input terminal current i_γ of the DCVM and the line current i_s was given by

$$\frac{i_\gamma}{i_s} = 1 - D \tag{17}$$

Then, through the average value of *the* $i_\gamma(t)$ over one positive-half cycle, the output ripple of an n-stage DCVM in the one line cycle was obtained as [1]

$$\delta v_o = \sum_{i=2,4,\ldots}^{N} \frac{T_s I_o}{C} \cdot \left(\frac{N-i+1}{2}\right) \tag{18}$$

where T_s, I_o and C are the period of the line voltage, the average output current and the capacitance of the capacitors in the DCVM, respectively. This equation can be used to specify the capacitance of the capacitors in the DCVM by a given voltage ripple. According to the theoretical waveforms in Fig. 4 and the previous analysis of the circuit operation, the duty ratio of the main switch can be given as

$$D = D_c + \frac{\Delta t_3 + \Delta t_4 + \Delta t_5}{T_{sw}} \tag{19}$$

By substituting (9), (10), (12) and (19) into (16), the theoretical voltage gain of the proposed converter with the soft-switching mechanism under consideration can be obtained as

$$\frac{V_o}{|V_s|} = \frac{N}{1 - \left\{D_c + (f_{sw}/\omega_0)\left[2\pi - \sin^{-1}\left((N|I_s|Z_0/V_o)\right)\right]\right\}} \tag{20}$$

where f_{sw} is the switching frequency.

3 Design considerations

In this section, the design considerations of the major circuit parameters are investigated to achieve proper soft-switching operations. First, to ensure that the S_p turns off with the ZCS, the conduction interval of the S_{ap} should meet the following condition

$$\Delta t_{on,Sap} \geq \Delta t_3 + \Delta t_4 \tag{21}$$

Thus, the conduction interval of the S_p can be obtained by

$$\Delta t_{on,Sp} \geq \sum_{i=1}^{4} \Delta t_i\big|_{I_{s,\max}} \tag{22}$$

where $I_{s,\max}$ is the maximum peak value of the line current. The soft-switching mechanism is based on the resonant behaviour between the L_r and the C_{pr}. On the other hand, the L_r can restrict the reverse recovery current produced by the diodes in the DCVM, thus a small value of the L_r may result in a large recovery current from the DCVM. The common way of computing the L_r is to set the period of the resonance not less than four times t_{rr} [23], where t_{rr} is the reverse recovery time of the associated diodes. The resonant behaviour occurs in stages 3 and 4, therefore

$$\Delta t_3 + \Delta t_4 \geq 4t_{rr} \tag{23}$$

According to stage 5, $I_{Lr,\ peak2}$ has to be negative during any switching cycle, thus the relationship between the maximum peak line current and the resonant components is given by

$$\frac{V_o}{NZ_0} \geq I_{s,\max} \tag{24}$$

By ignoring the ringing effect, the voltage stresses posed on the main and the auxiliary switches and all the diodes are determined by the equivalent voltage $V_{CW} = V_o/N$, and the current stresses posed on the main switches are $I_{s,\ max}$, while the maximum current carried by the auxiliary switches are the peak value of the resonant current, that is, $I_{Sap,\ peak} = (V_o/NZ_0)$.

To demonstrate the benefit of the proposed soft-switching topology, Table 1 compares the power losses in the switches both for the hard-switching and the soft-switching circuits [24]. According to the analysis of the circuit operation and the designations, the specification of the selected components can be used to determine the losses of the main devices for hard-switching and soft-switching, respectively. Based on the previous analyses, the proposed converter's main and auxiliary switches are turned off with the ZCS. Therefore the switching losses on the switches, and the reverse-recovery losses on the diodes, can be

Table 1 Comparison of the power losses in hard-switching and soft-switching

Type of loss	Hard-switching	Soft-switching
switching loss $P_{S,\ sw}$	$f_{sw}\cdot[E_{on}+E_{off}]\cdot(V_{CE}/V_{CE,\ Data})\cdot(I_{avg}/I_{C,\ Data})$	none
conduction loss on switch $P_{S,\ con}$	$I_{S,\ rms}\cdot V_{CE}$	$I_{S,\ rms}\cdot V_{CE}$
conduction loss on diode $P_{D,\ con}$	$I_D\cdot V_F$	$I_D\cdot V_F$
reverse-recovery loss on parasitic diode $P_{Pd,\ con}$	$Q_{rr}\cdot V_{Pd,\ peak}\cdot f_{sw}$	none
reverse-recovery loss on DCVM diode $P_{Cd,\ con}$	$Q_{rr}\cdot V_{Cd,\ peak}\cdot f_{sw}$	$Q_{rr}\cdot V_{Cd,\ peak}\cdot f_{sw}$
loss on resonant capacitor P_{Rc}	none	$I^2_{C,rms}\cdot r_{Rc}$
loss on DCVM capacitor P_{Cc}	$I^2_{C,rms}\cdot r_{Cc}$	$I^2_{C,rms}\cdot r_{Cc}$

E_{on}: Turn-on energy loss from the data sheet.
E_{off}: Turn-off energy loss from the data sheet.
$V_{CE,\ Data}$: The test voltage of E_{on} and E_{off}.
$I_{C,\ Data}$: The test current of E_{on} and E_{off}.

reduced. However, the losses caused by the non-ideal characteristics of the switches, the non-ideal resistances of the inductors and the capacitors and the conduction losses of the switches and the diodes still affect the conversion efficiency.

4 PFC control schemes and the experimental results

To achieve the goals claimed by this paper, a commercial PFC control IC, UC3854, was deployed as the controller. This popular PFC IC is designed to implement the average-current control. Moreover, an auxiliary digital circuit was designed to modify the PWM signal generated from this IC for providing suitable switching patterns to both the main and the auxiliary switches, in order to

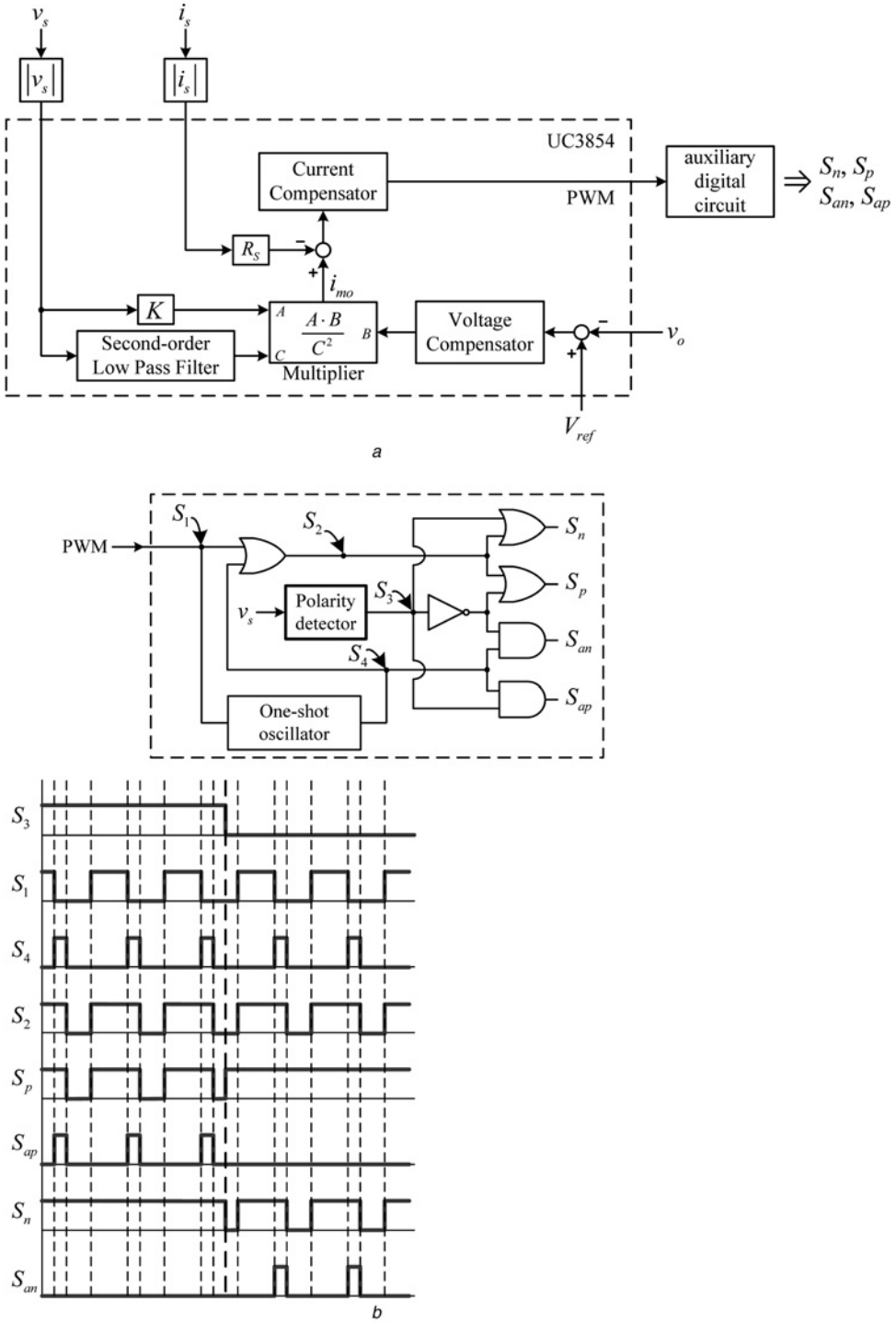

Fig. 5 *Control scheme, auxiliary digital circuit and timing chart of the relative switching signals*

a Control scheme of the proposed converter
b Auxiliary digital circuit
c Timing chart of the switching signals related to the digital circuit

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provide a soft-switching functionality. Fig. 5*a* shows the control scheme of the proposed converter, including the function of the UC3854 as shown in the dashed line. The line voltage and the current signals are rectified by two absolute-value circuits, then fed into the UC3854. To implement the soft-switching mechanism, an auxiliary digital circuit consisting of a few logical gates, a one-shot oscillator, and a line polarity detector as shown in Fig. 5*b*, adopts the pulse-width modulation (PWM) signal from the UC3854 and generates a suitable switching signals to the main and the auxiliary switches. The on-time state of the one-shot oscillator was set to be 1 μs according to (21). Fig 5*c* presents the timing chart for this auxiliary circuit's related signals.

A 1200 V/500 W prototype was built for testing, measurement and evaluation; Table 2 summarises the system specifications. According to the design considerations, the key components and the values of the passive elements were chosen and calculated as shown in Table 3. Fig. 6*a* shows the experimental waveforms of the output voltage, the line voltage and the line current at full load. In Fig. 6*a*, the dc output voltage is regulated at 1200 V with some ripple; the line current is nearly sinusoidal and inphase with the line voltage. To investigate the soft-switching performance, the waveforms of the resonant elements, the switching waveforms of S_p and S_{ap} in the marked point P are shown in Figs. 6*b–d*, respectively. At the point P, the phase angle is about 80° and the instantaneous voltage is about 153 V. Fig. 6*b* shows the waveforms of the inductor current and the capacitor voltage accompanied by the switching signal of the S_{ap}, Fig. 6*c* shows the waveforms of the voltage and the current of the S_p accompanied by the switching signal of the S_p, and Fig. 6*d* shows the waveforms of the voltage and the current of the S_{ap} accompanied by the switching signal of the S_{ap}. The on-state durations of the S_{ap} and the S_p in Figs. 6*b* and *c* are 1.1 μs (1 μs) and 3.9 μs (3.8 μs), respectively, which are very close to the theoretical values in the parentheses. Moreover, compared with Fig. 4, these experimental waveforms agree well with their theoretical counterparts. From Fig. 6*c*, the S_p is turned on softly and turned off with the ZCS by the resonant path made by the body diode of the S_p. On the other hand, the S_{ap} is turned on softly and

Table 2 System specifications of the prototype

Output power, P_o	500 W
Output voltage, v_o	1200 V
Line voltage, v_s	110 Vrms
Source frequency, f_s	60 Hz
Switching frequency, f_{sw}	60 kHz
DCVM Stage number, $N/2$	3

Table 3 List of the components

Component description	Symbol	Value/part no.
PFC control IC		UC3854
boost inductor	L_S	1.5 mH
bidirectional switch	S_p, S_n	IXGH30N60C3D1/600 V/30 A
capacitors	C_1–C_6	1000 μF/420 V
diodes	D_1–D_6	LTTH1506D/600 V/15 A
auxiliary switches	S_{ap}, S_{an}	IXGH50N60C4/600 V/30 A
resonant inductor	L_r	3.4 μH
resonant capacitors	C_{pr}, C_{nr}	15 nF/630 V
auxiliary diodes	D_{ap}, D_{an}	DSEP30-06A/600 V/30 A

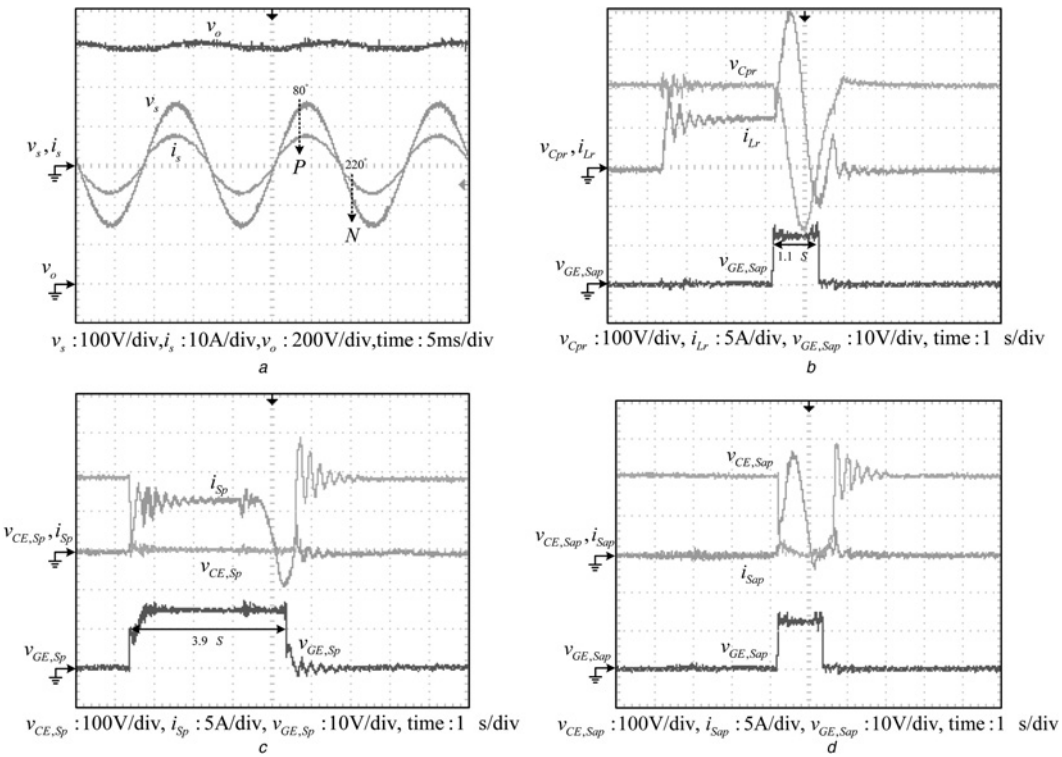

Fig. 6 *Experimental measured waveforms*

a Line voltage, line current and output voltage
b Waveforms of i_{Lr}, v_{Cpr} and $v_{GE,\ Sap}$ within the marked area
c Waveforms of i_{Sp}, $v_{CE,\ Sp}$ and $v_{GE,\ Sp}$ within the marked area
d Waveforms of i_{Sap}, $v_{CE,\ Sap}$ and $v_{GE,\ Sap}$ within the marked area

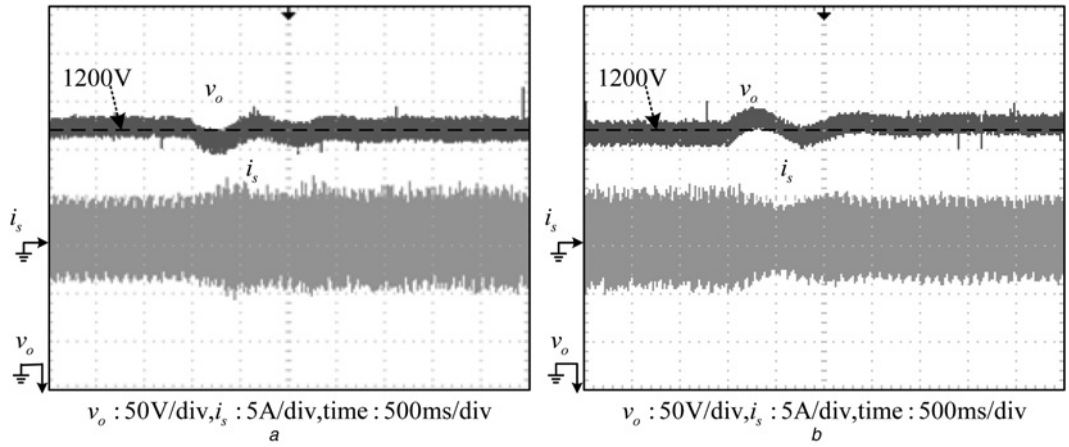

Fig. 7 *Measured transient responses of the load disturbance*

a Transient waveforms of v_o and i_s with the load changing from 300 to 381 W
b Transient waveforms of v_o and i_s with the load changing from 381 to 300 W

turned off with the ZCS by the resonant path made by the auxiliary diode of the D_{ap}.

It is important to note that the PWM and the soft-switching techniques used in this paper are related to the boost-type PFC function for improving the line condition of the ac source and the system efficiency. Thus, these techniques cannot mitigate the voltage dip caused by the load changing or the reduced capacitor size, because the DCVM is still energised based on the line frequency. Figs. 7*a* and *b* show the two measured transient responses of the load changing between 300 and 381 W, respectively. The voltage dip (overshoot) is about 2.5% and lasts about one second; nevertheless, the controller compensated for the dip, by bringing the output voltage back to its normal value (1200 Vdc).

For a comparison, the efficiency of the proposed converter operating with and without the soft switching was measured over the whole load range, as shown in Fig. 8*a*; the power consumptions in the IGBTs' gate circuits were not included in the measurement. It can be seen that the proposed converter's efficiency is about 2% higher when the soft-switching function is active over the whole load range. Fig. 8*b* shows the peak-to-peak ripple voltage and the ripple factor of the dc output, and both of them increase with the load. Under a full-load, the peak-to-peak ripple and the ripple factor are 32 V and 1.01%, respectively, and the measured power factor, the total harmonic distortion of the line current and the system efficiency are 99.6, 4.86 and 94%, respectively.

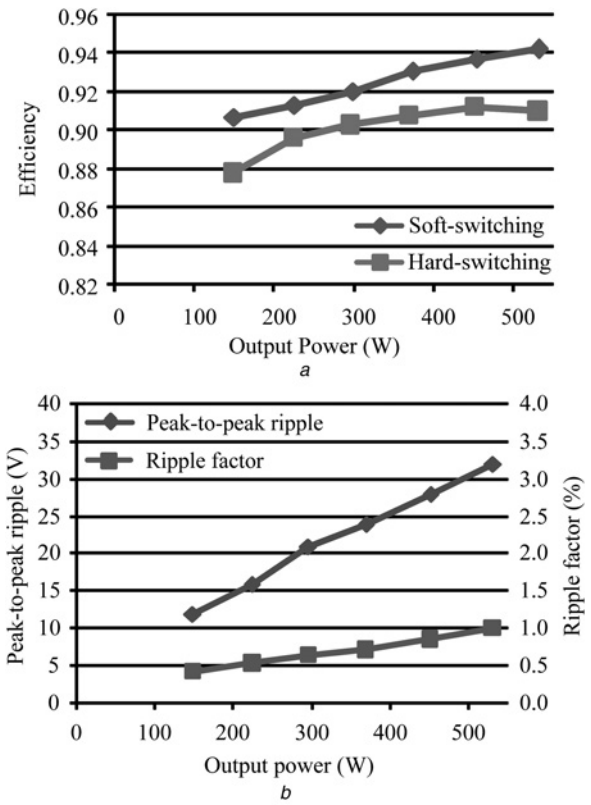

Fig. 8 *Experimental results under different load conditions*

a Efficiency
b Peak-to-peak ripple voltage and ripple factor

5 Conclusions

This paper proposed a soft-switching, high step-up ac–dc converter based on a conventional voltage multiplier with a PFC. A soft-switching circuit adopted from a boost-type dc–dc soft-switching converter was modified and added to the main power stage of the proposed converter to achieve a soft commutation. The operational principle of the proposed converter including the soft-switching behaviour was analysed theoretically, and the appropriate design considerations were investigated. A popular commercial IC was deployed in the proposed converter to implement the PFC and regulate the dc output. Moreover, an auxiliary digital circuit was designed to modify the PWM signal generated from the PFC IC, in order to provide suitable switching patterns for both the main and the auxiliary switches and achieve a soft-switching functionality. A 1.2 kV/500 W laboratory prototype controlled by the PFC IC was built for testing, measurement and evaluation. The measured waveforms of the prototype's major components agreed well with the theoretical counterparts, proving the correct design of the proposed scheme. Finally, from the experimental results, the proposed converter provided a 2% higher efficiency than the previous topographies without a soft-switching mechanism.

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