Saber Simulation and Experimental Study on Single-Phase Power Factor Correction Circuit

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***Abstract*—In order to solve the problem of serious harmonic pollution and power factor decline caused by uncontrolled rectification of the power electronic devices, an active power factor correction method based on UC3854 chip is proposed. The simulation model on the Saber software simulation platform is set up. Simulation results show that the power factor reaches more than 0.99. The system hardware circuit is constructed and the experimental results are basically the same as those of the simulation. Moreover the rationality and superiority of the circuit are verified.**

Keywords—APFC; UC3854; Saber simulation

I. INTRODUCTION

With the widespread use of the power electronic devices in many areas of development, the power grid harmonics and power factor problems have increasingly become prominent. As in the UPS (Uninterrupted Power Supply) system, whether for battery charging or providing DC power for inverter after the rectification, the rectifier links are essential. But the traditional rectifier using diode or thyristor as the rectifying device generates harmonic current which endanger the power grid. On one hand, the harmonic current causes the input power factor decline, on the other hand, it will affect the normal work of the load and even damage the electrical equipment[1,2]. Therefore, the power factor correction for power electronic equipment is imperative.

The function of APFC (Active Power Factor Correction) circuit uses a variety of control methods to modulate the phase of input current and input voltage into a consistent. The input current tracks voltage, which achieves the target power factor is 1 or close to 1[3,4].

This paper conducts the overall design of Boost APFC circuit. Then based on the design current, the circuit simulation on saber simulation platform is carried out. After the specific parameters are established through simulation. The physical structure is set up.

II. WORKING PRINCIPLE OF AVERAGE CURRENT CONTROL

From the definition of power factor, improving the power factor has mainly the following two ways. One is to make the input current sinusoidal as much as possible to reduce the current distortion factor, that is $I_1 = I_{rms}$ (harmonic is zero); the other is to make the input voltage and current in-phase as far as possible to reduce the displacement factor, that is $\cos\theta = 1$. Thus power factor correction is realized excellently. Aiming at the method of improving the power factor, this paper designs the power factor correction circuit using the average current control model. The schematic diagram is shown in Fig. 1. In this kind of APFC control method, it adopts double loop control which includes current control loop and voltage control loop. The current control loop makes input current closer to sine wave, and the voltage control loop makes output voltage of Boost circuit more stable[5,6].

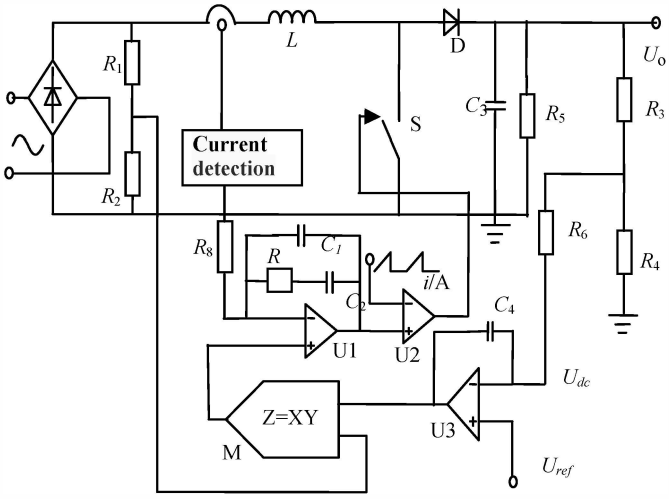


Fig. 1. Average current control circuit of Boost-type APFC

After comparing with the benchmark reference voltage U_{ref}, the main circuit output voltage U_{dc} is supplied to the voltage error amplifier U3, which output voltage signal and the detection value of the rectification voltage are provided into the input terminal of the multiplier M. The output of multiplier M is conducted as the reference signal of current feedback control. After comparing with the detection value of the switch current, add the output of multiplier M to PWM comparator through the current error amplifier U1, which generates PWM pulse signal to drive the transistor S conduction and shutting off. Therefore, the input current waveform and the input voltage waveform are basically the same, which makes the current harmonic components greatly reduced and improves the circuit power factor.

III. APFC CIRCUIT DESIGN

The overall design diagram of Boost APFC circuit is shown in Fig. 2. It selects UC3854 as the control chip, which adopts an average current mode control method inside. In main circuit, V_{in} is input AC voltage, D_1-D_4 are 4 rectifier diodes, C_1 is filter capacitance, L is boost inductance, T is power switch tube, and C_2 is output capacitance. The drive signal duty cycle of control circuit is determined by DC output voltage of pin 11, network voltage waveform of pin 6, network current waveform of pin 4 and network voltage effective value of pin 8. The corresponding protection circuit has startup delay of pin 10, soft-start of pin 13, and the maximum current limit on MOSFET of pin 2. Meanwhile, R_{VF} and C_{VF} constitute a group of RC compensating network, and R_{cz}, C_{cz}, C_{cp} compose another group of RC compensating network. The two groups of RC compensating network adjust the voltage and current waveform respectively. D_7 selects Schottky diode IN5820 to protect the circuit, and limit the low voltage to -0.4V.

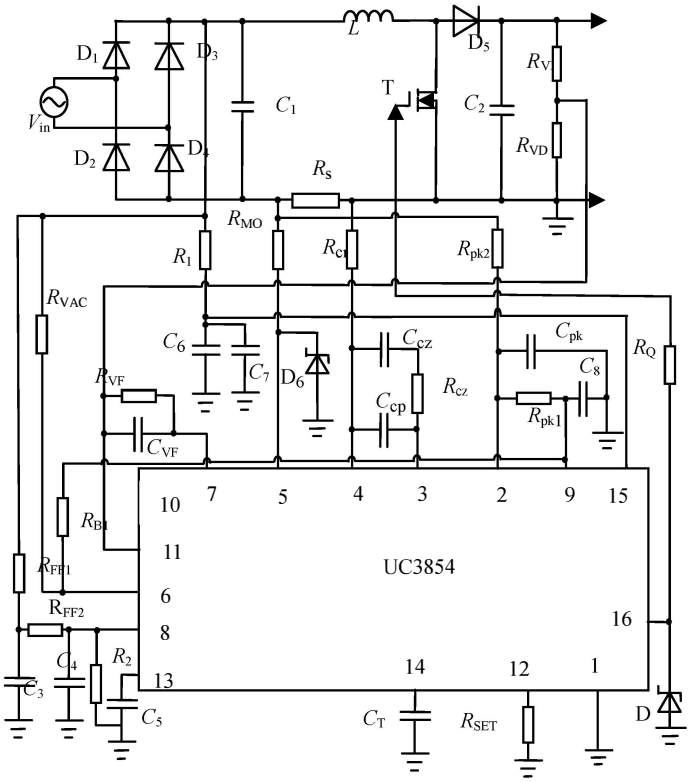


Fig. 2. APFC circuit

IV. SIMULATION AND EXPERIMENTAL RESULT ANALYSIS

A. Saber Simulation of APFC Circuit

TABLE I. SIMULATION PARAMETER

Simulation Parameters	
***Output DC voltage*(V)**	400
***Boost inductor*(mH)**	1
***Input filter capacitor*(uF)**	450
***VCC terminal voltage*(V)**	20

This paper uses Saber simulation tools to simulate the design circuit, which correctness is verified. The initial value of each parameter of the main circuit and the control circuit is obtained, which lays the foundation for practical system design[7]. Table I shows major parameters of the system.

The simulation waveforms are shown in Fig. 3.

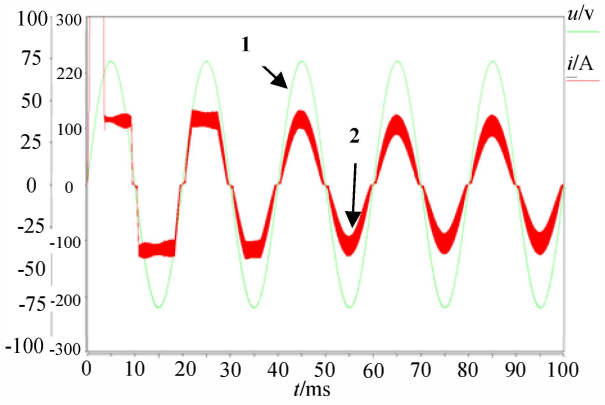


Fig. 3. Saber simulation waveforms of APFC circuit

In Fig. 3, curve 1 is the input voltage waveform, and curve 2 is the input current waveform. It can be see that the current waveform tracks the voltage waveform excellently after a cycle, thereby the goal of power factor correction is achieved. The total harmonic distortion is measured as THD=0.0919(ten times harmonic, fundamental frequency 50 Hz), and PF = 0.9915 is calculated by power factor calculation formula. The power factor reaches more than 0.99, which implies the impressive effect. Fig. 4 is the output voltage waveform diagram. The output voltage can rise up to 400V stably and the fluctuation voltage is small, which provides a good DC voltage source for the subsequent stage inverter circuit.

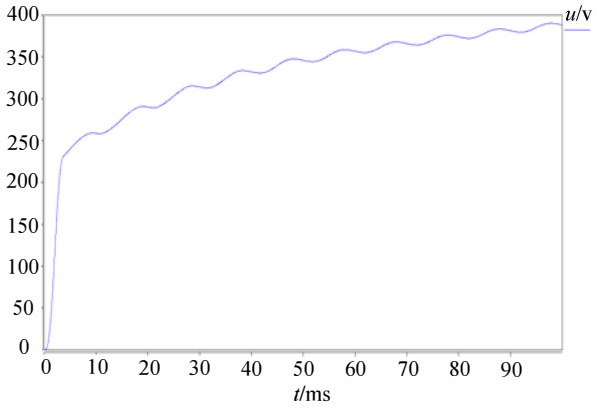
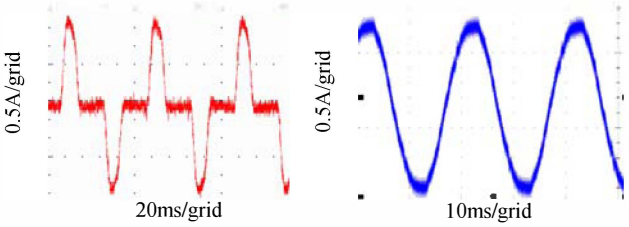


Fig. 4. Output curve of voltage waveform

The simulation results show that after adding the power factor correction circuit, the input current and the input voltage are modulated into in-phase and the size is proportional, so that it can achieve the anticipated target of the power factor as 1 in ideal conditions.

B. *Analysis on Simulation Results*

Through the simulation on Saber software platform, the specific parameters of the circuit are determined. On the basis of simulation, the APFC hardware circuit is set up with UC3854 chip. The input current waveforms before and after adding UC3854 are measured by the oscilloscope. The waveforms are shown in Fig. 5.



(a) Before correction (b) After correction

Fig. 5. Input current waveform

Before adding the power factor correction, the current distortion is serious and harmonic amount is large. After the UC3854 power factor correction, the input current waveform is basically sinusoidal and achieves the ideal standard. The experimental results and the simulation results are basically identical.

V. CONCLUSIONS

In this paper the Saber simulation model is established on the basis of the theory analysis and the satisfactory simulation results are obtained. At the same time, the Boost APFC circuit is set up with the UC3854 chip on the basis of the simulation. The experimental results verify that the APFC circuit is entirely feasible, the input current tracks the input voltage excellently, the THD of input current is far lower than the specified standard value in steady state, and the power factor is close to 1. Meanwhile, the circuit is simple and stable, which can be applied to different circuits with relatively high use value.

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