Design of Single Stage LED Driver

Li Qiang, Li Lei, Lv Guangqiang School of Automation Nanjing University of Science and Technology

Nanjing, China chnliqiang@163.cm

Abstract—The principle and design procedures of single stage PFC LED driver based on L6562 are discussed in this paper. Then the design of transformer and feedback loop are described in detail. The specification and experimental results are proposed at last.

Keywords- LED Driver; L6562; Single stage PFC; constant current:

I. INTRODUCTION

As a new green light source, lighting products of LED attract the world's attention and will play a chief role in lighting industry. But the power electronic devices in LED drivers are connected with AC mains by rectifiers, and current in these systems is interrupted by a switching action, the current contains frequency components that are multiples of the power system frequency, so the power factor of devices is very low.

In an electric power system, a load with a low power factor draws more current than a load with a high power factor for the same amount of useful power transferred. The higher currents increase the energy lost in the distribution system, and require larger wires and other equipment. Because of the costs of larger equipment and wasted energy, electrical utilities will usually charge a higher cost to industrial or commercial customers where there is a low power factor.

Usually, two stage PFC technology is used to reduce input current harmonics, but unfit for low power applications because of its high cost and complexity. The compromise between cost and performance should be considered. The single stage PFC technology is focused on by lots of researchers and electrical engineers, and most work and research is discussed about this technology in this paper.

II. PRINCIPLE AND DESIGN OF THE DRIVER

A. The overall structure and control mechanism

Actually, the single stage LED driver based on L6562 is a flyback converter consists of a EMI filter, a rectifier circuit, a control circuit, a flyaback transformer, a output filter circuit and a feedback circuit.

The structure of the driver is shown in figure 1:

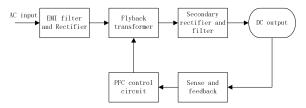


Figure 1. The overall structure

The input instantaneous line voltage is $Vs(t)=Vm \cdot \sin \omega t$, so the primary peak current is

$$i_{pk(t)} = \frac{V_{s(t)} \cdot T_{on}}{L} = \frac{V_m \cdot T_{on}}{L} \sin \omega t$$
 (1)

It is easy to know that the peak inductor current will be enveloped by a rectified sinusoid if the on-time is kept constant over each line half-cycle. Thus power factor correction can be achieved. The current waveforms and MOSFET timing are shown in figure 2.

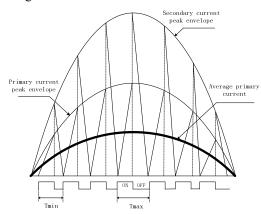


Figure 2. The current waveforms and MOSFET timing

B. Input circuit

The input circuit consists of a EMI filter, a rectifier and a filter capacitor. There are two input terminals, two output terminals and a earth terminal in the EMI filter. The EMI filter consists of a common mode choke Lc and four filter capacitors C1~C4. C1 and C2 are X-Cap, to filter the series mode interference. C3 and C4 are Y-Cap, connected between the two output terminals of the EMI filter, to suppress the common mode interference.

The input circuit is shown in figure 3:

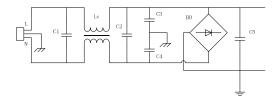


Figure 3. The input circuit

C. The control circuit

The control circuit is shown in figure 4:

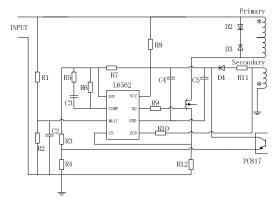


Figure 4. The control circuit

With the resistance divider (R1,R2), a partition of the instantaneous rectified line voltage is sent into the multiplier of the IC, then multiplied by the output of the E/A. The output of the multiplier is the reference signal for the current comparator, which sets the MOSFET peak current cycle by cycle.

The voltage across the current sense resistor (R12) is sensed by the current comparator and, by comparing it with the programming signal delivered by the multiplier, determines the exact time when the external MOSFET is to be switched off.

The Zero Current Detection(ZCD) block detects the demagnetization of the transformer and switches on the external MOSFET as the voltage across the auxiliary winding reverses, just after the current through the auxiliary winding has gone to zero.

D. Transformer design

It is assumed that the line voltage is perfectly sinusoidal and the rectifier bridge is ideal, thus the voltage downstream the bridge is a rectified sinusoid

$$V_{in}(t) = V_{PK} \cdot |\sin 2 \cdot \pi \cdot f \cdot t|, \qquad (2)$$

where f is the line frequency, V_{PK} is equal to the RMS line voltage times the square root of 2. Define $\theta = 2 \cdot \pi \cdot f \cdot t$, so the primary peak current is

$$I_{PKp}(\theta) = I_{PKp} \cdot |\sin \theta|. \tag{3}$$

The ON-time of the power switch is expressed by:

$$T_{on} = \frac{L_p \cdot I_{pkp}(\theta)}{V_{in}(\theta)} = \frac{L_p \cdot I_{pkp}}{V_{PK}},$$
(4)

where Lp is the inductance of transformer's primary winding. The OFF-time is instead variable:

$$T_{OFF} = \frac{L_{sI_{PKS}}(\theta)}{V_{O} + V_{F}} = \frac{\frac{L_{P}}{n^{2}} \cdot n \cdot I_{PKP} |\sin(\theta)|}{V_{O} + V_{F}} = \frac{L_{P} \cdot I_{PKP} |\sin(\theta)|}{n(V_{O} + V_{F})},$$
 (5)

where Ls is the inductance of the secondary winding, $Ipks(\theta)$ is the peak secondary current, Vo is the output voltage of the converter (supposed to be a regulated DC value) and Vf is the forward drop on the output catch diode. Therefore, the duty cycle will vary with the instantaneous line voltage

$$D = \frac{T_{ON}}{T} = \frac{1}{1 + \frac{V_{PK}}{V_R} \cdot \left| \sin(\theta) \right|}.$$
 (6)

The ratio between the line peak voltage Vpk and the reflected voltage Vr will be indicated with Kv. So the average value of input current is

$$I_{in}(\theta) = \frac{1}{2} \cdot I_{PKp}(\theta) \cdot D = \frac{1}{2} \cdot I_{PKp} \cdot \frac{|\sin \theta|}{1 + K_V \cdot |\sin \theta|}. \tag{7}$$

The total input power is

$$P_{in} = \overline{V_{in}(\theta) \cdot I_{in}(\theta)} = \frac{1}{2} \cdot V_{PK} \cdot I_{PK\rho} \cdot \frac{\sin^2(\theta)}{1 + K_V \cdot \sin(\theta)}.$$
 (8)

It is necessary to introduce the following function:

$$f(x) = \frac{\sin^2(\theta)}{1 + x \cdot \sin(\theta)} = \frac{1}{\pi} \cdot \int_0^{\pi} \frac{\sin^2(\theta)}{1 + x \cdot \sin(\theta)} d\theta \approx \frac{0.5 + 1.4 \times 10^{-3} x}{1 + 0.815 x}$$
(9)

From equation (8) and (9), it is possible to calculate Ipkp

$$I_{PKp} = \frac{2 \cdot P_{in}}{V_{PK} \cdot f(K_V)}$$
 (10)

The total RMS value of the primary current is

$$I_{\text{RMSp}} = \sqrt{\frac{1}{3} \cdot \overline{I^2_{\text{PKp}}(\boldsymbol{\theta}) \cdot D}} = I_{\text{PKp}} \cdot \sqrt{\frac{1}{3} \cdot \frac{\sin^2(\boldsymbol{\theta})}{1 + K_V \cdot \sin(\boldsymbol{\theta})}} = I_{\text{PKp}} \cdot \sqrt{\frac{f(K_V)}{3}} . \tag{11}$$

The average value of the current on the secondary side is

$$I_o(\theta) = \frac{1}{2} \cdot I_{PKs}(\theta) \cdot (1 - D) = \frac{1}{2} \cdot I_{PKs} \cdot K_V \cdot \frac{\sin^2(\theta)}{1 + K_V \cdot \sin(\theta)}. \tag{12}$$

So the peak secondary current is

$$I_{PKs} = \frac{2 \cdot \overline{I_o}}{K_V \cdot f(K_V)} \cdot \tag{13}$$

It is necessary to introduce the following function:

$$g(x) = \frac{\sin^{3}(\theta)}{1 + x \cdot \sin(\theta)} = \frac{1}{\pi} \cdot \int_{0}^{\pi} \frac{\sin^{3}(\theta)}{1 + x \cdot \sin(\theta)} d\theta \approx \frac{0.424 + 5.7 \times 10^{-4} x}{1 + 0.862 x}$$
(14)

The total RMS secondary current is calculated as follows:

$$I_{RMSS} = \sqrt{\frac{1}{3} \cdot \overline{I^2_{PKS}(\theta) \cdot (1-D)}} = I_{PKS} \cdot \sqrt{\frac{K_V}{3} \cdot \frac{\overline{\sin^3(\theta)}}{1 + K_V \cdot \sin(\theta)}} = I_{PKS} \cdot \sqrt{\frac{K_V}{3} \cdot g(K_V)}$$
(15)

Design index:

Universal mains voltage range is $88{\sim}264V$, the DC output voltage is 25V and output current is 0.7A. The expected efficiency is about 85%. The reflected voltage is selected 100V, the minimum switching frequency is selected at $25kHz_{\circ}$

Obviously, the output power is $Po=Vo\times Io=25\times0.7=17.5W$. Thus, the input power is $Pin=Po/\eta=17.5/0.85=20.6W$. The minimum input peak voltage is $Vpkmin=1.414\times88-4=120V$. The peak-to-reflected voltage ratio is Kv=Vpkmin/Vr=1.2. Therefore, f(1.2)=0.254, g(1.2)=0.209.

The primary current

The primary peak current is

$$I_{PKp} = \frac{2 \cdot P_{in}}{V_{PK \text{ min}} \cdot F_1(K_V)} = \frac{2 \times 20.6}{120 \times 0.254} = 1.35 A$$
 (16)

The RMS primary current is

$$I_{RMSp} = I_{PKp} \cdot \sqrt{\frac{F_1(K_V)}{3}} = 1.35\sqrt{\frac{0.254}{3}} = 0.393A$$
 (17)

The secondary current

The secondary peak current is:

$$I_{PKs} = \frac{2 \cdot I_{out}}{K_V \cdot F_1(K_V)} = \frac{2 \times 0.7}{1.2 \times 0.254} = 4.59 A$$
 (18)

The RMS secondary current is:

$$I_{RMSs} = I_{PKs} \cdot \sqrt{K_V \cdot \frac{F_2(K_V)}{3}} = 4.59 \sqrt{1.2 \times \frac{0.209}{3}} = 1.33A$$
 (19)

• The primary inductance

$$L_{\rho} = \frac{V_{PK \text{ min}}}{(1+K_{V}) \cdot f_{\text{sw min}} \cdot I_{PK\rho}} = \frac{120}{(1+1.2) \times 25 \times 10^{3} \times 1.35} = 1.616 mH$$
 (20)

• Turns of the transformer

Turns ratio is:

$$n = \frac{N_p}{N_s} = \frac{V_R}{V_{out} + V_f} = \frac{100}{25.7} = 3.89$$
 (21)

The primary turns of the transformer:

$$N_{\rm P} = \frac{V_{\rm pk(nin)} \times T_{\rm on(max)}}{B_{\rm m} \times A_{\rm c}} = \frac{90 \times 1.414 \times 0.53 \times 10^{-5}}{0.15 \times 40 \times 10^{-6}} \approx 112 \tag{22}$$

The secondary turns:

$$N_s = \frac{N_p}{n} = \frac{120}{3.89} \approx 29$$
 (23)

The auxiliary turns:

$$N_a = \frac{V_a}{V_s + V_f} N_s = \frac{15}{25.7} \times 29 \approx 17$$
 (24)

As a consequence, the primary inductance is 1.6mH, the primary turns are 112, so the secondary turns are 29, and the auxiliary turns are 17.

III. FEEDBACK CONTROL LOOP

The output circuit consists of a rectifier, a filter capacitor and a π -filter which is not the key point in this paper, while the design of the feedback loop will be mainly discussed.

The feedback control loop consists of a TL431, a LM368 and many other components. The TL431 is a three-terminal adjustable shunt regulator with specified thermal stability. The LM358 consists of two independent, high gain, internally frequency compensated which were designed specifically to operate from a single power supply over a wide range of voltages.

A. Current control loop

R1 is the output current sense resistor where the voltage drop is $R1 \times Iout$. This voltage signal is sent to the noninverting input terminal of the amplifier A1. Meanwhile, a partition of the 2.5V reference voltage is sent to the inverting terminal by the resistance divider(R4,R5).

By comparing the two signals, the amplified error signal is sent out from pin 1 which is one of the two output terminals of the LM358. Then the current will go through D2, C4 and R11, changing the forward current of the optocoupler of PC817.

Therefore, current variation is processed by the control circuit of the primary side, the duty cycle will be decreased to keep the output current constant. C4 and R6 is the compensation components of the current control loop amplifier A1

The expected output current is Iout, so the reference voltage of the current control loop is $R1 \times Iout$. The relationship between R4 and R5 is calculated as follows:

$$R_1 \times I_{out} = \frac{R_5}{R_4 + R_5} \times 2.5V \tag{25}$$

Where, Iout=0.7A,R1= $0.22\,\Omega$, the value of R1 should be chosen less than hundreds of $m\Omega$ to reduce extra losses. As a result, R4=20R5. R4= $2.2K\,\Omega$,R5= $33K\,\Omega$ are proved to be practicable. Design of the compensation networks depends on practical situation in different applications.

Because the voltage drop across the emitting diode in the optocoupler is about 1V, and the forward current of the optocoupler is set as If=1mA, while the output of the amplifier is about 2.5V and the voltage drop across D2 is 0.5V, so the voltage drop across R11 is about 1V. Therefore, the value of R11 is: R11= Δ V/If=1K Ω .

B. Voltage control loop

The work principle of the voltage control loop is similar to that of current control loop, there's no need to discuss it again.

The reference voltage from TL431 is 2.5V, so the voltage across the resistor R9 is VR9 = (R8/R8+R9) \times Vout = 2.5V, and Vout=25V. By experiments, R8=2K Ω ,R9=18K Ω are proved to be practicable.

The value of capacitor C5 is 0, for the amplifier A2:

$$V_0 = V_{in} + \frac{R_{10}}{R_7} (V_{in} - 2.5)$$
 (26)

Where, Vin is the voltage of the inverting input terminal of the amplifier A2, Vo is the output voltage of A2. The value of R7 and R10 depends on practical situation in different applications.R7=3K $\,\Omega$,R10=68K $\,\Omega$ are proved to be practicable.

The gain of the current loop should be higher than that of the voltage loop to ensure the LED driver functioning well as a constant current source.

The output circuit and feedback control loop is shown in figure 5:

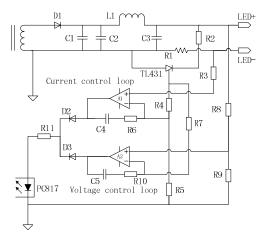


Figure 5. The output circuit and feedback loop

IV. EXPERIMENTAL RESULTS AND ANALYSIS

With the input voltage range of 88V~264V, the driver was tested in full load conditions(2 strings of LEDs and 8 LEDs in every string).

Waveforms of input voltage and current in condition of 220VAC input are shown in figure 6. The curve whose amplitude is higher is the waveform of input voltage, while the lower one is the waveform of input current, the time axis of the oscilloscope is 2milli second per grid.

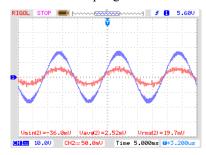


Figure 6. Waveforms of input voltage and current

Waveforms of output voltage and current in condition of 220VAC input are shown in figure 7, where the higher one is the waveform of output voltage and the lower one is the waveform of output current. From the picture, the current ripple is lower than 30% and the voltage ripple is lower than 5%, the time axis of the oscilloscope is 2milli second per grid.

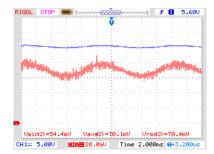


Figure 7. Waveforms of output voltage and current

Experiments demonstrate: Within the full voltage range, the output current of the driver is 0.7A±0.01A, output voltage is 25V±0.1V, the power factor is always higher than 0.95 and the efficiency is higher than 85%, all the parameters are satisfying and the performance are reliable. Therefore, this type of single stage PFC driver is suitable for LED lighting.

V. CONCLUSION

The single stage PFC LED driver based on L6562 consists of a EMI filter, a rectifier circuit, a control circuit, a flyaback transformer, a output filter circuit and a feedback circuit. The design procedure of the transformer and the feedback loop are mainly discussed in the paper. The experimental results and waveforms are given in the end. That simple structure, small size, high PF and high efficiency is the advantages of the single stage PFC driver.

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