

Mukti Barai  
Electrical Engineering Department  
NIT Calicut, India  
muktib@nitc.ac.in

compromise between good current quality and fast dynamic response, various methods have been proposed [2]-[5].

Fig.1. Conventional boost rectifier

Filters are used in the voltage loop to eliminate dominant low order harmonics from output voltage. This has been one of the attractive methods because of several advantages. The main purpose of the filter in the voltage loop is to eliminate the low frequency (2nd order) ripples from the regulator output before it is further processed. Various filters have been reported to eliminate the dominant second order harmonics. A notch filter [5], having notch frequency set at second-harmonic frequency reduces 2<sup>nd</sup> order ripples but higher order ripples are not reduced. The comb filter [6]-[7] with multiple notches for harmonics of second order and multiples has a complex analog implementation. The work presented in [8] is a simple digital implementation of a running average filter on FPGA. The filter placed after PI regulator eliminates the low frequency ripples which in turn reduces line current THD. This filter allows 2-3% of additional current distortion during line frequency variations as the clock has a fixed period which decides the averaging basis. The sliding mode

controller implemented by means of hysteretic controllers in[9] shows increase in THD with load.

In this paper a novel method is proposed to address the challenge of obtaining both low input current distortion and fast dynamic response at a common high bandwidth of the voltage loop. The proposed filter requires minimum additional circuitry in analog domain. Hence it has a simple analog and digital implementation which enables its application in various analog or digital control schemes. The work presented here proposes a simple RC low pass filter to be introduced as shown in Fig.3 in a voltage loop to filter out the harmonics from PI regulator output before it is further processed. The proposed methodology is implemented using UC3854 PFC controller [10]-[11].

Section II presents the working principle of voltage control loop with proposed filter. In section III the design of power and control stages of single phase boost rectifier are discussed. Section IV presents simulation and experimental results. Section V concludes the paper.

## II. PROPOSED CONTROL SCHEME

### A. Line current distortion

The output voltage of the boost PFC rectifier has ripples at twice the line frequency (100Hz) as the input which is described by Eq.(1). Therefore, output voltage consists of a constant dc part and varying quantity components. The output voltage is scaled down through a sensor and fed to the PI regulator. Even order ripples in this signal are responsible for the input current distortions because this signal is further processed to form a current reference. Conventionally, the bandwidth of the voltage loop is kept low (10-15Hz), in order obtain the low input current distortion [12]. But it is necessary to obtain a fast voltage loop response during transients which requires a high bandwidth of (45-50Hz).

$$v_{out} = \underbrace{v_o(t)}_{dc} + \underbrace{\frac{P_{out}}{2\omega C V_o} \sin(2\omega t)}_{varying} \quad (1)$$

### B. Proposed filter

The three main objectives of any ac-dc converter are high input power factor, low input current distortion and fast dynamic response. The output voltage of the rectifier contains harmonics at twice the line frequency and its odd multiples.

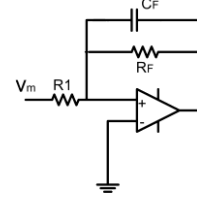


Fig.2. RC low pass filter

A simple RC low pass filter shown in Fig.2. is introduced after the PI regulator in the voltage feedback loop of the PWM boost rectifier system. In general, low pass RC filter blocks the frequency component range above the designed specific cutoff frequency. This indicates that harmonics at 2f and higher odd multiples of 2f components are effectively blocked by the filter. The cutoff frequency ( $f_c$ ) given by (2) is set at 2f/4 (10~20Hz) to eliminate second order ripples from regulator output.

$$f_c = \frac{1}{2\pi R_F C_F} \quad (2)$$

### C. Frequency domian analysis of voltage loop

The model of the voltage loop [13] with proposed scheme is as shown in Fig.3.

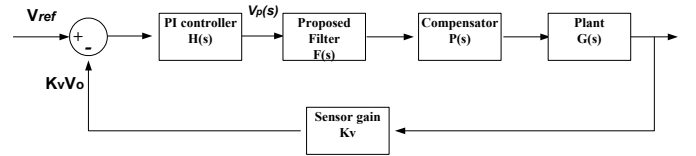


Fig.3. Voltage loop of proposed controller

$$G(s) = \frac{1}{2} \frac{V_s}{V_o} \frac{(R_o/2)}{1 + s(R_o/2)C_o} \quad (3)$$

$$H(s) = \frac{K_v}{1 + sT_v} \quad (4)$$

$$F(s) = \frac{K_f}{(1 + T_f s)} \quad (5)$$

$$P(s) = K_i \frac{(1 + T_c s)}{(1 + T_p s)} \quad (6)$$

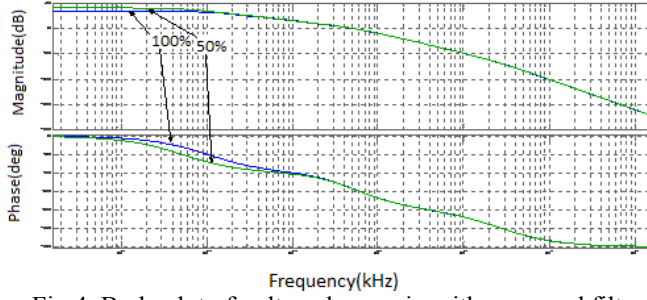


Fig.4. Bode plot of voltage loop gain with proposed filter

The Voltage loop parameters (3)-(6) play a significant role in limiting input current distortion. The frequency domain analysis of voltage loop of a converter is shown Fig.4. The bode plot is shown for 50% and 100% load and phase margins are  $53^\circ$  and  $54^\circ$  respectively. The filter transfer function is given by (4). The pole  $T_f$  is placed at 20Hz. In order to compensate for pole introduced by the filter in the voltage loop, a lead lag compensator (5) is designed. The compensator zero is placed at  $T_c = T_f$ , such that filter pole is cancelled and pole  $T_p$  is placed at high frequency.

#### D. Implementation

The proposed controller concept is designed and verified on MATLAB/SIMULINK software. The control scheme is tested and verified on 250W boost rectifier prototype. The block representation of proposed concept is shown in Fig.5.

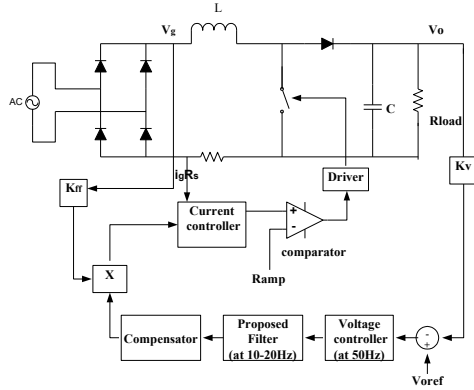


Fig.5. Proposed control scheme

The specifications of boost rectifier prototype are given in Table1.

The proposed control scheme is implemented using UC3854 PFC controller as shown in Fig.6. A series combination of PI regulator  $H(s)$ , filter  $F(s)$  and compensator  $P(s)$  is implemented externally and connected to current reference input (Pin7 of UC3854) of the multiplier [8][13].

TABLE I  
DESIGN PARAMETERS OF THE BOOST RECTIFIER

Parameter	Specification	Parameter	Specification
Output Power ( $P_o$ )	250W	Current sense gain ( $R_s$ )	0.25Ω
Load Voltage ( $V_o$ )	385V	Inductor (L)	8mH
Input Voltage ( $V_{in}$ ) RMS	85-265V	Output Capacitor ( $C_o$ )	470uF
Line frequency (f)	47-53Hz	Switch ( $S_1$ ) (MOSFET)	IRFP460
Switching frequency ( $f_s$ )	11kHz	Diode ( $D_1$ ) (Ultra fast)	MUR1660
Output voltage sensor gain ( $K_v$ )	0.02	Diode Bridge	DFB2060

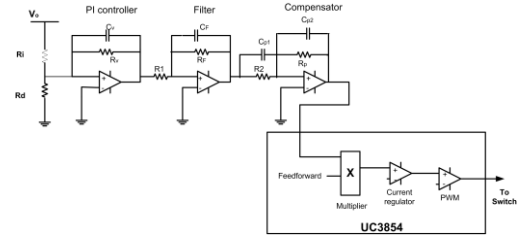
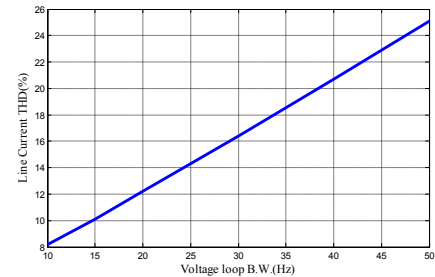


Fig.6. Implementation of filter with PI controller

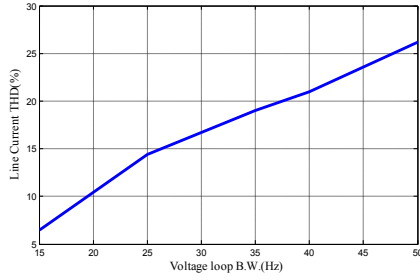
### III. EXPERIMENTAL RESULTS

#### A. Input Current Distortion

Fig.7. shows the variation of input current distortion with voltage loop bandwidth in conventional control method. The simulation and experimental results show that the line current THD(%) increases with the increase in voltage loop B.W. For voltage loop B.W. of 50Hz, the line current THD is 26.2%. The variations are recorded at the input voltage of 200  $V_{rms}$ .



(a)



(b)

Fig.7. Variation of % $I_{THD}$  with voltage loop B.W. using conventional control method  
(a) Simulated (b) Experimental

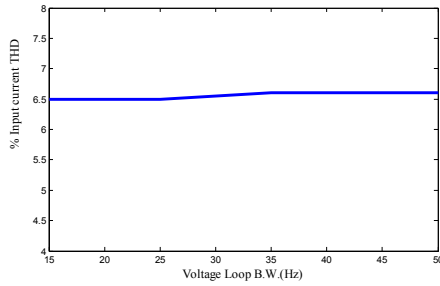


Fig.8. Variation of % $I_{THD}$  with Voltage loop B.W. with Proposed filter (Experimental)

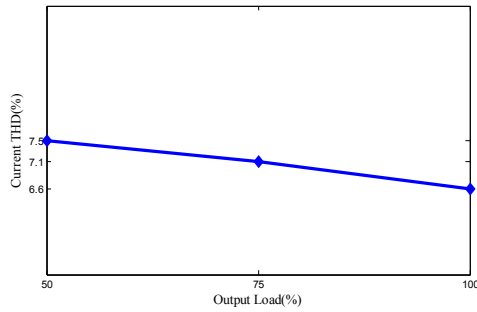


Fig.9. Current distortion at various load conditions with proposed control scheme (Experimental)

It is observed from experimental results shown in Fig.8. that the proposed control method keeps the line current distortion under 6.6% at feedback loop B.W. of 50Hz. Fig.9. illustrates that the current distortion remains under 7.5% when the load current is set at 50%, 75% and 100% of its full load value using proposed scheme.

### B. Power Factor

Fig.10. shows variation of Input Power factor with load. The p.f. remains close to unity at 50%, 75% and 100% of the full load.

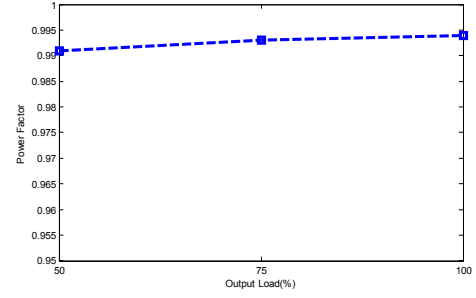
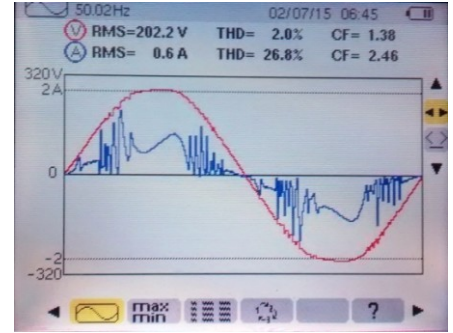
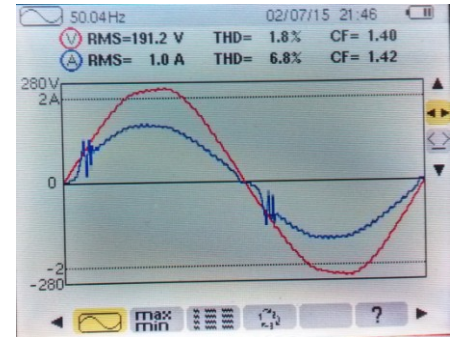


Fig.10. Power factor vs. Load

The line current and Line voltage waveforms for voltage loop B.W. of 50Hz are shown Fig.11 (a). and (b). The current quality in Fig11.(b) suggests that the line current THD is low and p.f. is high. Fig.12 shows Load voltage and line current waveforms at full load.



(a)



(b)

Fig.11. Line voltage and Line current waveforms at voltage loop B.W. =50Hz (a) Conventional controller  
(b) With proposed control

The Experimental setup is shown in Fig.13.

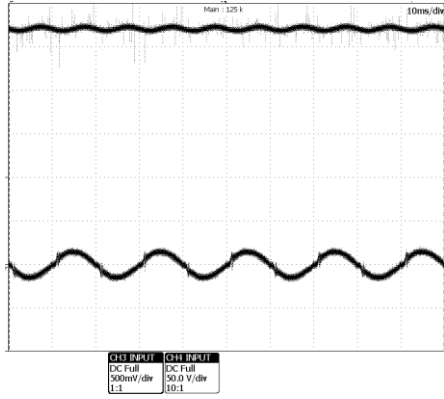


Fig.12. Output voltage and Input current at voltage loop B.W. = 50Hz with proposed control method



Fig.13. Experimental setup

#### IV. CONCLUSION

A simple, low cost method is proposed in this paper to improve input current quality of single phase boost rectifier. The boost rectifier with proposed control scheme shows significant reduction in current distortion. The RC filter is simplest in implementation in both analog and digital domain. The controller requires minimum additional circuitry. This method enables the rectifier to operate at higher bandwidth of voltage loop without any compromise between current distortion and dynamic response. The control scheme can be extended to NLC or PSM control [14][15] concepts which eliminate the use of input voltage sensor.

#### REFERENCES

- [1] IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems, IEEE std 519-1992, 1992.
- [2] Z. Lai and K. M. Smedley, "A family of continuous-conduction-mode power-factor-correction controllers based on the general pulse-width modulator," *IEEE Trans. Power Electron.*, vol. 13, no. 3, pp. 501–510, May 1998.
- [3] Liu, Xudan, et al. "A high-efficiency single-phase ac/dc converter with enabling window control and active input bridge." *IEEE Transactions on Power Electronics* 27.6 (2012): 2912-2924.

- [4] G. Spiazzi, P. Mattavelli, and L. Rossetto, "Methods to improve dynamic response of power factor preregulators: An overview," in *Proc. EPE*, 1995, vol. 3, pp. 754–759.
- [5] A. Prodic, J. Chen, R. W. Erickson, and D. Maksimovic, "Digitally controlled low-harmonic rectifier having fast dynamic responses," in *Proc. IEEE APEC*, Mar. 2002, vol. 1, pp. 476–482.
- [6] A. Prodic, J. Chen, D. Maksimovic, and R. W. Erickson, "Self-tuning digitally controlled low-harmonic rectifier having fast dynamic response," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 420–428, Jan. 2003.
- [7] A. Prodic, D. Maksimovic, and R. W. Erickson, "Dead-zone digital controllers for improved dynamic response of low harmonic rectifiers," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 173–181, Jan. 2006.
- [8] R. Ghosh and G. Narayanan, "A simple analog controller for singlephase half-bridge rectifier," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 186–198, Jan. 2007.
- [9] Adria Marcos-Pastor, Enric Vidal-Idiarte, Angel Cid-Pastor, and Luis Mart'inez-Salamero, "Loss-Free Resistor-Based Power Factor Correction Using a Semi-Bridgeless Boost Rectifier in Sliding-Mode Control," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5842–5853, Oct. 2015.
- [10] Philip P. Todd, "UC3854 Controlled Power Factor Correction Circuit Design," Unitrode Application Note-134
- [11] L. H. Dixon, "High Power Factor Preregulator for Off-Line Supplies," Unitrode Power Supply Design Seminar Manual SEM600, 1988
- [12] J. B. Williams, "Design of feedback loop in unity power factor AC to DC converter," in *Proc. IEEE-PESC*, Jun. 1989, vol. 2, pp. 959–967.
- [13] R. W. Erickson, *Fundamentals of Power Electronics*, 1st ed. New York: Chapman & Hall, May 1997.
- [14] D. Maksimovic, Y. Jang, and R. W. Erickson, "Nonlinear-carrier control for high-power-factor boost rectifiers," *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 578–584, Jul. 1996.
- [15] S. Chattopadhyay, V. Ramanarayanan, and V. Jayashankar, "Predictive switching modulator for current mode control of high power factor boost rectifier," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 114–123, Jan. 2003