Multistage Active-Clamp High Power Factor Rectifier with passive lossless current sharing

José Villarejo
Member, IEEE
Universidad P de Cartagena
Dpto de Tec Electronica
Cartagena, Spain
Jose.villarejo@upct.es

Esther de Jódar
Student, IEEE
Universidad P de Cartagena
Dpto de Tec Electronica
Cartagena, Spain
esther.jodar@upct.es

Fulgencio Soto
Asociated, IEEE
Universidad P de Cartagena
Dpto de Tec Electronica
Cartagena, Spain
Pencho.soto@upct.es

Miguel Moreno
Universidad de Murcia
Facultad de Informática
Dpto. de Inf y Sistemas
Murcia, Spain
mimoreno@um.es

***Abstract* – A new method to design active power-factor-corrector for high-power applications is introduced in this paper. It consist in using the high input impedance of Active Clamp boost converters in order to make easier the parallel connection of power stages. Experimental results are presented, taken form a three stages laboratory prototype rated at 0.35x3 kW, input ac voltage of 230Vrms, output voltage of 400V, and 120 kHz switching operation. Due to the simplicity of the current share technique, the control can be done using analog control based on the Unitrode's UC3854 strategy.**

***Index Terms*-- Boost converter, current sharing, paralleled converters, power factor correction, zero-voltage switching.**

I. INTRODUCTION

At higher power levels (1-3kW), the continuous-conduction-mode boost converter is the preferred topology for implementing a front end with power-factor correction (PFC). The main difficulty of this technique at high power levels are the switching losses increased due to the adverse effects of the reverse-recovery characteristic of the boost rectifier [1]. Reduction of reverse-recovery-related losses requires the boost rectifier to be "softly" switched off by controlling the turn-off rate of its current, so the converter design increases its complexity. Low and medium power converters (100-400W) have a big market so the design cost is not important in the final converter price. However, this cost is not negligible in high power converter with small market and more complex designs. Multistage converters could be a solution for both problems. A multistage converter allows a modular design to achieve high power levels from a "base" converter. Furthermore, small converters can be optimized from the point of view of components and layout. Nevertheless, there is a problem: power stages require current sharing among paralleled power channels.

The current sharing among the different converters could be done using a master-slave configuration with a current control loop for each converter or increasing the converter output impedance for a passive current share [2]. Including a current loop is relatively expensive because of the required electronic circuitry (sensors) and a more complex control.

Active-Clamp boost converter has interesting properties for this application: zero-voltage switching (ZVS) of the boost switch besides the soft switching of the boost rectifier, and high input impedance that can be used as a passive lossless current sharing method [3].

The Active-Clamp boost converter shown in Fig. 1.a was presented in [4] and used as PFC in [7]. However, in this work the converter design will be based on the developed average model, shown in Fig. 1.b and obtained following the method presented in [5]. Similar models have been presented in [6], but the effects of the clamp capacitor are not included. In this way, the design of the PFC is easier to analyze.

In order to simplify the current sharing analysis, the clamp capacitor will be neglected. Nevertheless, using the complete model, it can be proved that high clamp capacitor must be taken into account for the dynamic current share.

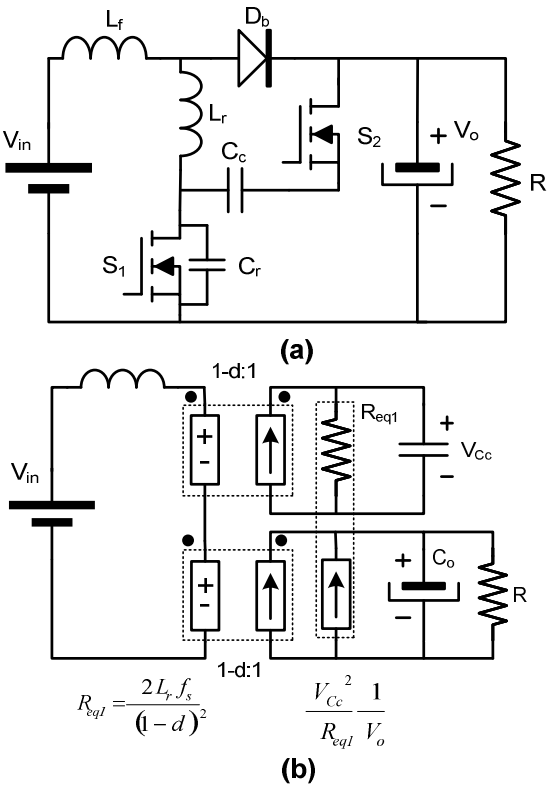

Fig. 1. (a)Boost with active-clamp (b) average model

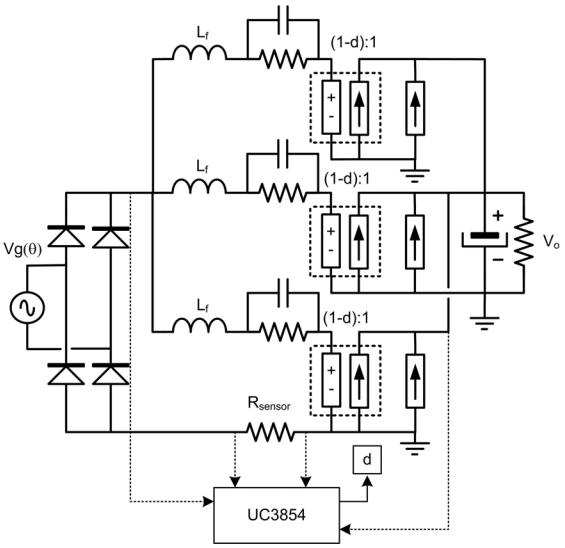

Fig. 2 Proposed solution k=3, with only one control circuit.

II. CURRENT SHARING

The desired modularity requires a simple method for paralleling. So, the simplest concept of paralleling power stages [2], where all the power stages are controlled by a single control loop and the duty cycle "d" is distributed for the main switches is the best option. As well, load sharing must be ensured without additional active methods so the converter impedance will be used as an "open loop droop method" where the load-dependent output voltage can be exploited for load sharing. Fig. 2 shows the proposed solution using the averaged circuit presented in Fig. 1.b.

In order to study the low frequency current share the clamp capacitor (C_c) and the filter inductor (L_f), designed to operate at high frequency, will be neglected assuming that theirs effects at low frequency are negligible. As would be shown in section 5, this is correct only in carefully designed converters.

The converters are connected in parallel so all of them have the same output voltage. In these conditions, the circuit shown in Fig. 3 could be used to study the current sharing. Due to the high output voltage the load share is very sensitive to duty cycle mismatch "Δd" introduced by driver and switches tolerances. This effect has been included in Fig. 3 that shows the worst case where phase "i" has the highest duty cycle and all other phases have the minimum duty cycle. In these conditions (1) can be derived to obtain the current mismatch as a function of the number of stages "k", the mismatch duty cycle "Δd" and the equivalent lossless resistance "R_{eq}" introduced by the averaged model (2).

$$\Delta I = I_i - \frac{I_{in}}{k} = \frac{k-1}{k}\frac{V_o \Delta d}{R_{eq}} \quad (1)$$

$$R_{eq} = 2L_r f_s \quad (2)$$

Now, using (1) and (2) together with the design conditions, the value of $L_r \cdot f_s$ can be calculated. A multiphase converter can be designed setting the maximum current deviation from nominal value due to a deviation in duty cycle. The lossless resistor (2) ensures, in the worst case, that current mismatch will not exceed the design limits. A three stage converter (k=3) with V_o=400V, a mismatch duty cycle Δd=0.01 (1%) and R_{eq}=14Ω will have a current mismatch ΔI=0.19A. Usually, the switching frequency is selected before the equalizing resistor calculation, so the resonant inductance L_r can easily be calculated.

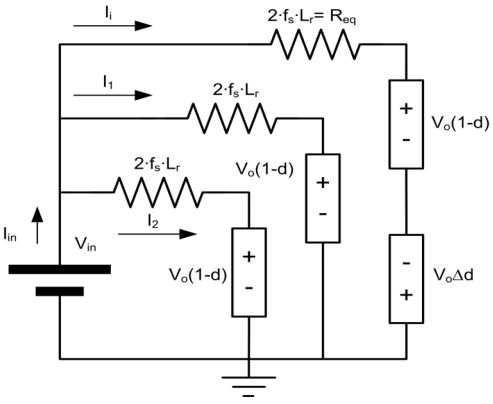

Fig. 3. DC model to analyze current sharing, k = 3

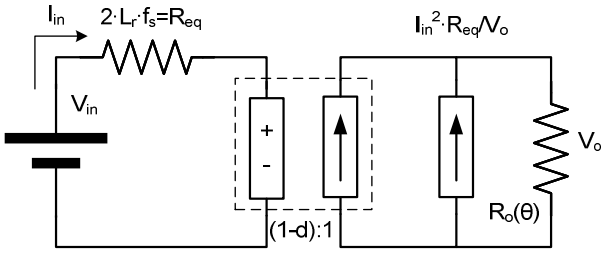

Fig. 4 Simplified DC model for PFC

III. ACTIVE CLAMP BOOST BEHAVIOUR IN HIGH POWER FACTOR RECTIFIER

In a switching cycle, the operation of the selected converter, in the AC/DC mode, is the same as in DC/DC mode, although it is necessary to advice that the converter will operate with a rectified sinusoidal input voltage and due to the bulk capacitor, in this application the output voltage "V_o" can be considered constant for an ac line half-cycle.

A. Duty Cycle

In order to obtain the duty cycle from the averaged model some simplifications have been done. In the DC averaged model shown in Fig. 4, inductors and capacitors have been removed. So, due to input power must be the same that output power for any instant of time, load "$R_o(\theta)$" must change according to input voltage as shows (3). Now from the averaged DC model the duty cycle can be derived as (4).

B. Clamp Voltage

Another important parameter to be calculated is the clamp capacitor voltage. This capacitor is parallel connected with the lossless equivalent resistance across a "DC" transformer with transfer ratio (1-d(ϴ)) so the clamp capacitor voltage can be calculated as the voltage across the equivalent resistance "R_{eq}" and the duty cycle dependent transfer ratio as shows (5). From (3), (4) and (5) clamp capacitor voltage can be simplified as (6). This is an important result: the clamp voltage is constant for an ac line half-cycle.

$$\frac{V_o^2}{R_o(\theta)} = V_{in}(\theta)\cdot I_{in}(\theta) \tag{3}$$

$$d(\theta) = 1 + \left(\frac{R_{eq}}{R_o(\theta)} - \left(\frac{V_{in}(\theta)}{V_o} \right)^2 \right) \frac{V_o}{V_{in}(\theta)} \tag{4}$$

$$V_c(\theta) = \frac{\sqrt{2} Ig_{rms} \left|\sin(\theta)\right| R_{eq}}{1 - d(\theta)} \tag{5}$$

$$V_c(\theta) = \frac{V_o}{\frac{Vg_{rms}^2}{R_{eq} P} - 1} \tag{6}$$

Where $V_{in}(\theta)$ and $I_{in}(\theta)$ can be expressed as

$$V_{in}(\theta) = Vg_{rms}\sqrt{2}\left|\sin(\theta)\right| \tag{7}$$

$$I_{in}(\theta) = Ig_{rms}\sqrt{2}\left|\sin(\theta)\right| \tag{8}$$

According to (6), where P is the rated power, this converter is not a good option for universal voltage range (85-265V). As shows Fig. 5, low input voltages will deliver high clamp voltages and so high switches stress. To use this solution in the universal voltage range switching frequency could be changed. At low input voltages there will be high input currents so input impedance could be reduced maintaining the current share among the power stages. Although differences among currents increase, relative values will not change. So, using lower frequencies for low input voltages the voltage stress is limited and the load share is not penalized.

C. Zero Voltage Switching

To ensure the ZVS operation the stored energy in L_r when S_2 is turn-off must be greater than the energy required to discharge C_r from V_o+V_{clamp} to 0. Considering neglected the input filter current ripple, the ZVS condition can be expressed as (9).

$$L_r I_{in}^2(\theta) > C_r (V_o + V_c)^2 \tag{9}$$

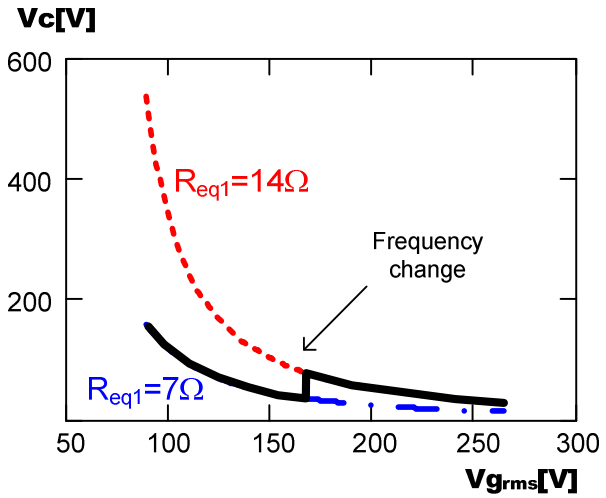

Fig. 5. Clamp capacitor voltage, frequency and input voltage dependence

Input filter current shape will follow the rectified input voltage, so there will be small current values that could not carry out with (9). Fig. 6 shows the percentage of power processed with ZVS as a function of input power calculated with the prototype characteristics for different input filter inductors. As can be seen, current ripple reduces the percentage of power processed with ZVS. So, efficiency is not as high as expected. For the design prototype (L_f=0.8mH) for loads higher than the 60% of rated load the power processed with ZVS is higher than 50%. Furthermore, in order to ensure the existence of ZVS a dead-time must be introduced between transistors control signals. This dead-time is not difficult to obtain thanks to clamp voltage (6) is not angle dependent. The maximum dead-time will be necessary at full load and minimum input voltage [4].

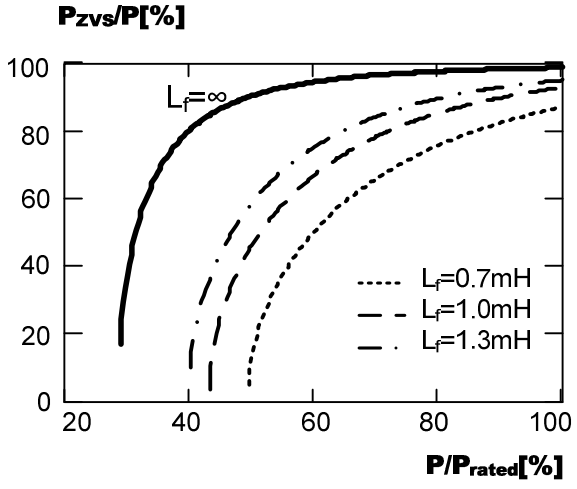

Fig. 6. Percentage of power processed with ZVS calculated with fs=100 kHz, Cr=0.16nF, Lr=70µH and different input inductors.

IV. Dynamic Current Share: Clamp Capacitor Influence

In order to analyze the clamp capacitor influence in the dynamic behavior of the converter the small-signal equivalent circuits shown in Fig. 7 have been obtained from the averaged model presented in Fig.1 b) In order to derive the impedance used as current equalizer, duty cycle variation "$\tilde{d}$" and input voltage variation "$\tilde{v}_{in}$" must be zero. Load transients will produce output voltage variations that will affect to all the power stages parallel connected. This behavior is represented in Fig. 8 changing the output capacitor and output load by a small signal output variation "$\tilde{v}_o$", after that, parallel connected elements (k_1, k_2, R') have no effect. Now, all the elements can be represented in the same side of the transformers in order to simplify the impedance representation. As shows Fig. 8, the converter impedance is a constant loss-free resistance in parallel with a duty cycle dependent capacitor with the filter inductance serial connected.

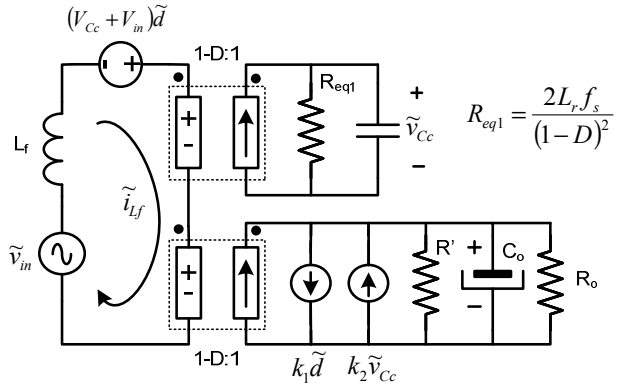

Fig. 7. ZVS boost small signal model. Small signal parameters are shown in Table I.

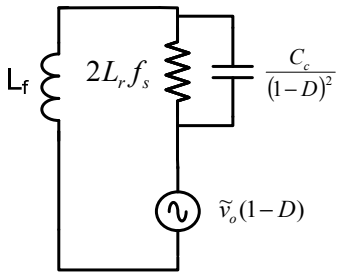

Fig. 8. Input impedance of ZVS boost converter.

Impedance evaluation will be done from the approximate Bode diagram. The magnitudes of the individual resistor, inductor, and capacitor asymptotes are plotted in Fig. 9. According to the corner frequencies f_1 and f_2 that can be calculated by (10) and (11), the impedance is dominated by the resistor at low frequency and by the inductor at high frequencies, as illustrated by the bold line in Fig. 9. This corner frequencies configuration gives to the converter high impedance for all frequencies and ensures good current balance for low and high frequency load transients.

TABLE I

Parameter	Value
k_1	$I_{Lf}+\frac{V_{Cc}^2}{V_o}\frac{(1-D)}{(L_rf_s)}$
k_2	$\frac{2I_{Lf}}{V_o}$
R'	$-\frac{V_{Cc}^2}{V_o^2}\frac{(1-D)^2}{(2L_rf_s)}$
R_{eq1}	$\frac{2L_rf_s}{(1-D)^2}$

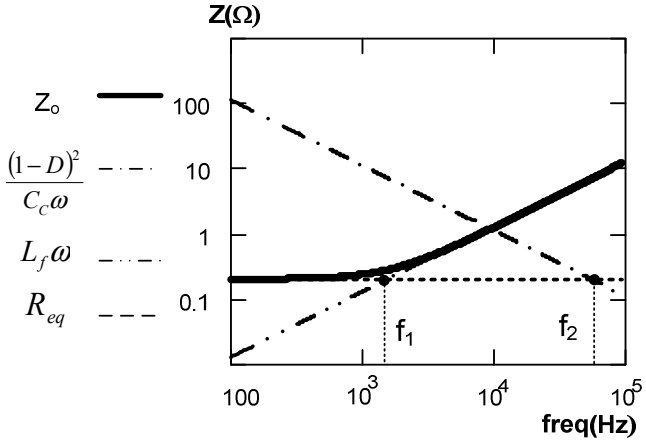

Fig. 9. Impedance Bode diagram. Corner frequencies.

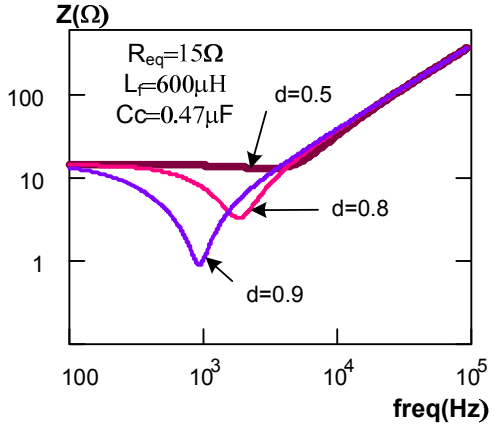

Fig. 10. Impedance Bode diagram for different duty cycles. Active clamp boost converter

$$f_1=\frac{L_rf_s}{\pi L_f} \quad (10)$$

$$f_2 = \frac{(1-d)^2}{4\pi L_r f_s C_c} \qquad (11)$$

However, the active clamp boost converter as high power factor rectifiers has an additional design problem: duty cycle changes and so input impedance also changes as shows Fig. 10. It has been designed a 3 stages PFC rectifier with the following parameters: V_{IN}=180-265V_{RMS}, V_o=400V, f_s=120kHz, Power=3x350W, L_r=70µH, L_f=700µH, C_C=0.47 µF. Simulated results for two different clamp capacitors are presented in Fig. 11, as can be noted when the duty cycle has the maximum value current share problems and oscillations appear. These problems increase for bigger clamp capacitors. When duty cycle is reduced dynamic problems disappear, and only steady state current share problems remain as a consequence of small differences added in duty cycles (Δd=0.01). It should be pointed out that input current has no oscillations. Oscillations appear as an unequal current share among different stages during transients.

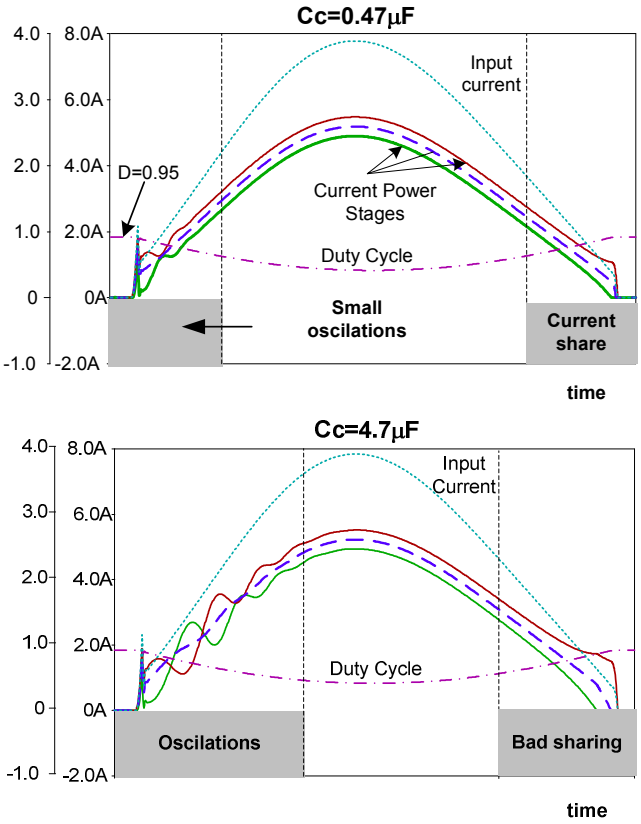

Fig. 11. Line input current and power stages input current for different clamp capacitor values.

V. EXPERIMENTAL RESULTS

The simulated converter presented in section 4 has been built, Fig. 12. The transistors are CoolMOS SPP20N60 and the diode is RHRP1560. Full load efficiency is 96% (without force cooling and EMI filter not included). Input current, input voltage, clamp capacitor voltage and input power of one power stage are shown in Fig. 13. Duty cycle is limited by the control circuit (UC3854), so clamp capacitor voltage decreases at low values of input voltages. Anyway, the theoretical value (52V) is similar to the measured value (56V).

Fig. 14 shows the input currents for three stages parallel connected. As can be seen in Table II for an input voltage of 220V_{rms} and Table II for 190V_{rms}, the maximum current mismatch at full load is 40mA. Although the L_r nominal value is 70µH, every inductor prototype has been measured: L_{r1}=68.5µH, L_{r2}=70.85µH, L_{r3}= 70.14µH. Small inductance differences will cause small input current mismatch as the experimental results show.

Oscillations or bad current sharing have not been observed in prototypes, where duty cycle differences are negligible. When Δd≈0 these problems disappear also in simulation.

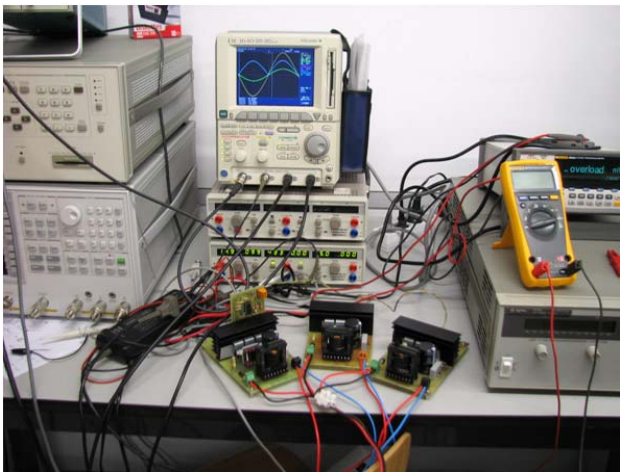

Fig. 12. Prototypes, 3x350W boost PFC rectifiers, only one control.

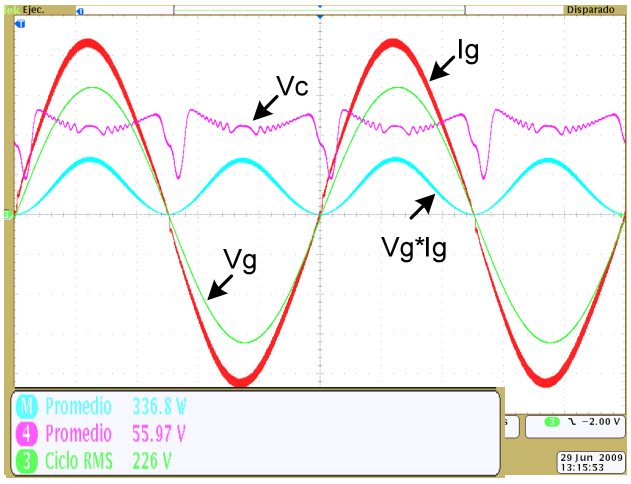

Fig. 13. Input current, Input voltage, clamp capacitor voltage and power measured in one prototype.

TABLE II (220V)

I_{Lf1} (A)	I_{Lf2} (A)	I_{Lf3} (A)	Power (W)
0.915	0.878	0.902	717
1.043	1.003	1.017	817
1.188	1.144	1.161	928
1.332	1.286	1.299	1035

TABLE III (190V)

I_{Lf1} (A)	I_{Lf2} (A)	I_{Lf3} (A)	Power (W)
1.065	1.017	1.053	733
1.204	1.154	1.173	812
1.347	1.303	1.318	907
1.515	1.454	1.558	1008

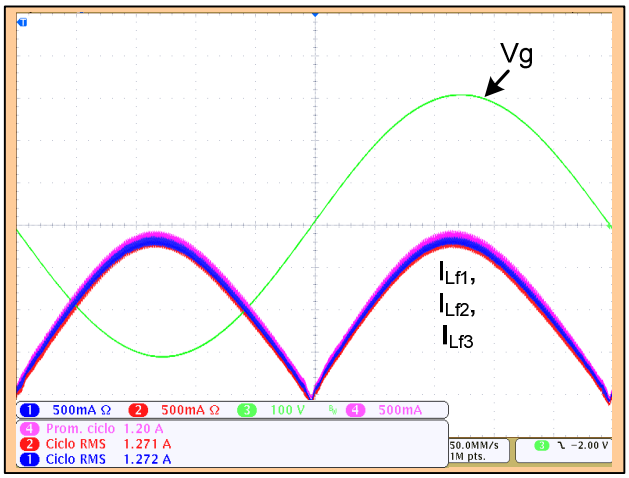

Fig. 14. Stages Input currents

VI. CONCLUSION

The input impedance of the active clamp boost converter has been proposed and tested as a method to equalize currents among k parallel stages in high power factor rectifiers. This method does not require any current sensor or control loop to share the currents among the different power stages and can be designed to avoid current imbalances even in the presence of large duty cycle mismatches or components tolerances. However, this topology is not the best option for universal voltage range converters. In these applications, the switching frequency must be changed in order to limit the semiconductor voltage stress. Clamp capacitor can be neglected for current share when is designed for high frequency operation (small values). Anyway, differences among the resonant inductors will take to differences among input currents and, therefore, to current distribution. However, it is easier to pay attention only to this parameter instead of the full converter.

The objective of this paper is to propose a method to design active power-factor-correctors for high power applications using multiphase ZVS boost converters and take advantage of the converter impedance to improve the current balance without using current loops. The converter efficiency is not the main objective of this work nevertheless the measured efficiency was 96% at full load operating at 120 kHz. Interleaving techniques can be used to reduce the input current rippled.

ACKNOWLEDGMENT

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