Pong Game
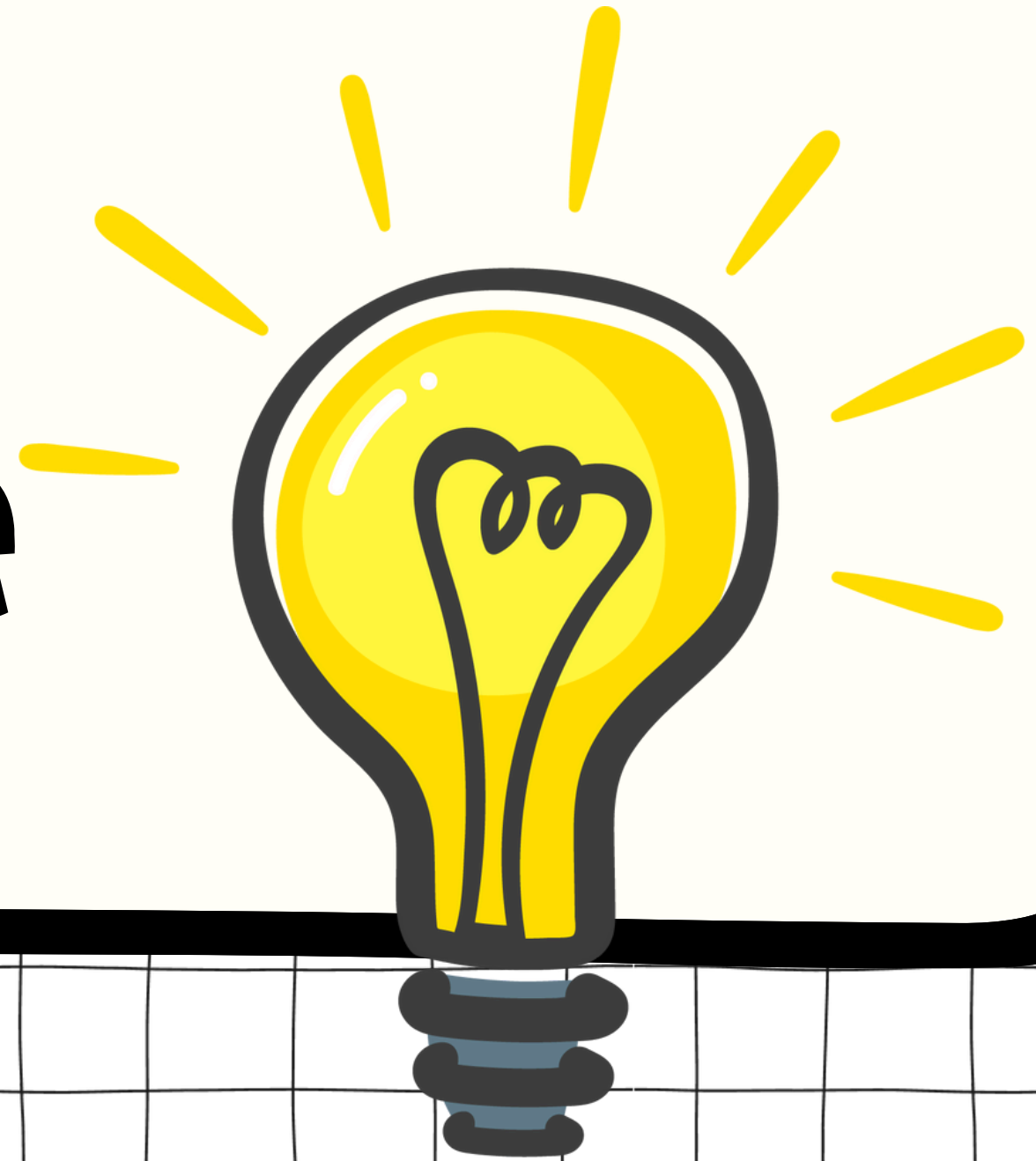
NCKU 數位系統實驗 期末專題 第一組

Introduction

一個酷酷的 Pong Game

1. 使用SevenDisplay來紀錄遊戲時間

2. 使用 Dot Matrix 紀錄玩家得分

3. 使用 KeyPad 來控制遊戲

4. 使用 VGA 來顯示遊戲畫面

Demo

https://youtu.be/Ks2PTz6LR7c?si=Cnb7uunXocdk2mc4

```verilog
module main(
    input clk,
    input rst,
    // gen up & down via key_pad_controller.v
    input [3:0] kp_col,
    input start,
    output Hsync,
    output Vsync,
    output [3:0] red,
    output [3:0] green,
    output [3:0] blue,
    output [7:0] dot_row1,
    output [7:0] dot_col1,
    output [7:0] dot_col2,
    output [6:0] sd_sec_dig1, //七段顯示器 Hex0
    output [6:0] sd_sec_dig2, //七段顯示器 Hex1
    output [6:0] sd_min, //七段顯示器 Hex2
    output [3:0] kp_row,
);
```

```verilog
// FSM Game Logic
always @(*)
begin
    state_d = state_q;
    score1_d = score1_q;
    score2_d = score2_q;
    stop = 1;
    newball_timer_start = 0;
        case(state_q)
            new_game:
                begin…
                end
            play:
                begin…
                end
            //when any of the player misses,
            new_ball:
                begin    …
                end
            over:
                begin …
                end
        endcase
end
```

```verilog
begin
    stop = 0;
    if(miss1)
    begin
        newball_timer_start = 1;
        score2_d = score2_q + 1;
        state_d = new_ball;
    end
    else if(miss2)
    begin
        newball_timer_start = 1;
        score1_d = score1_q + 1;
        state_d = new_ball;
    end
    else if(min == 0 && sec1 == 0 && sec2 == 0)
    begin
        state_d = over;
        stop = 1;
    end
    else
    begin
        state_d = play;
    end
end
```

```verilog
new_ball:
begin
    newball_timer_start = 1;
    if(clk_2s) state_d = play;
    else state_d = new_ball;
end
over:
begin
    // When time over. End the game
    if(clk_2s)
        state_d = new_game;
    else
        state_d = over;
end
```
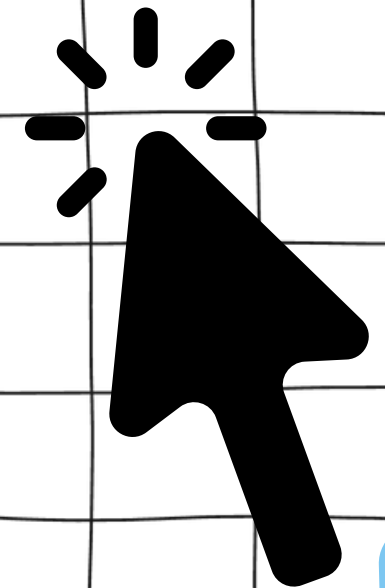
Module

dot_matrix
controller

Graphics
Generator

seven display
controller

VGA
Controller

Key Pad
Controller

state
machine

分工

1.專案架構
2.遊戲機制&
運動機制
Designer

AN4116039
張百鴻

1.專案架構
2.GraphGen
(VGA)
Designer

F74111055
余祥任

謝謝所有幫
助過我們的
助教！

C77777777
優質助教

Thank you

Verilog_FPGA_Pong_Game